DEVICE FABRICATION USING A DOUBLE LEVEL POLYSILICON SELF-ALIGNED PMOS PROCESS

Sally A. Plevniak
5th Year Microelectronic Engineering Student
Rochester Institute of Technology

ASTRACT

A double level polysilicon self-aligned PMOS process was used to fabricate an integrator circuit using a switch capacitor configuration at the input of an op amp. This process includes a spin-on dopant step to dope the first level of polysilicon while also doping the source and drain of the transistors on the design, thus creating self-aligned gates. The dielectric for the double polysilicon capacitors was a dry oxide on doped polysilicon which also served as the contact cut mask. Electrical testing included several test structures to evaluate process level performance. Problems with doping of the first polysilicon layer did not give good result which caused the circuit not to work. Several resistors did work on the Diffusion and second polysilicon layers.

INTRODUCTION

A conventional op amp integrator circuit is shown in Figure 1. The resistor, R, was replaced with two switches and a capacitor as shown in Figure 2a. The switches allow for a voltage of a specific frequency to be passed through the integrator op amp. The switches in Figure 2a are opened and closed by JK flip flop circuitry at a specific frequency which is much greater than that of the input signal. The whole redesigned integrator is shown in Figure 2b. The darkened portions of the schematic in Figure 2b involved a double level polysilicon PMOS process.

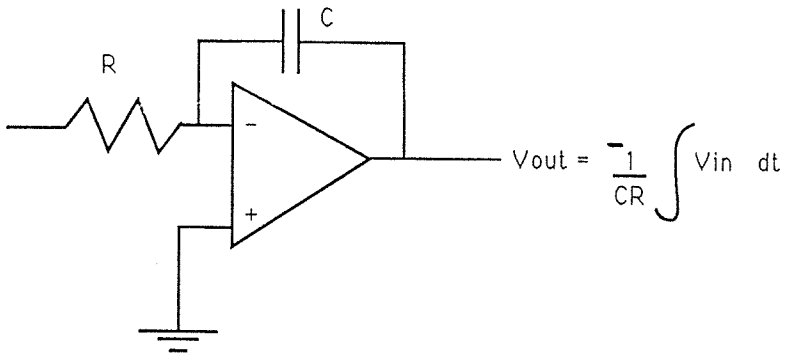

FIGURE 1: SCHEMATIC OF INTEGRATOR CIRCUIT

The above circuitry is compatible with the sophisticated designs on the microelectronics horizon. Chip density is increasing and the vertical density is also increasing. By using polysilicon as the conducting material on intermediate circuit layers, subsequent processing can be performed which may involve high temperature steps [1]. Due to the size of many capacitors needed, it is advantageous to use an intermediate polysilicon layer for the capacitor thereby leaving the substrate for more dense circuitry.

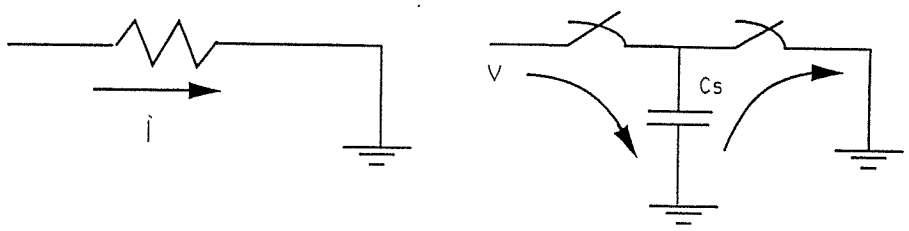

FIGURE 2a: THE SWITCHES ON THE RIGHT WILL SERVE THE SAME PURPOSE AS THE RESISTOR ON THE LEFT.

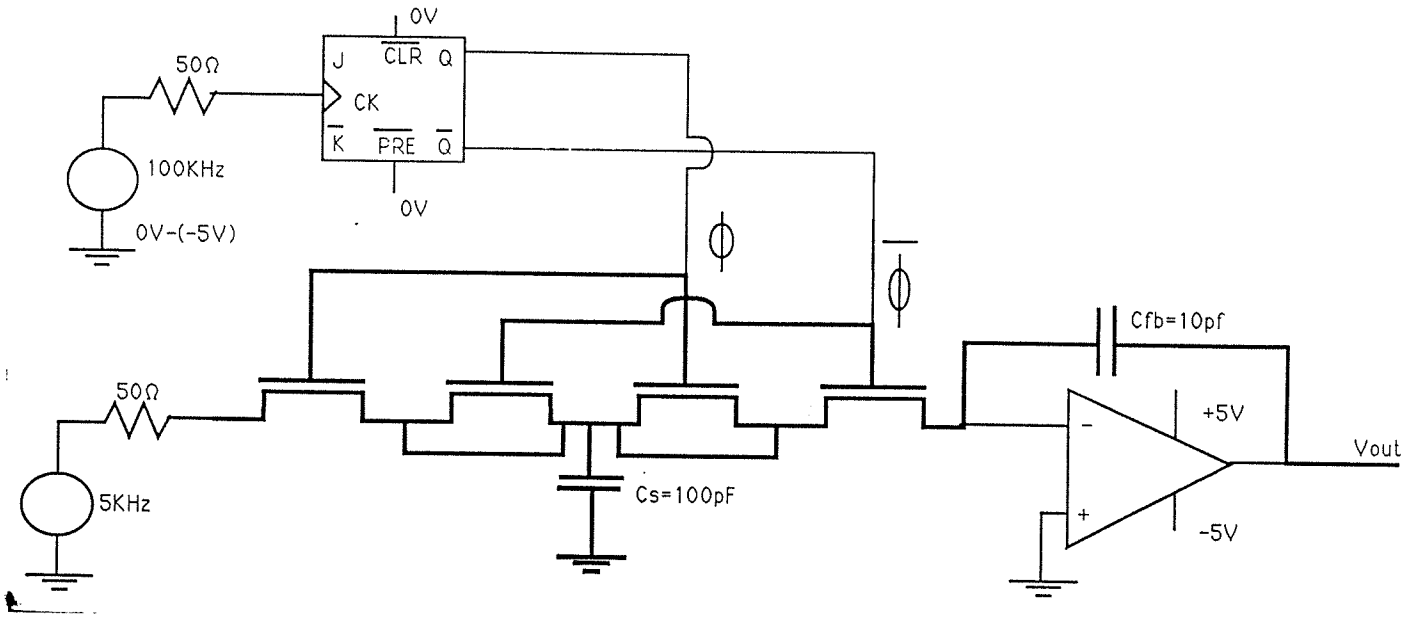

Figure 2b: Design Schematic of Integrator Op Amp

The process designed for this uses self-aligned source/drain technology with polysilicon as the gate material. This will give greater control over source and drain lateral diffusions by only allowing dopant to enter around the gate. Polysilicon has been incorporated into the process as the base for a polyI/oxide/polyII capacitor. The dielectric oxide will have to be as smooth and pure as possible to minimize leakage current in the poly/oxide/poly sandwich [2]. The final cross section will look similar to that of Figure 3.

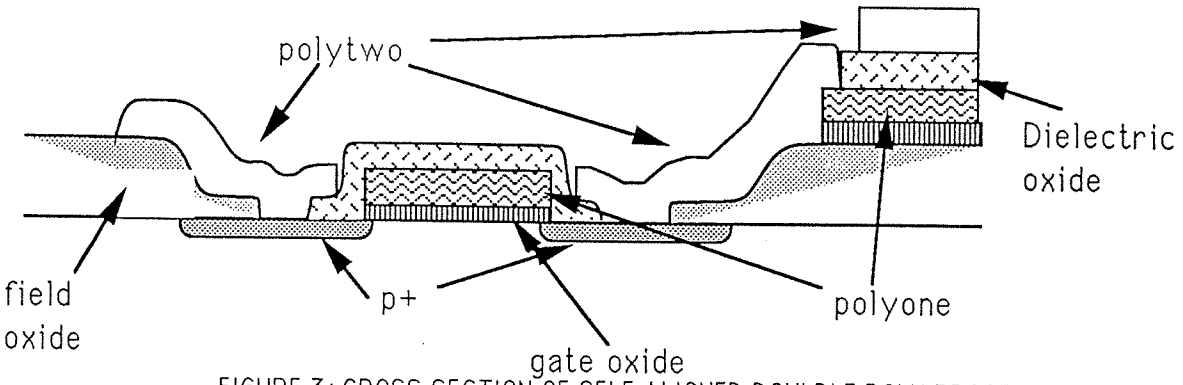

FIGURE 3: CROSS SECTION OF SELF ALIGNED DOULBLE POLY PROCESS

The main objective was to develop a process that could be used to fabricate the switch capacitor integrator circuit of Figure 1. The process includes two polysilicon layers which are used to create the 10pf and 100pf capacitors. The darkened portion of the circuit was the device designed using ICE. Several test devices were also placed on the die including several resistors and Van der Pauw structures in the DIFFUSION, POLYONE and POLYTWO layers.

EXPERIMENT

Eight n-type wafers were four point probed. Four were used as controls to determined process parameter results. A wet oxide was grown at 1100C for 47 minutes. Active area windows, the DIFFUSION layer, were patterned into the field oxide. A dry oxide growth was then performed at 1100C for 15 minutes to create a 510 angstrom gate oxide. The first polysilicon layer was then deposited by LPCVD at 610C with a 90 sccm silane flow rate for 66 minutes. A film of approximatley 6000 angstroms of polysilicon was deposited. Then the polysilicon was patterned, using the POLYONE mask layer. The wafers were then dry etched in the Tegal700 using a 3:1 ratio of SF6:02. After the poly is etched, the gate oxide over the source and drain regions was etched. With the source and drain exposed, the wafers were doped using Borofilm 100 spin-on dopant. This step also doped the POLYONE regions. After a drive-in of 5 minutes at 1100C the Borosilicate glass which formed after the drive-in was etched. The dry oxide dielectric was then grown at 1100C for 50 minutes. This also served as the CONTACT CUT masking layer which was then patterned. The second polysilicon layer was deposited the same way as the first layer was deposited. The thickness desired was approximately 5000 angstroms which took 55 minutes according to the previous deposition rate is used. The same spin-on dopant and doping procedures were used to dope the POLYTWO layer except the drive-in consisted of the additional 5 minute in a Nitrogen ambient at 1100C then the 5 minute wet 02 growth. The POLYTWO was then patterned and etched in SF6:02 with a ratio of 3:1. Aluminum was evaporated on the wafers, then patterned and etched.A final sinter of 450C for 15 minutes was performed in a forming gas ambient to consume native oxide in all contacts and to reduce the amount of fixed charges.

Table 1 summarizes the processing parametrs obtained. Results from similar processing are given in reference [3].

Table 1

Wafer Type	N-Type
Dopant Concentration	0.7E+15 /cm^3
Field Oxide Thickness	4800angstroms
Gate Oxide Thickness	530angstroms
Polyone Thickness	6000angstroms
Spin-On Dopant	Borofilm 100
Spin Speed/Time	3000rpm/25seconds
Polysilicon Dopant Concentration	0.5E+18/cm^3 - 0.9E+19/cm^3
Source/Drain Xj	1.5microns

RESULTS/DISCUSSION

The layout designed contained test structures for the Diffusion, Polyone and Polytwo layers. From previous work, sheet resistance was estimated at 200ohms/square for the diffused portions of the wafer. The polysilicon sheet resistance was estimated at approximately 200ohms/square for a 10 minute drive-in as taken from Izzio [4]. The only working devices obtained were a diffused resistor consisting of 36.15 squares and a polytwo resistor consisting of 47.15 squares. The expected resistances are 14.5Kohms and 9.43Kohms for the Diffused and Polytwo resistors respectively. Upon device testing, the Diffused resistor gave a value of 15.1Kohms and the Polytwo resistor gave a value of 4.5Kohms.

The Polyone resistor gave a plot similar to an opaen in the connections. No significant results were obtained for any Polyone device. Therefore the switching capacitor network was unable to be tested because the Polyone would not properly conduct.

There were several observations which may account for the defective Polyone layer. The Polyone was doped with the spin-on dopant Borofilm 100 then a drive-in was performed which consisted of a 5 minute wet 02 growth to strip the Borosilicate glass. It may have been that the oxide growth removed most of the spin-on dopant and did not properly drive-in. The second polysilicon layer was first doped and had a drive-in of 5 minutes in a Nitrogen ambient then the wet 02 growth to remove the Borosilicate glass. The Polytwo resistors had several working resistors.

CONCLUSIONS

Unfortunately no conclusive results were obtained to prove that the double polysilicon PMOS process producess working devices. The major drawback of the process was the uncharacterized doping procedure for polysilicon.

This process was set up for time constraint purposes and therefore may have been successful if there was more time to perform solid source diffusion for both polysilicon layers. To be sure that this is the problem, the wafers used here could be retested for sheet resistance and to see if the capacitors were conducting properly. There is a Polyone control wafer that could be tested to see if was the measured sheet resistance is after all subsequent processing on the wafers was performed. Once the doping problem is resolved, different dielectric glasses could be experimented with to produce the best conductivity in the capacitors. More test runs could also be performed to determine polysilicon oxide growth characteristics.

ACKNOWLEDGMENTS

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