GaAs MESFET LOGIC

Dave Petzold
5th Year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

Two 2" Gallium Arsenide wafers underwent MBE deposition processing to create two differing epitaxial layer schemes for processing of MESFET devices. A four level process was used to fabricate isolated MESFET structures, diodes, resistors, other test structures, and simple logic gates using Buffered FET Logic (BFL). Two ohmic contact schemes were utilized; Aluminum for an as-deposited contact to InGaAs and AuGe as an alloyed contact to GaAs. Results were working MESFETs with pinchoff voltages ranging from -1V to -4V, source to drain saturation currents ranging from 7 to 28 mA, and transconductances up to 22.4 milliSiemens. Schottky C-V and interdigitated diodes had threshold voltages of 0.4 to 0.6 volts. Logic reliability, however, was very low, with few gates functional.

THEORY

The MESFET device, a cross section of which follows in Figure 1, works on the simple property that depositing a rectifying contact (gate) on the surface of an n doped layer can control the current flow in the channel between the ohmic source and drain contacts on either side of the gate. This property is attained simply by placing a voltage on the gate metal that will form a depletion region in the channel to constrict current flow. No oxide or foreign barrier to current is needed, as the reverse biassed diode inhibits current flow from metal to substrate simply by the barrier potential between the two materials. Aluminum is the metal used in this project to form the Schottky contact.

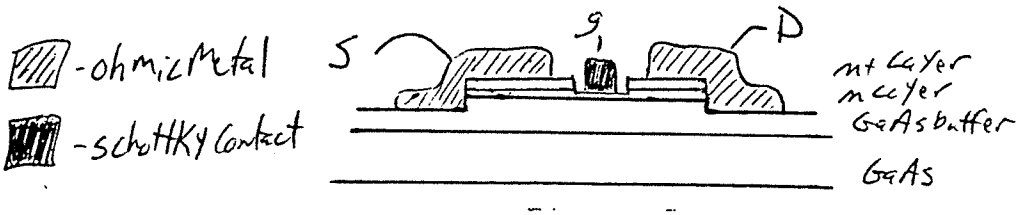
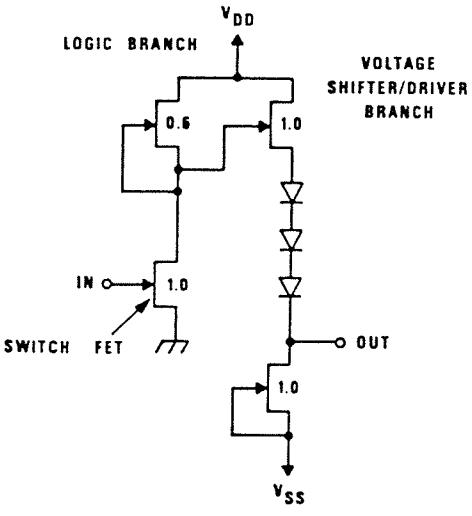


Figure 1: The MESFET Device

The ohmic contacts are formed by depositing Aluminum to n+ InGaAs or alloying deposited AuGe to n+ GaAs. The doped InGaAs wafer has a fermi level greater than the conduction band, thus producing the tunneling contact to the deposited Aluminum[1]. This characteristic is achieved at the surface by three thin (100 A) layers of highly doped (5E18 Si atoms/cm3) In(x)Ga(1-x)As deposited above MBE grown buffer, n, and n+ layers. The concentration of Indium increases with each layer such that x = 0.11, 0.35, and 0.98.

The alloy process for the AuGe contact to GaAs produces a thin layer of n++ Ge doped GaAs such to force the fermi level above the conduction band. Germanium exhibits an enhanced diffusivity into the donor sites of the doped GaAs at the elevated temperatures of the alloying process. Both these ohmic contacts give a free flow of electrons from metal to substrate and form the source and drain regions of the MESFET device.

Buffered FET logic, (BFL), was the first logic family utilized to fabricate GaAs integrated circuits. The schematic and a photograph of the fabricated gate in Figure 2 shows a typical BFL inverter circuit. The logic system uses depletion mode n-type MESFETs, thus requiring a negative voltage at the gate with respect to the source in order to pinchoff the channel current and put the transistor in the "off" state. BFL consists of two branch circuitry; the logic circuit, which performs the logic, and the voltage shifter branch, which inverts the logic output from the logic branch to be compatible with input voltages. The logic branch consists of MESFETs tied together in various ways, depending upon the logic function being modelled. The voltage shifter branch is made up of one or two MESFETs and two or three schottky diodes which are used for voltage level shifting. A second source voltage is needed to supply the transistor in the level shifting branch[2].



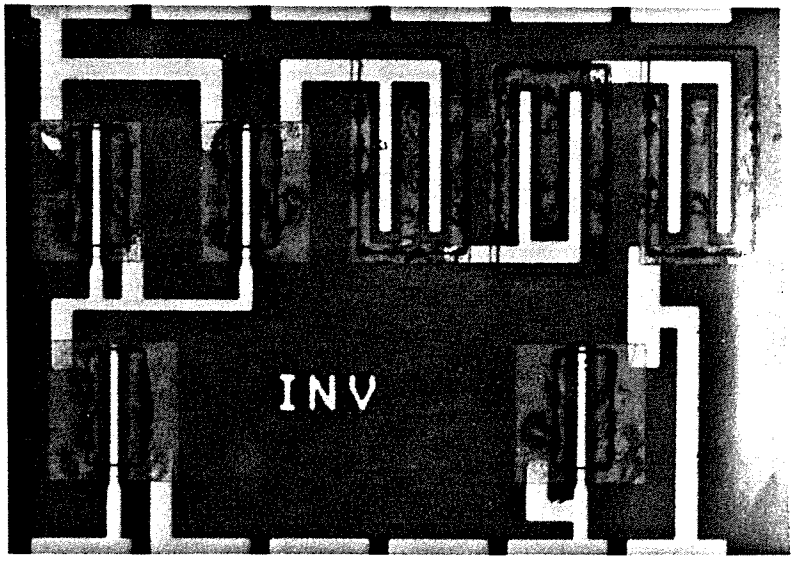


Figure 2: Inverter Design and Realization

EXPERIMENT

Shipley 1400-27 resist was used throughout the experiment to pattern the GaAs wafers for either substrate etch or metal liftoff steps. Wafers were quartered prior to process start to increase the number of samples to eight. Acetone and methanol were used in conjunction with an ultrasonic agitator for initial and subsequent cleans throughout processing.

Mesas were etched using a 1:1:3 solution of HF/H2O2/H2O with the purpose of isolating the FET regions. The height of the Mesa step was targeted at 6000-7000 Angstroms and was monitored using a Tencor Alpha Step after short etches and subtracting out the initial resist thickness. Approximate total etch time was 19 seconds.

Secondly, Ohmic Metal pads were defined using a chlorobenzene soak liftoff process and depositing either Aluminum or AuGe. A 10 second cleaning etch was performed prior to deposition of the metal with 1:2 NH4OH/H2O to remove any residual photoresist. Deposition of approximately 2000 Angstroms of either metal was performed by evaporation and liftoff was performed in acetone. Alloy of the AuGe contact scheme took place in a Mini-Brute tube furnace for 3, 3.5 or 4 minutes at a temperature of approximately 435 degrees Celsius.

Gate Recess Etch step was the third step and this defined the source to drain saturation current by wet etching through the n+ region and into the n region of the channel. Targeted current values varied from 40 to 80 mA and were monitored using a Tektronix curve tracer after short periods of wet etch. The etch took place in a solution of 1:1:100 NH4OH/H2O2/H2O after an initial surface clean of a 15 second 1:2 NH4OH/H2O etch.

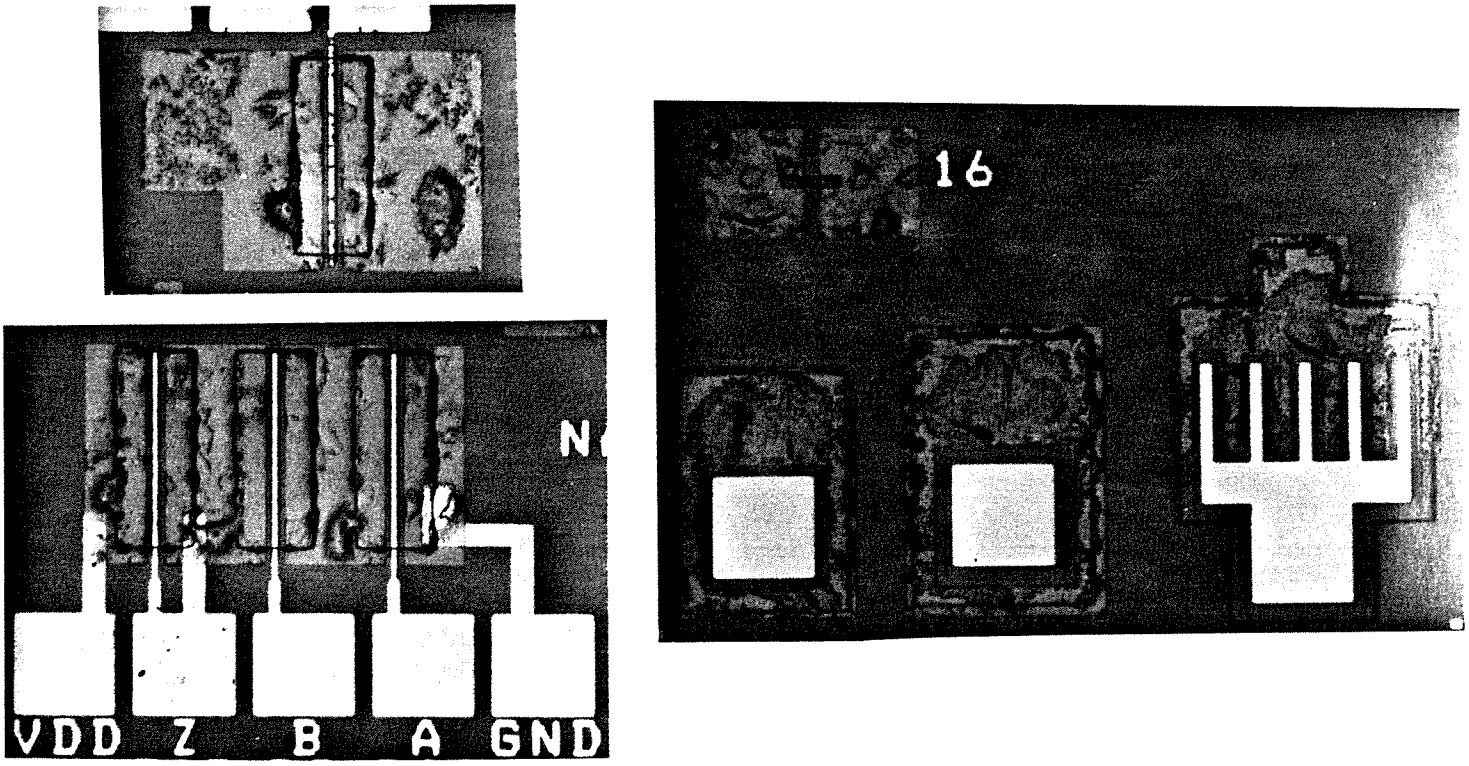
The fourth and final step deposited Aluminum for the gate metal and also electrically connected the devices in the logic ciruitry. Once again a chlorobenzene soak liftoff process was employed prior to develop. A two minute ash at 175 watts in oxygen followed by a 15 second wet etch clean in 1:2 NH4OH/H2O were performed to clear the small gate geometries of any residual photoresist. Deposition took place by evaporation.

RESULTS/DISCUSSION

Device evaluation took place using the HP4145 Parameter Analyzer. Results of drain to source saturation current were inconsistent with the Tektronix curve tracer. As a result, Idss values were less than 35 percent of the targeted value, in the range of 7 to 28 mA. Pinchoff voltages of the FETs ranged from -1 to -4 volts, and transconductances reached a maximum of 22.4 millisiemens. Schottky diodes had thresholds between 0.4 and 0.6 volts. Sheet resistance of the n+ layers were comparable at 48 ohms per square for InGaAs and 44 ohms per square for GaAs using values of two resistors of known number of squares. At the time

of writing this paper, a sole logic section of NAND gate was proven to be functional, without the inclusion of the level shifting section in the testing.

Figures 3,4, and 5 show photographs of the most successful isolated MESFET design (3 micron gate), the working NAND gate logic section, and 3 Schottky diodes, two of which are intended for C-V measurements and the last is interdigitated for series resistance minimization. Figure 6 on the following page shows the characteristic curve of the MESFET in Figure 3, fabricated using the AuGe/GaAs ohmic contact scheme.



Figures 3,4,5: MESFET, NAND Gate (Logic Section), Diodes

Conclusion

Gallium Arsenide Technology is being used throughout industry to make devices that are fast, radiation hard, and reliable. This project utilized MESFET Technology to implement Buffered FET Logic for simple digital circuitry. Sixteen logic and test cells were designed using this logic family, examples of which can be found in figure 2. Individual devices for test or monitoring purposes consisted of MESFETs, schottky diodes for both CV measurements and series resistance minimization, ohmic contact resistance measurements, resistors for sheet resistance calculations, and van der Pauw structures. Digital logic circuitry comprised the balance of the cells, which were designed to perform various logic functions.

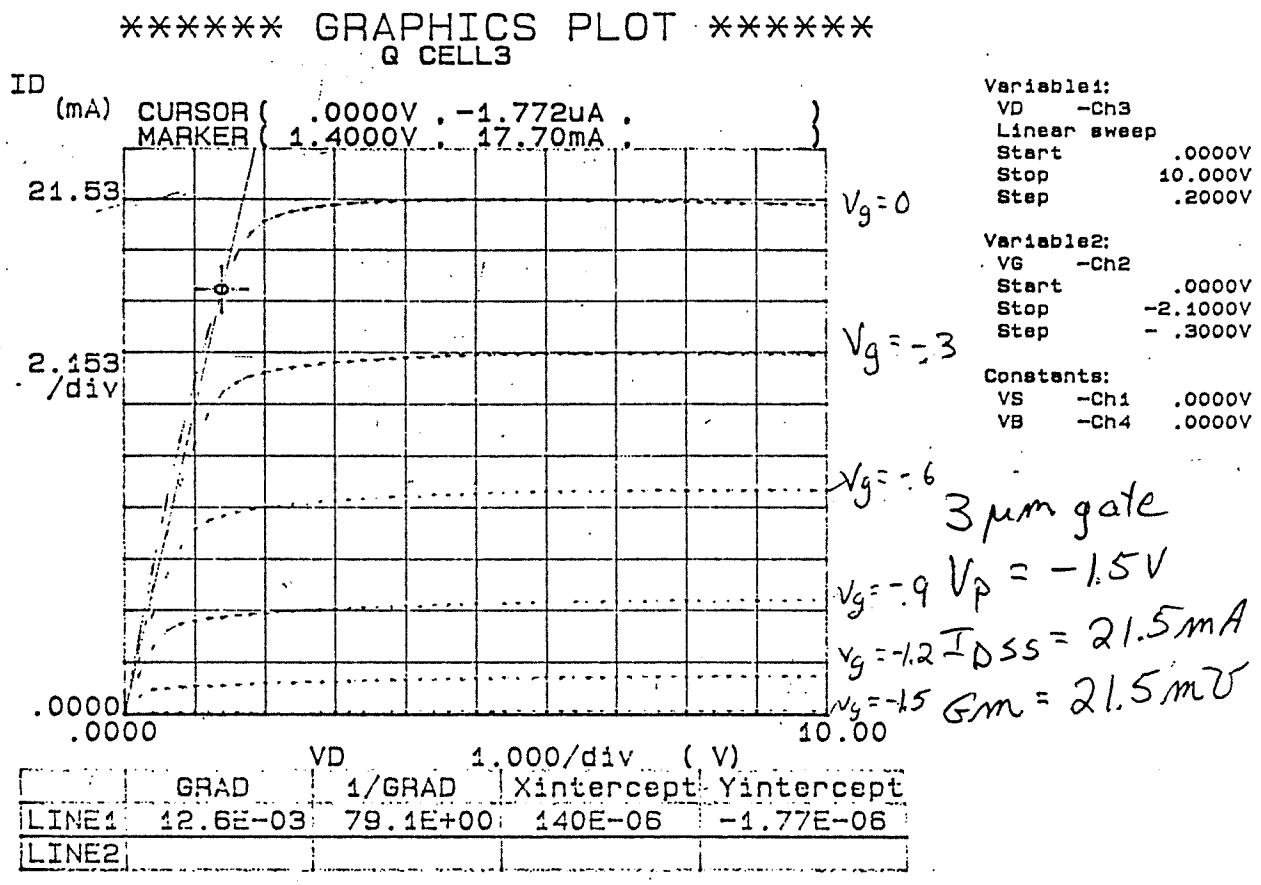


Figure 6: Characteristic Curve of a Fabricated MESFET Device

ACKNOWLEDGEMENTS

Thanks to Robert Hume of IBM for donation of the GaAs substrates and David Miller and Sabya Bose of the Pennsylvania State University for the growth of the MBE layers. Thanks to Mike Jackson and Bruce Smith for their availability and guidance during this project, and to Lynn Fuller for his correspondence with Penn State Faculty in setting up the MBE work. Special thanks to Vince Genova of IBM for his invaluable technical support throughout this project.

REFERENCES

[1] Woodall, J.M. et. al. J. Vac. Sci. and Tech. 19(3), September/October 1981, p. 626-7.

[2] David Haigh, Jeremy Everard. GaAs Technology and its impact on Circuits and Systems, (London: Peter Peregrinus, 1989.), pp. 190-191.