CAPACITANCE-VOLTAGE CHARACTERIZATION FOR POLYSILICON GATE MOS CAPACITORS

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ABSTRACT

The effects of an n-type and p-type doped polysilicon gate fabricated over both an n-type and p-type substrate for MOS capacitors with different polysilicon doping processing schemes was evaluated and compared to the current RIT process that utilizes a metal gate. Both boron and phosphorous spin on dopants were used to supply the conduction for the gate region of the polysilicon capacitors. Bias temperature bias was performed to evaluate the mobile ion contamination non-ideality, while a FORTRAN program was written to extract important capacitance voltage parameters from the actual C-V plots obtained that are of interest for MOS technologies.

INTRODUCTION

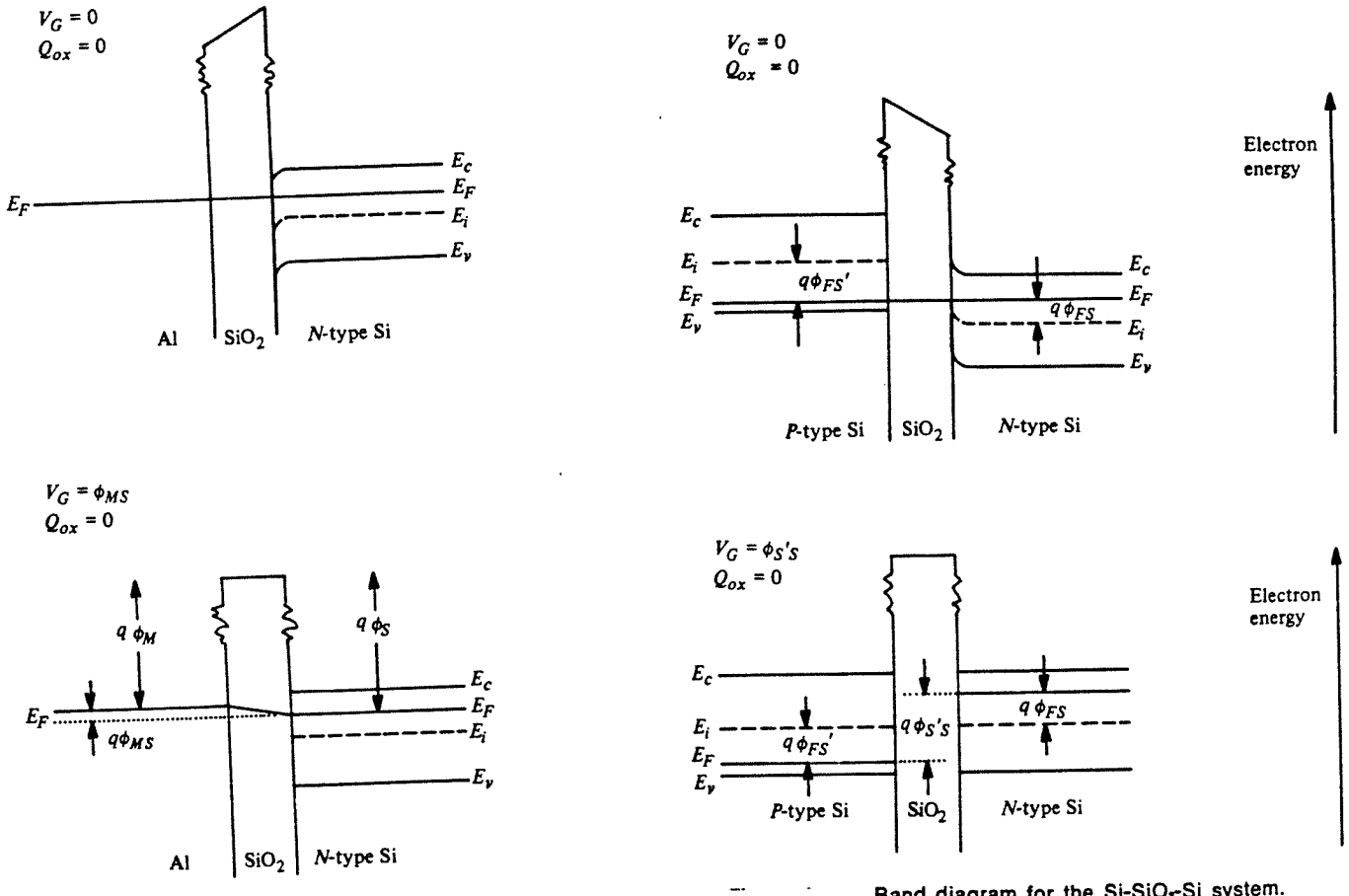
Due to their speed of operation, ease of fabrication and scalability, and quick processing time, MOS technologies are dominating the markets of modern microelectronic devices. The quality of a MOS device can be characterized by its C-V relationship and its deviation from the ideal case. The C-V characterization is a powerful diagnostic tool for identifying these deviations from the ideal case in both the oxide and semiconductor. Therefore, a large percentage of the MOS system fabricated can be analyzed by the differences between the observed and predicted C-V characteristics on a theoretical basis assuming an ideal structure.

The purpose of using a doped polysilicon gate is to reduce some of the non-idealities that are present in the aluminum gate devices. These non idealities are believed to arise from the CVC evaporation process at RIT. The evaporation system contains a coiled tungsten boat to hold the aluminum pellet that has sodium encorporated into it so that the coil may be bent. Upon evaporation of the aluminum pellet onto the wafers surface, sodium is also deposited. When subjected to bias temperature stressing, a common reliability-testing procedure where a device is heated under bias to accelerate device-degrading processes, the MOS structures should display a severe instability and the C-V plot should shift due to the mobile ions in the gate oxide.

Instead of using an aluminum gate, a phosphorous doped polysilicon gate could be used to reduce the alkali metal contamination. During the diffusion, phosphorous enters the outer portion of the silicon dioxide film layer and becomes encorporated into the bonding structure, thereby forming a new thin layer referred to as a phosphosilicate glass. At the diffusion temperature the mobile ions are extremely mobile and wander into this glass region of the oxide. Once in the phosphosilicate glass, the ions become trapped and stay trapped when the system is cooled. The alkali metals are essentially "gettered" out of the oxide and are positioned near the interface where they give rise to the least amount of C-V shifting and are held firmly in place during normal operating conditions.

The flatband voltage and the threshold voltage is a function of the work function difference between the gate and the silicon substrate. This difference depends largely on the substrate doping, and on the polysilicon doping level (or the metal gate work function). The energy band diagrams below in Figure 1 show a typical metal gate structure and a p-type polysilicon doping structure.

Figure 1: Typical metal gate structure and a p-type polysilicon doping structures



Band diagram for the Al-SiO_2-Si system.

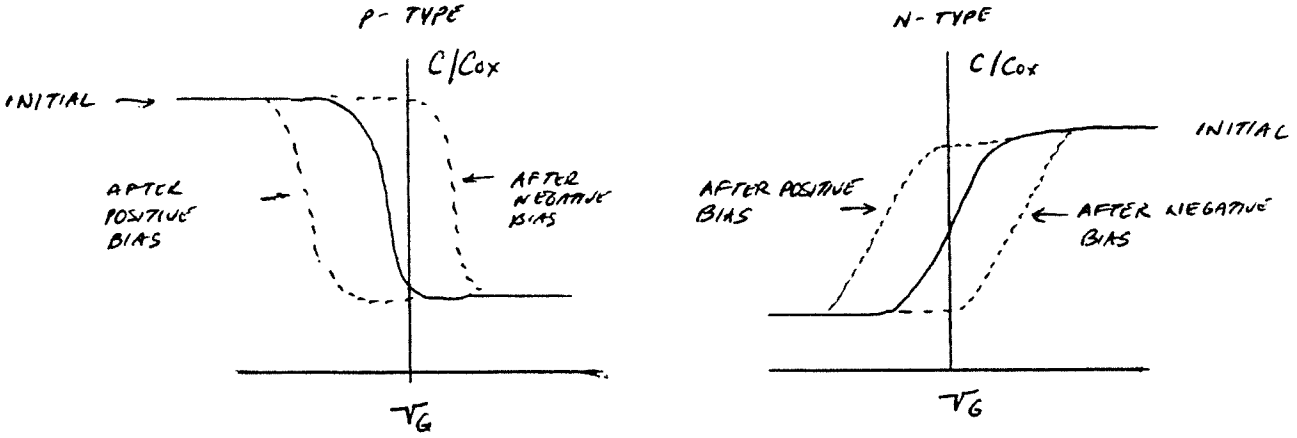
Band diagram for the Si-SiO_2-Si system.

When the aluminum gate is replaced by the doped polysilicon gate, the work function between the gate electrode and the silicon substrate is changed. By assuming that a band analysis is valid for the polycrystalline silicon, the effective work function difference (phigs) is given by the equation

$$phigs = phig - phis$$

where phig is the Fermi potential in the gate silicon. Silicon gate MOS structures represent a way to achieve low threshold voltages. Other advantages of the doped polycrystalline silicon over aluminum gate include high temperature processing steps which allows for complete reorganization of the MOS fabrication sequence (ie. multilayer polysilicon MOS capacitors). For RIT, an advantage would be reduced mobile ion contamination in the oxide since no metal is used. Typical high frequency C-V plots for n and p type wafers are shown below in Figure 2 with bias temperature shifts.

Figure 2: Typical high frequency C-V plots for n and p type wafers with bias temperature shifts



EXPERIMENT

The main objectives were to develop a process to fabricate the doped polysilicon MOS capacitors, test the effects of a bias temperature stress and compare the results to those obtained for a a metal gate by inspecting such parameters as flatband voltage, flatband voltage shift, threshold voltage and flatband capacitance. A FORTRAN program was written to perform the needed calculations.

The wafers were four point probed to determine the bulk doping level and an RCA clean was performed to remove the organics and silicon chips from the scribe procedure. A 500 angstrom thin oxide growth was performed at 1100C in a dry oxygen ambient for 15 minutes followed by an 1100C nitrogen ambient anneal for 30 minutes. Since fixed oxide charge is a strong function of the oxidation conditions, the anneal was performed to reduce the amount of fixed charge. The gate oxide thickness was measured to find the oxide capacitance.

Polysilicon was deposited at 610C (flat profile) with 50 sccm silane for 53 minutes and dummy wafers were used in the load as a radiation shield. Prior to the spin on dopant application, an RCA clean with 20 second 1:10 HF dip was performed to provide the optimum surface for impurity application. Borofilm 100 was used as the boron impurity source while Diffusion Technology P-854 was used as the phosphorous impurity source. The spin on dopants were coated at 3000 RPM for 25 seconds using a hand spinner technique and then the wafers were prebaked at 200C for 15 minutes to drive off the solvents. The impurities were then diffused and driven into the polysilicon in a 5 lpm nitrogen ambient at 1100C for the three different times of 10, 20 and 30 minutes. Upon completion the wafers received a buffered HF dip to remove the doped glass on the polysilicon and then the wafers were four point probed to determine doping levels and sheet resistance.

The wafers were patterned using the capacitor mask at an exposure dose of 45 mJ/cm2. The Tegal 700 was used to selectively etch the doped polysilicon to photoresist and oxide. The parameters that were used are shown below in Table 1.

Table 1: Tegal 700 parameters for etching doped polysilicon

Base pressure: 225 mtorr
Forward power: 125 W
Reverse power: <5 W
Operating pressure: 600 mtorr
SF6 flow: 10 sccm
O2 flow: 3.3 sccm
SF6:O2 3.03:1
Time boron doped: 40 sec
Time phosphorous doped: 30 sec

A 5 lpm 10%H290%N2 450C 15 minutes sinter in forming gas was performed to consume native oxide on the contact. The wafers were tested using a high frequency C-V set up. The operating frequency was 1 MHz. Bias temperature stressing was performed at 200C for various times and applied voltage.

RESULTS

The polysilicon resistivity was measured on the control wafers with only marginal results. It was expected that the different diffusion times would produce very different doping concentrations, but according to the four point probe results, this is not the case as shown below in Table 3.

Table 3: Doped polysilicon resistivity results

Dopant type	Drive-in time (min)	Rho (ohm-cm)	Rhos (ohm/sq)	N (x10E15 atoms/cm3)
p (boron)	10	8.146	213.8	1.6370
	*20	n o t	p e r f o r m e d	
	30	2.251	59.07	6.4898
n (phosphorous)	10	0.648	17.01	7.5880
	20	0.649	17.02	7.5810
	30	0.646	16.94	7.6190

The doping level of the polysilicon remained essentially constant for the various phosphorous diffusions, which suggests that the temperature at which the polysilicon was grown or the diffusion temperature maybe the major contributors to the doping level. Table 4 below show the results of testing the MOS capacitors. These tests were conducted at room temperature and no bias temperature stressing was supplied.

Table 4: MOS capacitor results

CAPACITOR TYPE G:ST:DT	VT V	VFB V	C/COX -	CFB pF	NSS states/cm2V	RS ohm/sq
P+:P:10	4.5	0.6	0.416	333	1.8e12	152
P+:N:10	1.6	2.4	0.341	232	8.4E11	170
N+:N:10	-1.0	-0.2	0.351	232	9.0E10	112
N+:N:20	-1.0	-0.2	0.346	230	9.2E10	183
N+:P:20	1.0	-0.8	0.376	262	1.2E12	100
N+:N:30	-1.0	-0.2	0.343	231	9.3E10	152
N+:P:30	0.5	-1.0	0.423	326	1.1E12	81
M :N:0	-2.3	-1.5	0.380	246	3.7E11	115
M :P:0	-0.5	-1.7	0.376	250	4.5E11	70

WHERE: P+: boron doped polysilicon gate
N+: phosphorous doped polysilicon gate
M : metal gate
P : p-type substrate
N : n-type substrate
G : electrode gate type
ST: substrate type
DT: diffusion time

The flatband voltage (VFB) is read directly from the C-V graph after the debye capacitance and the corrected oxide capacitance was calculated. The flatband capacitance (CFB) assumes one-dimensional uniform substrate doping. Table 4 shows that the doped polysilicon gate MOS capacitors lowered the effective threshold voltage as expected. NSS, the surface state density

was the smallest (ie. 1e10 range) on doped n-type wafers, while all the p-type doped polysilicon gate capacitors yield high NSS values (ie. 1E12 range). The metal gate capacitors resulted in NSS between these two ranges. The series resistance values obtained are reasonable, meaning, that with proper equipment a more intense study of MOS non-idealities can be made.

No C-V results were obtained for the 15 minute and 20 minute boron doped polysilicon gate because it is believed that since boron is a fast diffuser due to its high diffusivity rate, it diffused through the oxide and into the silicon substrate. Hence, the gate oxide thickness should be increased to approximately 800 angstroms for a 20-30 minute diffusion.

SUMMARY

Bias temperature stressing of the doped polysilicon gate MOS capacitors at +/-20V and +/-30V at 200C showed no observable flatband shift. However, at voltages greater than +/-30V, it appeared that the oxide broke down and the probe was essentially shorted to the substrate and the chuck. The metal gate MOS capacitors however, showed a 2 to 3 volt shift in the C-V plot when stressed. It appears that the sodium from the CVC evaporator is the culprit for mobile ion contamination in the oxide. Therefore, if it is critical to control this non-ideality for a device, a polysilicon gate should be utilized.

SUGGESTIONS FOR FUTURE WORK

It is recommended, however, that for process optimization, an experiment with a two-step diffusion should be implemented as part of a Box-Behnken analysis. By using a two-step process, the dopant can be reorganized in the polysilicon to provide a more uniform doping distribution throughout the polysilicon thickness. However, it must be stressed that if the dopant diffuses through the polysilicon and penetrates the gate oxide, this will have an adverse effect on the C-V characteristic curve by shifting the curve, which is due to the introduction of additional impurity non- idealities. It should be noted that the boron and phosphorous diffusivity rate is different, boron being the faster diffuser, and more care is needed when developing and performing a two-step diffusion process to insure that gate oxide doping does not occur. If a two-step process is implemented, then the gate oxide thickness for the boron impurity should be increased so the substrate does not become heavily doped.

ACKNOWLEDGEMENTS

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