POLYSILICON vs. ALUMINUM GATE PMOS RING OSCILLATORS

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ABSTRACT

A nine stage PMOS ring oscillator was designed using polysilicon gates for a self-aligning process while another was designed using a standard metal gate process. A comparison of the polysilicon and metal gate PMOS processes was planned to show the reduced gate capacitance of the self-aligning process. This reduced gate capacitance was to be observed by measuring and comparing the propagation delay of each design on the oscilloscope.

INTRODUCTION

A ring oscillator is an electrical circuit that is used to measure the time required for a signal to travel through an odd number of inverters serially connected. That is, the output of one inverter stage is used as the input to the next stage. The inverter gain is used to restore any signal loss as it travels through the interconnection material. The minority carrier mobility, the channel resistance, gate capacitance, and the interconnect material capacitance and resistance are some of the main parameters that affect the propagation delay through an inverter. N-type minority carriers have larger mobilities than P-type carriers. Therefore, NMOS technologies are preferred over PMOS when cicuit speed is critical in a design. Channel resistance and gate capacitance of a transistor combine to yield the RC delay time constant as shown in Equation 1.

$$T = RC \qquad (1)$$

This is the minimum time required for charge to pass from the source to drain of a MOS transistor when a gate voltage greater than the threshold voltage is applied. The RC delay time is used in the calculation of the inverter pair delay time. The pair

delay time is the combined rise and fall times of the inverter. The rise time is the amount of time required for the inverter to charge from a low ouput voltage to a high output voltage. The fall time is the time it takes the inverter to discharge from a high output voltage to a low one. Equation 2 for the pair delay time is given below:

$$Tp = T(1 + K) \frac{Ctot}{Cg} (x) \qquad (2)$$

where T is the RC delay time, Ctot is the total gate and stray capacitance, Cg is the gate capacitance, and x is the number of transistor gates. The stray capacitance is the capacitance associated with the interconnect material. The constant K, which is the square of the inverter gain, is calculated using Equation 3.

$$K = \frac{(L/W)\ \text{pull-up transistor}}{(L/W)\ \text{pull-down transsitor}} \qquad (3)$$

Where L and W are the lengths and widths of the pull-up and pull-down transistor gates of the inverter. Figure 1 shows an example of an inverter and figure 2 shows a ring oscillator.

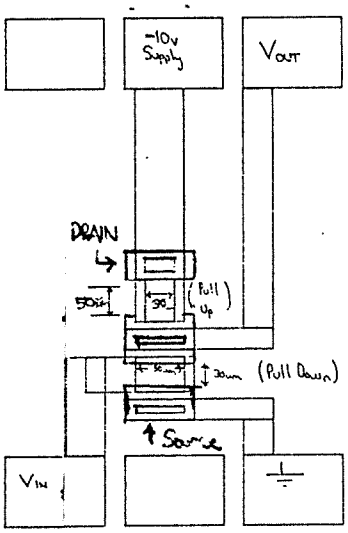


Figure 1:(Metal gate inverter)

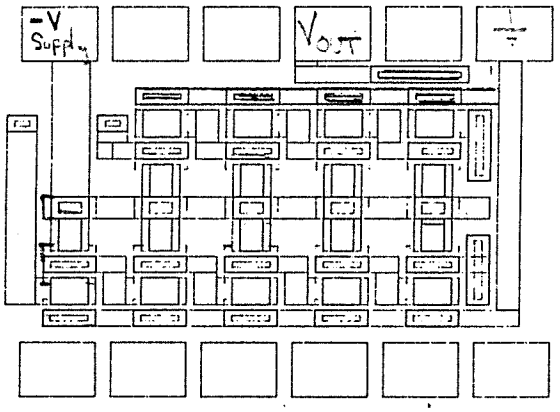


Figure 2:(9 stage ring oscillator)

As shown by the equation for the pair delay time, the gate capacitance has a direct effect on the inverter pair delay time. Keeping the designed gate capacitance small will result in shorter propagation delay times. This results in faster circuit performance.

The polysilicon gate PMOS process provides the opportunity to reduce the gate capacitance of each inverter substantially

over the standard metal gate process. This is because the polysilicon process is self-aligning. In the polysilicon process, the gate region is defined in the beginning of the process. Polysilicon has the ability to withstand the thermal temperatures of the source and drain diffusion. Aluminum does not have this property, it would flow. Because polysilicon can withstand thermal processing, the source and drain diffusion can be performed with the gate region already defined. Thus the lateral diffusion of the source and drain dopant automatically aligns the source and drain to the gate. In the standard metal gate process, the source and drain regions are defined first in the subtrate. The gate is defined by aligning the gate oxide to the source and drain with a designed 1 lambda overlap over each. This overlap is required to offset any worst case misalignment error. This overlap is the source of additional parasitic gate capacitance. The polysilicon process tends to minimize this parasitic capacitance through self-alignment. The reduced gate capacitance of the polysilicon process should translate into faster pair delay times as given by Equation 2. For this experiment, it is assumed that the stray capacitance of each design (polysilicon and metal gate) is the same as well as the RC delay time constant. A cross-section of each process is shown below in Figure 3.

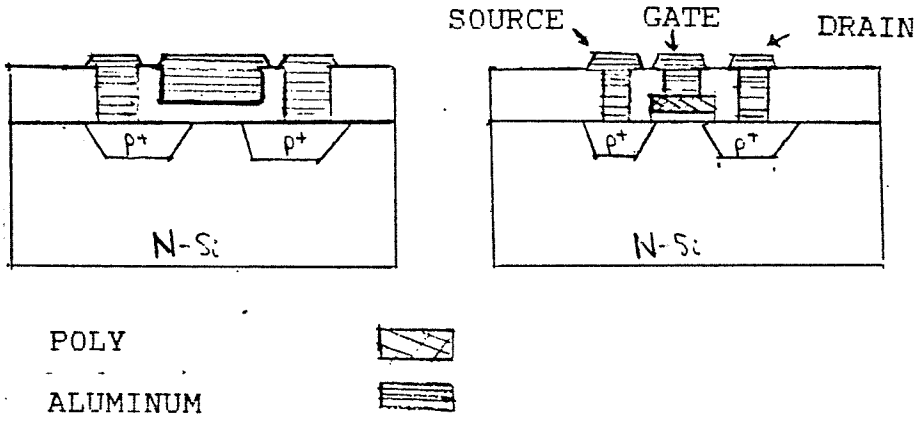


Figure 3: (Cross-section comparison of metal gate and poly gate PMOS- metal gate is on the left, poly gate is on the right.)

EXPERIMENT

A 4 mask level process was designed for each oscillator. For the standard metal gate process, a 5000 A masking oxide was grown on n-type (1 0 0) wafers. The first mask level defined the source and drain regions in photoresist. The oxide was then etched back to the substrate. B-150 spin-on dopant was then predoposited at 1100 C for 10 minutes in wet O2. The borosilcate glass was then stripped back and the boron driven in for 40 minutes at 1100 C in wet O2. The second level mask was

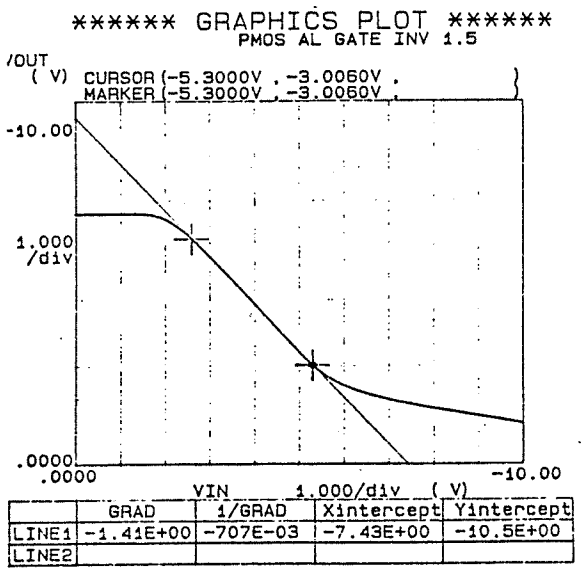
then used to define the gate regions in the photoresist. The oxide was then etched back to the substrate. A 500 A gate oxide using a TCA tube clean was then performed. This was a 12 minute dry 02 growth at 1100C. The third mask level was then used to define the contact openings to the source and drain diffusions. The oxide over these regions was then etched back to the substrate. Aluminum was then evaporated on to the wafers. The fourth mask level was used to pattern the metal. An aluminum etch and a 30 minute foming gas sinter at 450 C was performed.

For the polysilcon process, it also commenced with the growth of a 5000 A masking oxide. The first mask level defined all the inverter areas with the oxide etched back to the substrate. Growth of a 500 A gate oxide as above followed by a minimum LPCVD deposition of 5000 A polysilicon. Patterning of the gate regions with the second level mask. Etching of the polysilicon using a Tegal plasma etcher with SF6 and 02 etchant gases. Wet etch of the gate oxide. Boron predeposition as above. Drive-in of the boron at 1100 C for 20 minutes in wet)2. The third and fourth mask levels performed as above.

The oscillators were tested using a Textronics digital oscilloscope. To test these devices, -10 volts was applied to the drain of each inverter pull-up transistor. The source of each pull-down transistor was connected to ground. The output of one inverter was connected to a pad to view the waveform.

TESTING/DISCUSSION

The following figures (Figures 4 and 5) show the produced inverter gain and oscillator waveform of the metal gate process.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-1.41E+00	-707E-03	-7.43E+00	-10.5E+00
LINE2				

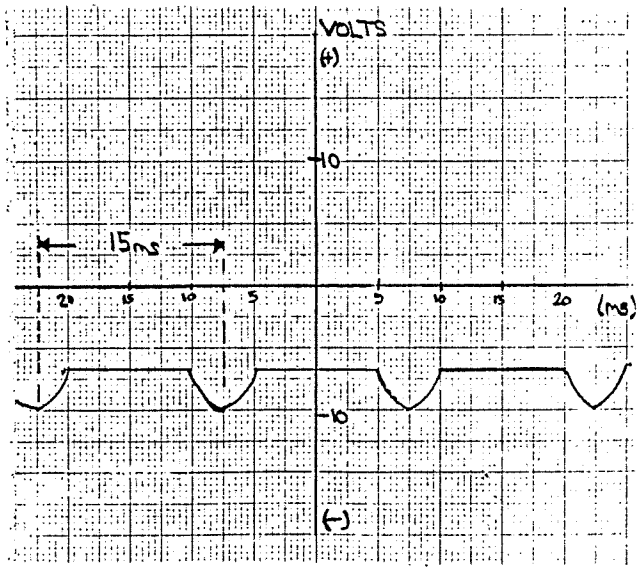


FIGURE 4:(Inverter Gain) Figure 5: (Oscillator waveform)

The threshold voltage that was measured was approximately -2.0 volts. The propagation delay as measured across 5 different locations was determined to be about 1.6 milliseconds. SPICE predicted a propagation delay of 110 nanoseconds based on the measured gate oxide thickness. The measured delay time is considerably slower than predicted. When the individual inverter gains were measured, the average gain was approximately 1.4. However, the gain was not inverted as shown. There were kinks in many of the plots of Vin vs. Vout. Also observed was a non-consistent input transistion voltage to swing the output voltage high. Because the measured propagation delay is so slow, it appears that there must have been some unaccounted for resistance and capacitance. Contact resistance had not been taken into account. It was very difficult to obtain measurements for most of the oscillators and diagnostic devices. A small amount of oxide (if it had not been entirely etched) in the contact cuts is probably to blame. This would greatly effect the circuit speed. Another possible explanation would be that the stray capacitance of the metal gate ring oscillator was much larger than expected. This would cause the charging and discharging of the output of the inverter to be unusually slow.

The polysilicon process was scrapped after the second mask level. A design error was discovered with the polysilicon gates, and it was determined the source and drain diffusions would short together.

CONCLUSIONS

The results of this experiment did not allow for any conclusions to be made. Once a polysilcon device can be fabricated, preferably in parallel with the metal gate device, some comparisons and conclusions about circuit speed can be arrived at

ACKNOWLEDGMENTS

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