EVALUATION OF AN ENHANCEMENT PMOS OPERATIONAL AMPLIFIER

Hung Q. Doan
5th Year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

An all enhancement PMOS op amp was designed and fabricated using the RIT standard PMOS process. The mask contained diagnostic components (resistors, discrete transistors and van der Pauw resistors), discrete stages of the op amp circuit, and a complete op amp circuit. Non-working op amp circuits were found due to parasitic loses. Circuit simulation using SPICE was performed. It was shown that inverter with the gain higher than 25 is not possible and the transistor load as a current source degraded the stage performances.

INTRODUCTION

Operational amplifiers (op amp) are used extensively in linear and non-linear applications. The ideal op amp has a high input impedance, a high voltage gain, and a low output impedance. The project is a fabrication of an all enhancement PMOS op amp. Figure 1 is the schematic of the op amp circuit [1]. The corresponding numbers at each device is the length to width ratio of the transistor gate. The op amp connections consist of two inputs (inverting and non-inverting), two voltage supplies, and the output. Its output voltage swing is limited by the supply voltages. The circuit consists of three distinct stages; the differential input stage, the differential converter stage, and the second gain stage.

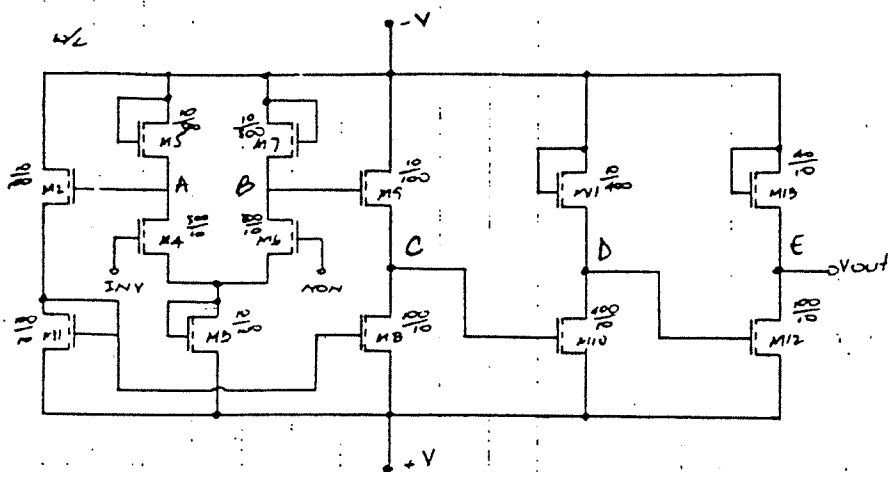

Figure 1: PMOS Op Amp circuit.

The input section contains four transistors (M4, M5, M6, and M7) and a current source transistor, M3. The stage is similar to two inverters in parallel. Nodes A and B in Figure 1 are the outputs of this stage. The output, A or B, pulls low (+V) when M4 or M6 turns on. Otherwise, it stays high, -V. The gain of the stage is 50.

The converter stage also contains four transistors; M1, M2, M8, and M9. The stage is a voltage follower having no voltage gain. The outputs from the input stage are the inputs of the converter. The converter inverts one of the outputs and combines the two outputs into a single output at node C. If node A is high, M2 turns on, M1 and M8 will also turn on. Node C pulls low, +V, which is inverted. If node B is high, M9 turns on and node C pulls high, -V.

The second gain stage has two inverters. One inverter has the gain of 40 (M10 and M11) and the other has the gain of 1.6 (M12 and M13). The total gain of the circuit is 3200 (50x40x1.6) or 70 decibels.

The circuit has been fabricated here at RIT but non working or inconsistent op amps are obtained. This project also included testing of discrete transistors, resistors and each individual stage of the op amp circuit. Op amp performance is characterized by the following parameters: input impedance, output impedance, input offset (voltage and current), slew rate, frequency response, and common mode rejection ratio. Detail of each parameter can be found in Reference [2] and [3]. If a working op amp is realized, it will be characterized for the above specifications.

EXPERIMENT

The chip design consisting of discrete PMOS transistors, resistors, van der Pauw resistors, discrete stages of the circuit, and a complete op amp circuit was created. The design was fabricated on a 5 ohm-cm (100) n-substrate following the RIT standard PMOS process [1]. Discrete transistors were tested and parameters extracted for computer simulations using SPICE. Each stage of the circuit was simulated for transfer characteristics. The fabricated circuits were tested and compared with the simulations.

RESULTS/DISCUSSION

Figure 2 is the output curve of a discrete transistor. The threshold voltage is about -2.5 volts. Figure 3 is the output curve for the M10 device that is obtained from the op amp circuit. Unlike Figure 2, Figure 3 is similar to a short channel transistor. The current increases with the drain voltage in the saturation region and the drain current does not switch off the, even with no voltage on the gate. The short channel effect is found in a higher region of density of devices, but not for the discrete device. The short channel effect usually does not occur for less than 1.5 microns channel length devices and the minimum channel length used in this case is 10 microns.

Figure 4 is the experimental characteristic of the 1.6 gain inverter (M12 and M13) in the second gain stage. The supply voltages are -10 and +10 volts. It is desired to have the maximum and minimum swings of -7.5 and 10 volts. The pull up is distorted by one threshold, -2.5 volt, due to the shorted gate to drain configuration. The maximum and minimum voltages are measured to be -3 and 8 volts. The pull up is distorted by 7.0 volts and the pull down is distorted by 1.5 volts. The distortions are caused by the voltage drop across the parasitic resistance. The parasitic resistance is the combination of the contact resistance, source or drain resistance, and the channel resistance of the transistor. The pull up transistor has a potential difference between the source and the bulk. This increases the threshold voltage, called body effect, and decreases the maximum output voltage. The effect is relatively small, 1 to 2 volts.

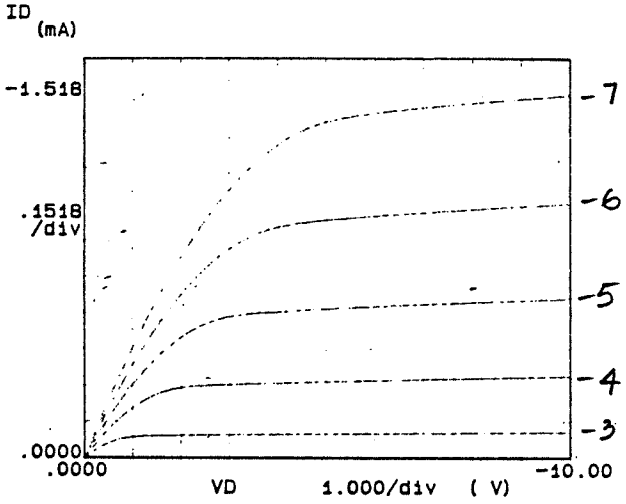

Figure 2: Discrete transistor.

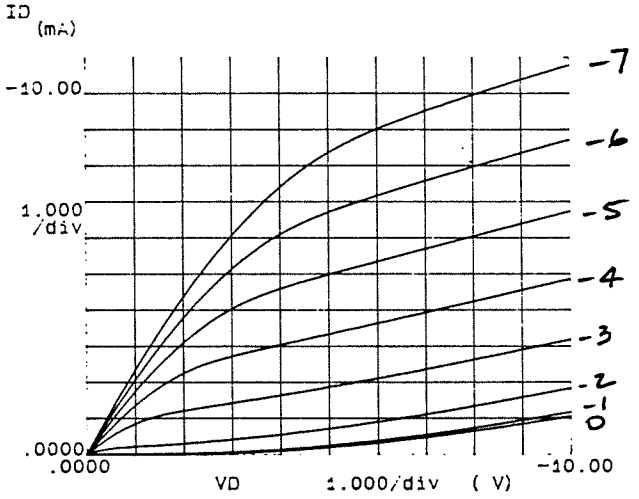

Figure 3: Transistor in circuit.

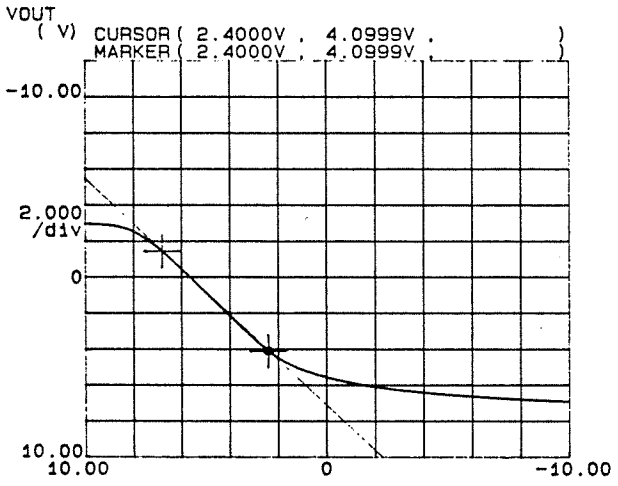

Figure 4: Low gain inverter.

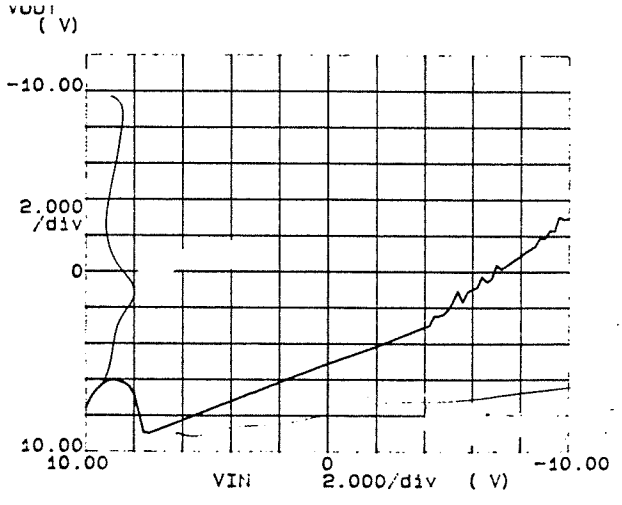

Figure 5: Inverter, gain=40.

Figure 5 is the obtained characteristic curve for the inverter with the gain of 40, M10 and M11. The rising tail of the curve is not fully understood, which could cause the short channel effect as seen before. Neglecting the tail end portion, the maximum and minimum output swings are 6 and 9 volts. The pull up is distorted significantly, 16.0 volts and the pull down is distorted by 1 volt. Figure 6 is another inverter characteristic curve with a gain of 50. Noted that the curve is obtained without the current source, M3. The supply voltages are -10 and 0 volts, which gave the pull up distortion of 7.2 volts. The distortion would be double, 14.5 volts, if the supply voltages are -10 and +10, which is similar to Figure 5, 13.5. A high gain inverter requires a long pull up gate. However, a long channel gate has a relatively high resistance and large voltage drop. Since both inverters, Figures 5 and 6, have long pull up gates, significant voltage distortion at the pull up occured. The measured gains were 5 and 10, Which is much smaller than their designed values. The large distortion limits the maximum pull up decreases the inverter gain significantly.

SPICE simulations show that inverter's gain does not go higher than 25. Inverters with gains of 40 and 50 are saturated at 25 as simulated. SPICE also shows the differential input stage with a transistor as a load at the bottom degrades the stage performances. The stage doesn't converge for lower supply voltage greater than 6 volts. Also, The gain of the stage degrades significantly. Figure 7 is the simulated characteristic curve of the differential input stage with the current source (M3, M4 and M5). Noted that the supply voltages are -10 and 0 volts, the gain of the stage is 2. Figure 8 is another simulation using a resistive load in place of the M3 transistor. The simulation is converge and stage gain is restored, saturated at 25.

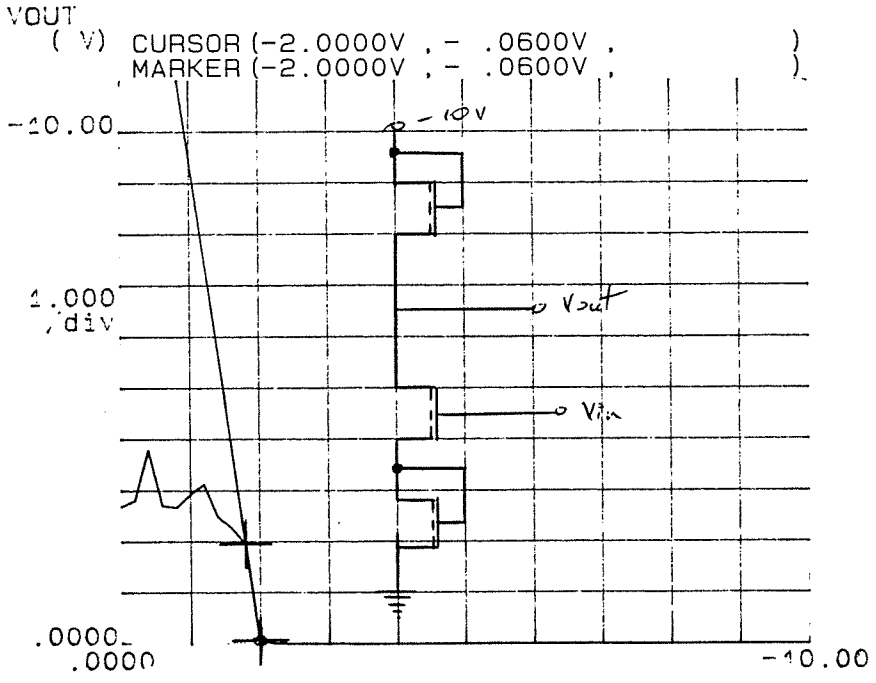

Figure 6: Inverter, gain=50.

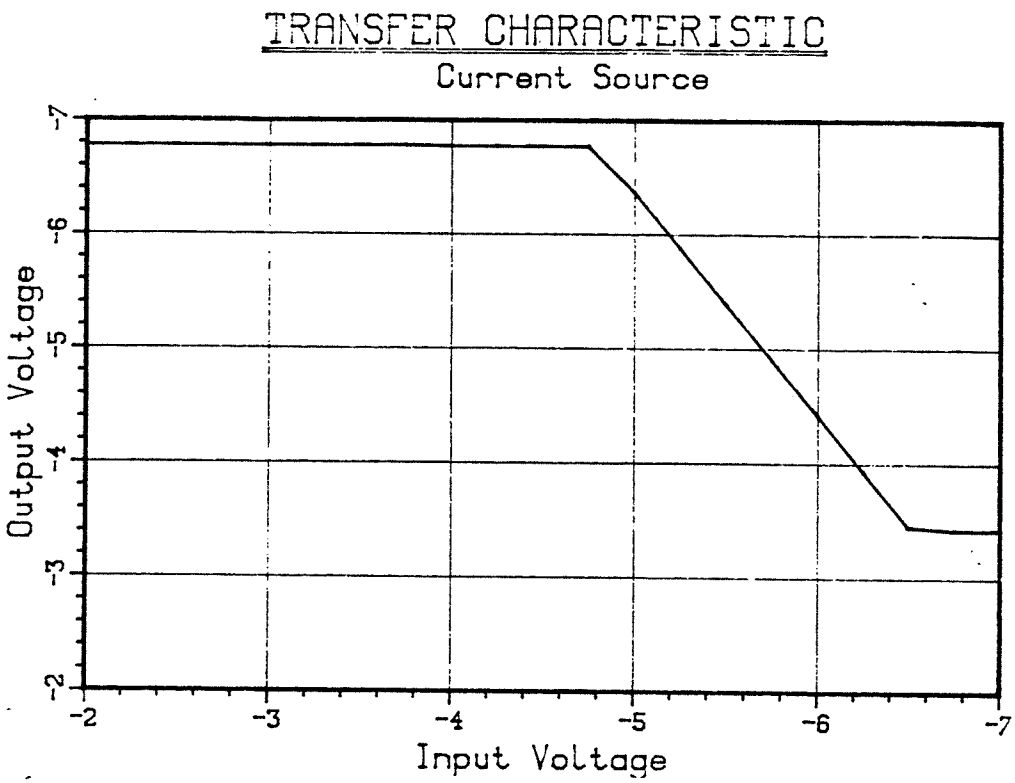

Figure 7: Inverter with current source.

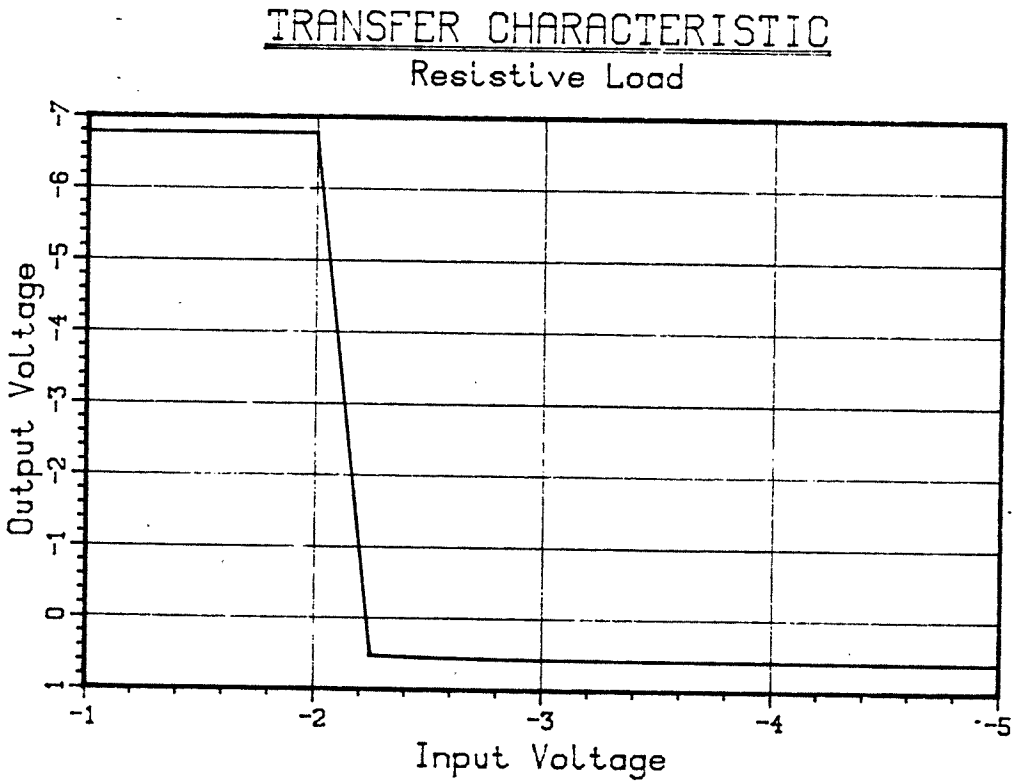

Figure 8: Inverter with resistive load.

CONCLUSION

The distortion voltages degrades performances of the inverter and it becomes more significant for a higher gain inverter. The 1.6 gain inverter has a pull up distortion of 7 volts, which should be 2.5 volts. The pull down is distorted by 1.5 volts, which should be 0. The pull up for inverters with gains of 40 and 50 are distorted by 16 and 14.5 volts. Short channel effect are found in higher dense regions which are not well understood. SPICE simulations show the maximum gain of an inverter is 25 for for this process. Inverters with higher gains are saturated at 25. The simulation also shows that the a transistor load for the current source degrades the stage performances. The stage gain is 2 instead of 50 as designed. The simulation does not converge for the lower supply voltage greater than 6 volts. The stage performs much better using a resistive load as a current source. The gain is saturated at 25 and converge for any supply voltages.

SPICE indicates that inverters with gains higher than 25 are not possible. Also, higher gain inverters introduce more parasitic resistances. Modification of the gain of the stage is needed for a better working device. Reference [4] is a paper on an all-enhancement NMOS op amp which is a good reference for circuit modification.

ACKNOWLEDGMENTS

I like to thank Michael Jackson for his guidance throughout the project and his recommendations. I like to thank Dr. Lynn Fuller for his permission using the circuit that he designed and his comments on the results. I also like to thank Kurt Gerger for his help with the fabrication.

REFERENCES

[1] 650EMCR note, from Microelectronic Engineer Department

[2] K. R. Roberge: "Operational Amplifiers: Theory and Practice", John Wiley and Sons, Inc., New York, 1975.

[3] Ramakant A. Gayakwad: "Op-Amps and Linear Integrated Circuits, Prentice Hall, New Jersey, 1988.

[4] Yannis P. Tsividis: "An Integrated NMOS Operational Amplifier with Internal Compensation", IEEE J. Solid State Circuits, vol. SC-11, Dec. 1976, pp. 748-753