INVESTIGATION OF PROCESS INDUCED DEFECTS USING A LTO PROCESS

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ABSTRACT

The effects of process induced defects, such as dislocations and/or oxide induced stacking faults, were investigated for a bipolar process employing solid diffusion sources. Carborundum BN975 Boron Sources have a low temperature oxide (LTO) step to minimize defects. Two bipolar processes, one with and one without LTO were run and electrical tests done to evaluate device characteristics. At this point results were inconclusive.

INTRODUCTION

Currently the RIT bipolar process for NPN transistors, which uses both boron and phosphorous solid sources, has yielded current gains ranging from 10 to 200 depending on design specifications. Routine optical inspection during a recent processing run displayed defects in the base region. As subsequent high temperature processing was encountered, the defects became more prevalent. During a standard RCA clean, the ammonium hydroxide/hydrogen peroxide bath unknowingly had decomposed to just hot ammonium hydroxide, which selectively etches silicon. Optical microscopy and SEM micrographs were taken of wafers that had been etched in heated ammonium hydroxide [1]. This etch drastically highlighted the defects in the base regions as shown in Figures 1 and 2.

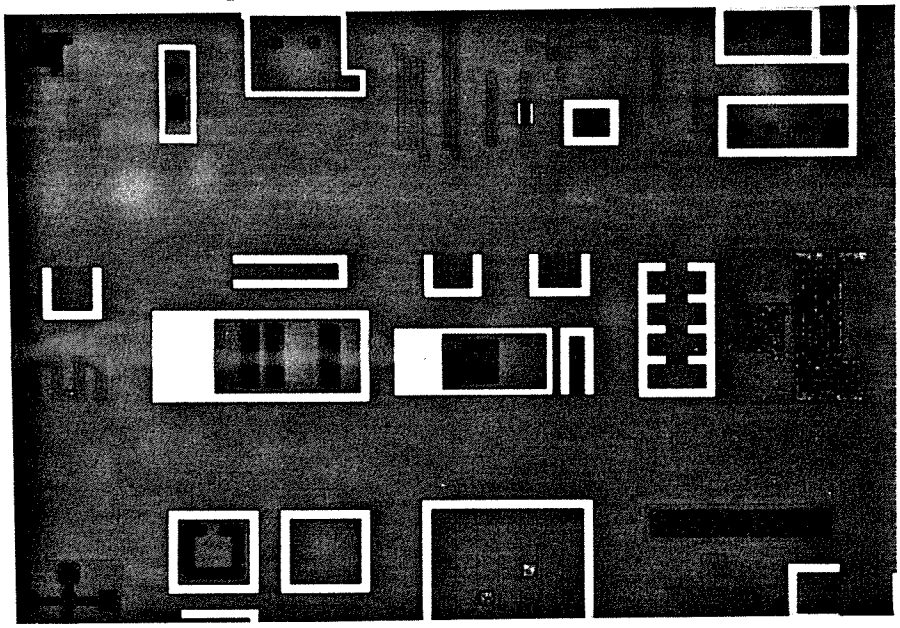

Figure 1: Bright field; blackened areas are base diffusion regions that were exposed to silicon etch.

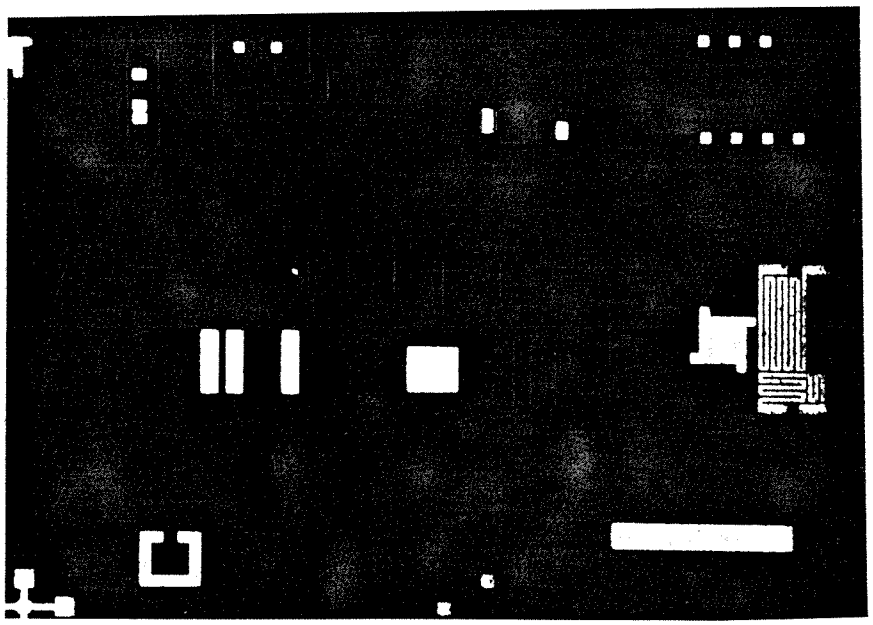

Figure 2: Dark field; lightened areas correspond to blackened regions of Figure 1.

This project was an attempt to characterize this phenomenon and study its effects on device characteristics. It was hypothesized that the defects may result from starting material and/or the solid source boron diffusion for the base. This project focused on the base diffusion and the absence of a low temperature oxide (LTO) step in the process. A LTO process was suggested by the manufacturer of the solid sources, Carborundum Products, for minimizing defects [2]. It was hypothesized from diffusion theory that defects such as dislocations diffuse more rapidly than impurities [3]. Since diffusion is a direct function of temperature these defects would propagate into the substrate before they could be consumed by the growing oxide at high temperatures. The LTO step was used to oxidize the boron-silicon (Si-B) layer and a thin layer of silicon (Si) below it prior to harmful propagation of these defects into the substrate. This oxidation would trap the majority of the crystal defects in the oxide thereby allowing a deglaze to remove them. As a result the subsequent drive cycle would be damage free [2].

In order to determine the optimum time for the LTO cycle an experiment was previously performed [4]. A graph that measured the incremental percent changes in sheet resistance as a function of process run time was constructed. The knee in this curve, see Figure 3, corresponded to the time required to remove the Si-B layer, which lead to the desired LTO time and temperature.

Control wafers were used to monitor sheet resistances and junction depths throughout the process. These in process measurements were compared to SUPREM simulated results. Samples were preferentially etched, at various intervals throughout the process, with a Schimmel Solution, which was to decorate the defects for identification. Completed devices, half subjected to the LTO and half not, were evaluated at electrical test to determine the effects of this damage upon the parameter of the devices, such as junction leakage and current gain.

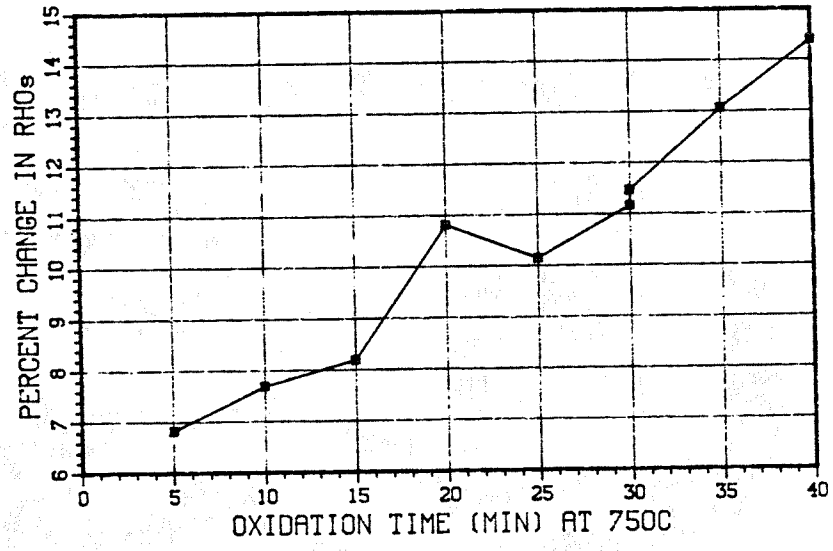

Figure 3: Graph of percent change in sheet resistance versus oxidation time at 750C for BN975 solid sources.

EXPERIMENT

A 3500A masking oxide was grown for 30 minutes at 1100C on n-type (100), 5-15 ohm-cm silicon wafers. Photolithography was performed for the base mask followed by a base predeposition, using BN975 solid sources at 975C for 30 minutes. The lot was split and half of the wafers underwent an LTO cycle of 25 minutes at 750C. Once the Si-B layer was etched, the wafers were recombined for a base drive-in of 1 hour, 30 minutes in nitrogen (N2) and 30 minutes in wet oxygen (O2), at 1050C. This was followed by the emitter mask, an emitter predeposition using PH1025 solid sources at 1000C for 20 minutes, and an emitter drive-in at 1000C for 40 minutes in wet O2. Contact cut photolithography was performed. Aluminum was evaporated and patterned to form discrete transistors, resistors, and test structures. Finally the aluminum was sintered at 450C for 30 minutes.

For preferential etching a 0.75M solution of chromic acid (CrO3) was made. Upon activation hydrofluoric acid (HF) was added to the chromic acid in a 2:1 ratio. This was known as the Schimmel Solution [5]. The specimens were placed in a tray, with the polished surface up, and covered with the etchant. A 5 to 10 minute etch was used depending on the strength of the solution. Then the specimens were rinsed thoroughly and dried in order to be inspected.

RESULTS/DISCUSSION

The Schimmel etch was ineffective in duplicating the highlighting noticed in Figure 1. In fact there was no noticeably difference in the wafers that saw the LTO and those that did not. Not only that but there was little difference in the base, emitter, and collector regions. The time of the etch was increased to 15 and 20 minutes in an attempt to achieve the desired affect. However, it was to no avail. As a result these defects were unable to be identified.

	SUPREM	No LTO	LTO
Base drive-in			
rhos (ohm/sq)	68.5	81.0	89.5
xj (um)	2.2	1.5	1.2
Emitter drive-in			
rhos (ohm/sq)	8.0	6.2	5.4
xje (um)	1.8	1.2	1.5
xjb (um)	4.2	3.3	2.4

TABLE 1: Simulated and measured sheet resistances and junction depths.

From Table 1 the predictions of SUPREM were in general low for sheet resistances and high for junction depths compared to measured values. However, the emitter rhos was slightly higher from SUPREM than from the four point probe measurements. Considering these expected trends when using SUPREM, based on past experience, the theoretical values were in relatively good agreement with experimental values.

The LTO process was shown to lighten the doping in the base since boron is more soluble in oxide than silicon, thereby producing a higher rhos. Due to this higher rhos the base junction was 1.2um with an LTO and 1.5um without, as expected, because there was less dopant in the LTO wafers. As a result a decreased base width was expected in the LTO wafers since the emitter was being diffused into a lighter doped base. From the data the base width for the LTO wafers was 0.9um compared to 2.1um for the wafers without the LTO. Therefore a higher current gain, since a decreased base width reduces the recombination of the minority carriers in the base, was foreseen for the LTO wafers.

At electrical test the wafers that did not see an LTO step were unable to be tested. The collector current (Ic) versus collector to emitter voltage (Vce) graph showed some kind of breakdown at about 6 volts. No family of curves was obtainable. Both diodes the emitter base and collector base seemed to be fine. After many hours of testing no logical conclusion was found to account for the above mentioned phenomenon.

For one LTO wafer current gains of 517 to 755 were measured, see Figure 4. Other LTO wafers showed that the emitter had punched through the base because a straight line was seen on the transistor curve. Due to the narrow base width this problem was a concern. The LTO wafers that had the unusually high betas are most likely very close to punch through and therefore are not reliable devices.

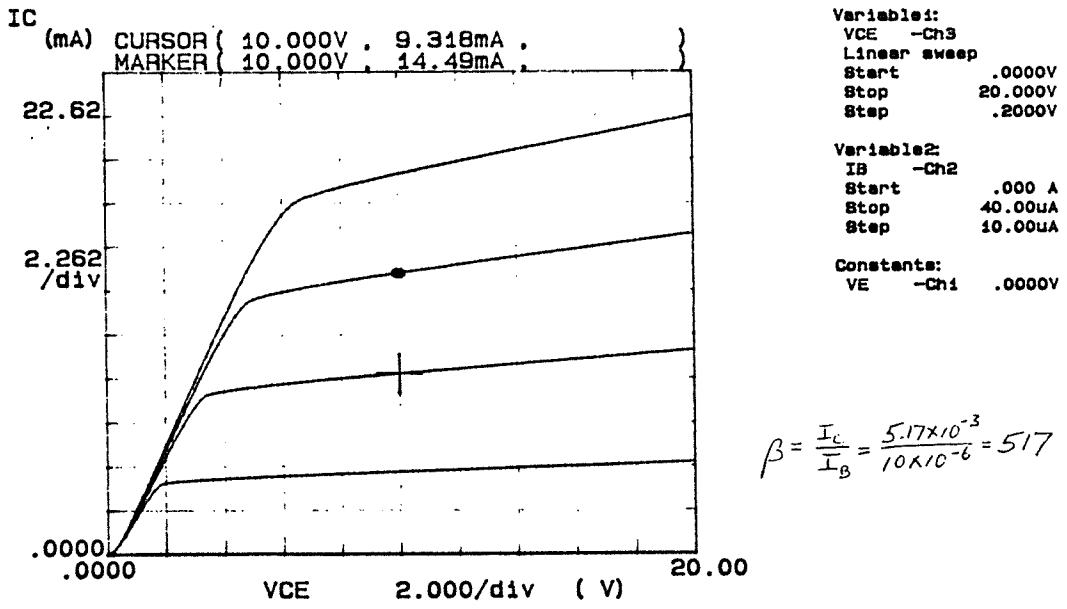

Figure 4: NPN beta for LTO wafer number 5.

CONCLUSION

The LTO process increased the current gain by reducing the base width. The emitter times could be decreased to guard against emitter punch through. It was not exactly clear that LTO process minimized the defects in the base, due to the ineffectiveness of the Schimmel etch. However, this process is recommended since it preserves the uniformity of the base while increasing beta and has been proven to enhance device characteristics in industry.

ACKNOWLEDGMENTS

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REFERENCES

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[4] Experiment performed by Roger Buromiah, Microelectronic Engineering Graduate Student.

[5] ASTM, F47-84 "Crystallographic Perfection of Silicon by Preferential Etch Techniques", 1984.