DESIGN AND CONSTRUCTION OF A STEP ETCHING INSTRUMENT

Robert L. Crandall
5th Year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

An instrument was designed and constructed to perform a sequential etch of an oxidized silicon wafer by periodically lowering the wafer deeper into an etch bath. The unit will step the wafer at four different time intervals 15, 30, 45 and 60 seconds. Either five or ten steps can be done at one time. The unit is primarily designed for the etching of silicon dioxide in a Buffered Oxide Etch.

INTRODUCTION

Step etching of silicon dioxide is an excellent educational method to determine etch rate of the film. Etch rate uniformity, as well as the relative thicknesses of oxide are easily seen. A step etch in general is a sequential etch of a silicon wafer at timed intervals. The result is a wafer with differing thicknesses of oxide across its surface. Because of the lack of a commercial system to accomplish step etches, the author decided to create a system that would step etch.

Operation of a step etcher is relatively simple. A wafer is placed in an acid resistant holder, periodically lowered into an etchant and then returned to the starting position. Three significant steps in this operation were identified. The first is the lowering of the holder to the initial etch position. The second is the timed stepping of the wafer, consecutively moving the wafer deeper into the etchant. The last step is the extraction of the wafer from the etchant. The design of the device addressed these essential steps.

Prior to the design of the step etcher, many factors were considered and decisions made so that the implemented design would be reliable, upgradeable, and utilize practical components which were readily available. These factors kept device structure and operation to a minimum level of complexity.

The first principal decision in the design was the type of logic which would be employed to control the step etcher. Considered were discrete CMOS components and a microcontroller. The microcontroller, although powerful was not adopted because it would introduce much more complexity to the project. With the microcontroller one would have to include EPROMS and possibly RAMS, as well as write software to drive the system. In the event of a design change, the software would have to be re-written and another EPROM created. This would increase

testing time, another limiting factor. Discrete CMOS components were utilized because of their availability, low cost, and their relatively simple method of design change. Seeing no need for high speed operation and because of voltage ranges, the 4000 series CMOS components were chosen. These components are Schotky diode protected on the inputs to prevent ESD damage. Circuit modification is as simple as rewiring and/or adding gates and testing is made easier because all points of the circuit are available for measurement.

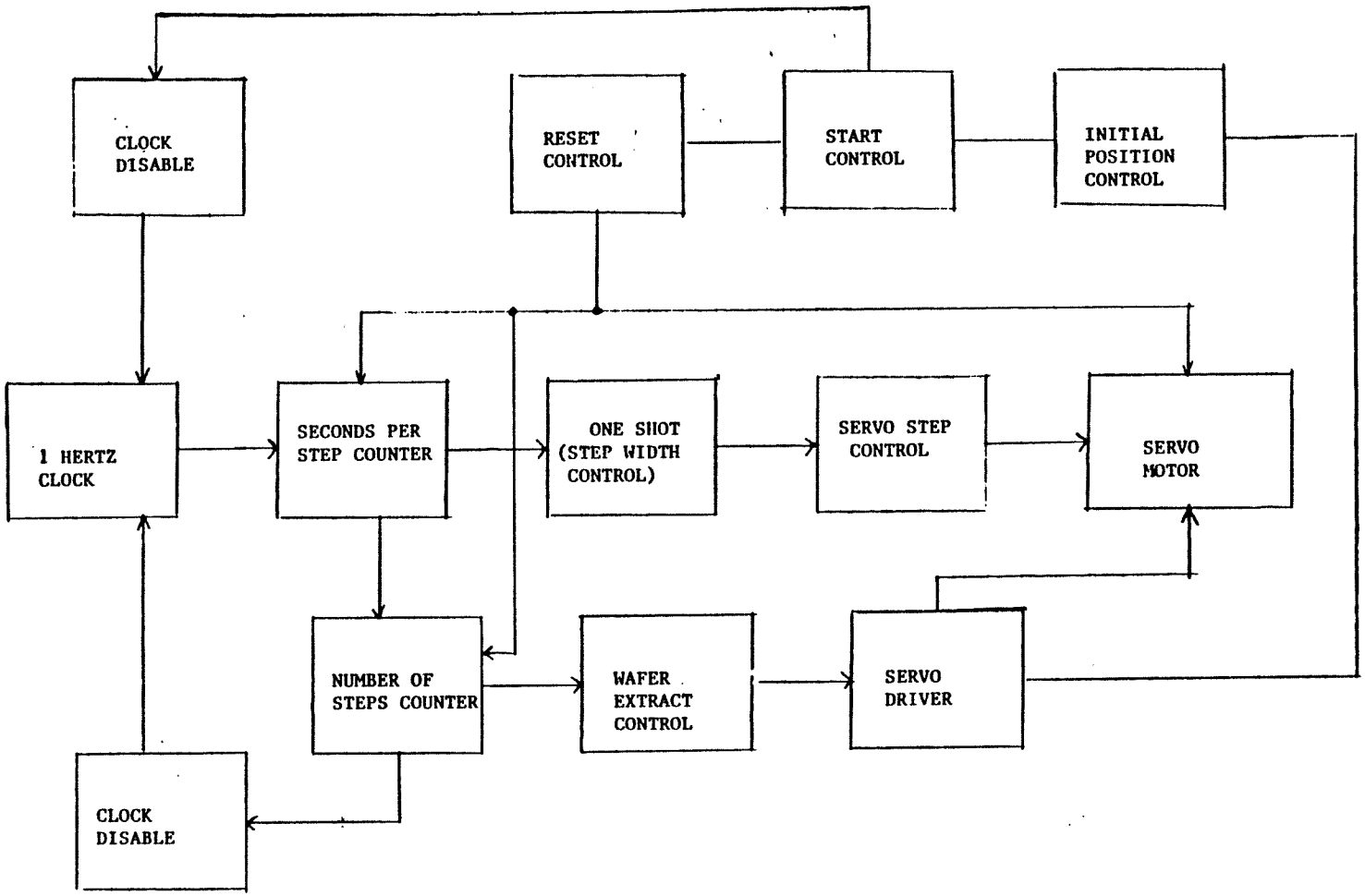
The second design decision was the method of interfacing the digital logic circuitry to the type of servo motor used to drive the system. Considered were DC servo motors and DC stepper motors. Although each would have worked, the DC stepper motor was discarded because of the extra componentry needed to interface the motor to the digital control, their relatively high price, and the torque requirements to drive the etching platform. The linear DC servo chosen worked at a low voltage, had good reversing properties, and had sufficient torque at low rpm's.

Three different, albeit similar methods were used to interface the digital logic to the servo motor. Each method used a mechanical relay at the final stage before the motor. Relays were chosen instead of solid state devices because of the high current requirement of the motor.

CIRCUIT OPERATION

Figure 1 is a block diagram of the circuitry with schematics in Appendix A. The two main sections of the etcher are the seconds per step counter and the number of steps counter. The clock generates pulses that are counted by the seconds per step counter. When the proper number of pulses arrive, the counter enables the one shot timer and servo step control and the wafer lowers into the etchant for the next step. Also at this time, the number of steps counter is clocked and increases by one. At the same time the number of steps counter is clocked, the number of seconds counter is reset to zero by the number of steps conter and the process starts over. When the number of steps counter reaches the final value, the counter enables the extract control. The clock is then disabled so no more steps can occur until the system is reset. Reset control resets all counters and also enables wafer extract control. As long as reset is held, the wafer will continue to extract. Start control starts the process by enabling the initial position control to lower the wafer to the initial position. While start control is operative the clock is disabled. The following section gives a more in depth view of circuit operation.

During the start and finish of the etch, the platform must move large distances for a long time, in different directions. To handle initial positioning, in which the platform moves the wafer down to the initial etch start point, an SCR linked to a relay was utilized. To handle stepping, the digital logic was linked to a 555 timer device so as to be able to adjust step



STEP ETCHING INSTRUMENT BLOCK DIAGRAM

widths. The 555 timer then drives another relay. Finally, at the end of the etch, the wafer must be moved back to starting position. The digital logic drives an NPN transistor, and this transistor drives yet another relay to control current to the servo. Multiple relays are used because the motor needs to see positive and negative voltage.

Figure 2 is a schematic diagram of the digital section of the step etcher. Refer to Figure 2 during the following analysis. IC1 is a NAND gate configured as a clock oscillator. R1 and C1 control the frequency. Frequency can be adjusted using R1 to the specified value of 1 hertz. From IC1 the clock signal is routed through an inverter in IC10. (Note that chips IC2, IC3 and IC7 are 4017 decade counters, all others are 4011 NAND gates) The inverter cleans up the rounded edges that this type of clock produces. From there the clock is routed to IC2, the first half of the seconds per step counter. IC3 is connected to IC2 through the carry line of IC2 in order to achieve a counter with a maximum count of 99 seconds. Times of 15, 30, 45 and 60 seconds were implemented in the final design. The counter pair counts the clock pulses and decodes them on their output lines. The output lines are connected to IC4 and IC5. These chips are connected as AND gates and provide a high output when the proper count (ie. number of seconds) has occurred. Their are four AND gates and thus four different selectable times. (15, 30, 45 and 60 seconds). Note that the counters are rising edge triggered and will only count when their RESET and CLOCK ENABLE lines are logic low. The outputs of the AND gates are connected to S1, the number of seconds per step select switch. It is a 6 position rotary switch with only 4 positions used. S1 routes the logic high signal to IC6 and IC11. IC6 is configured as an AND gate and inverter and it purpose is to inhibit clock signals to IC7 when the final number of steps is reached. IC11 is configured as an inverter and an OR gate and generates the reset pulse to IC2 and IC3 to reset the number of seconds count. IC7 counts the number of steps and decodes them on its 9 output lines. Up to 9 steps are possible and as configured either 5 or 9 steps can be selected utilizing S2, the number of steps select switch. S2 routes the high signal to IC6, the clock cutoff and to IC8. IC8 functions as an OR gate, and its purpose is to provide the active high extract signal, and to also invert the step signal to active low to trigger the step timer. Extract can be high either when all stepping is done or when the reset switch S3 is depressed. IC9 and IC10 are more AND gates that perform a circuit reset to all counters and send a high to the extract IC8 when reset switch S3 is depressed. IC12 is configured as an OR gate and its purpose is to OR the reset line on the seconds per step counter with either the reset line switch or the number of seconds complete from IC2 and IC3. Clock enable to IC2 and IC3 is provided by the analog circuitry discussed next.

The analog circuitry is shown in Figure 3. It is composed of three separate blocks. From top to bottom there is initial position control, step control and extract control. Initial position control includes start switch S4, top of etchant switch

S5, SCR1, and relay K1. When S4 is pressed, current enters the gate of SCR1 through a current limiting resistor and switches it on. Current flows through S5, SCR1 and relay K1. Relay K1 pulls in and positive voltage is applied to the servo motor which moves the platform down. When the platform wafer holder is at the initial position at the etchant S5 opens and breaks current to the relay. The SCR remains off since its gate is no longer positive and the platform remains there. A clock enable signal is generated from this section of the circuit at the connection between the SCR and relay. When the relay is engaged, the voltage is high, inhibiting IC2 and IC3 from clocking. When the relay is disengaged the voltage falls to zero and the counters begin to count.

Step control includes IC13, a 555 timer chip configured as a one shot. IC13 and its associated components make up the timing circuit that is variable and adjusted using R2 to achieve the desired step distance. IC13 drives relay K2 that applies positive voltage to the motor for a short time. Trigger pulses for the 555 must be active low and are introduced through the normally closed bottom limit switch, S6. Stepping cannot take place if this switch is open. Trigger pulsed come from IC8.

The last section of the circuit includes the necessary componentry to extract the wafer and chuck from the etchant bath. It includes Q1, an NPN transistor and its associated componentry. When the extract line comes high from IC8, the transistor saturates and activates relay K3. This relay applies negative voltage to the servo motor and moves the platform up. Switch S7, the top limit switch is a normally closed switch in series with the relay. This disengages the relay when the platform is at its top limit.

The power supplies can be found in Figure 4. For the logic circuitry, transformer T1 along with diodes D1-D4 and filter capacitor C1 form the DC supply. The supply is regulated with a 7812 12 volt regulator providing +12 volts. For the motor, transformer T2, a 9 volt center tapped transformer is used to form a bipolar supply with D5 and D6. D5 and D6 are 50PIV diodes rated for 6 Amps continuous.

PLATFORM DESIGN

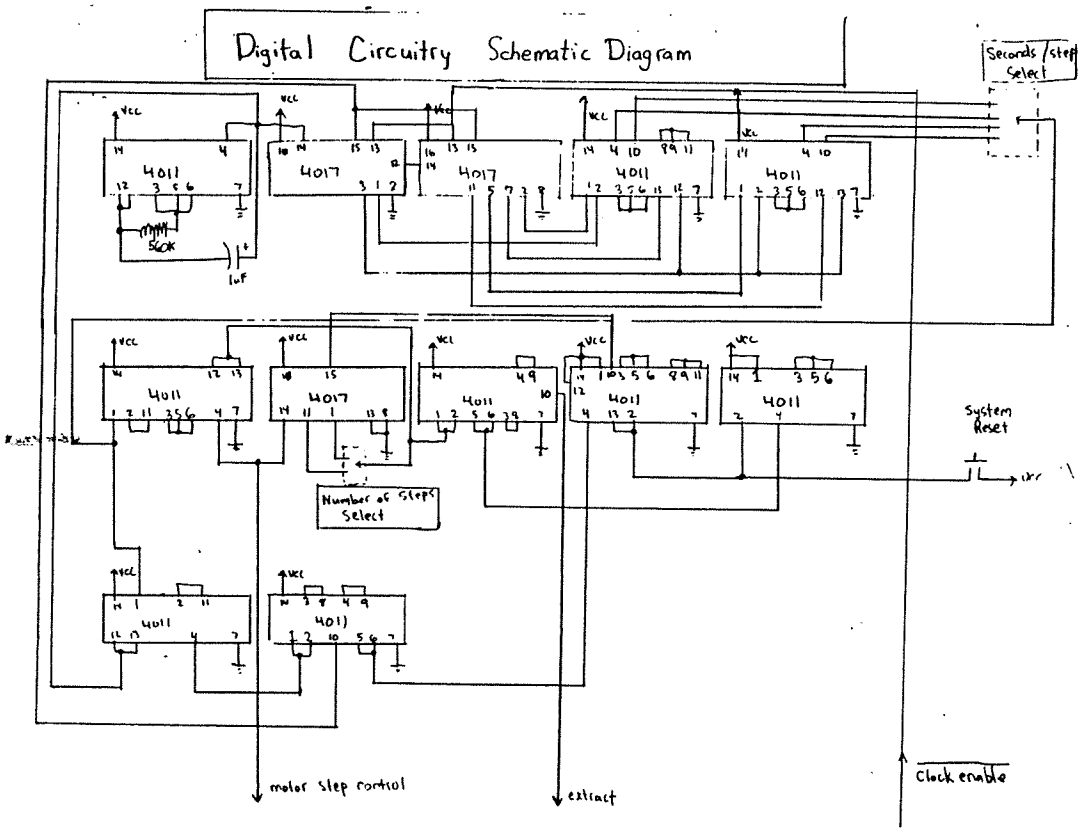
The step etcher platform was designed using 1/2 inch PCV plastic pipe, because the step etcher will be in an area with acid fumes and water. Figure 5 shows a cross section of the main structure. Basically it is a rectangular base with uprights holding up a travelling platform. The traveling platform is a wooden dowel and the wafer holder is simply a four inch wafer holder. The four inch holder will hold both four and three inch wafers. The servo motor sets on top and through a set of reduction gears drives a type of worm gear. The worm gear is actually a threaded steel dowel. The steel dowel was machined by the RIT machine shop to specifications.

SUMMARY

The step etching instrument at this point meets the design goals and is functional. Basically it operates as intended, but still suffers from random timing errors. In particular, the timing pulse that resets the seconds per step counter has problems. Much troubleshooting and work went into getting this to work, but more needs to be done. Improper operation of this section results in inaccurate step timing.

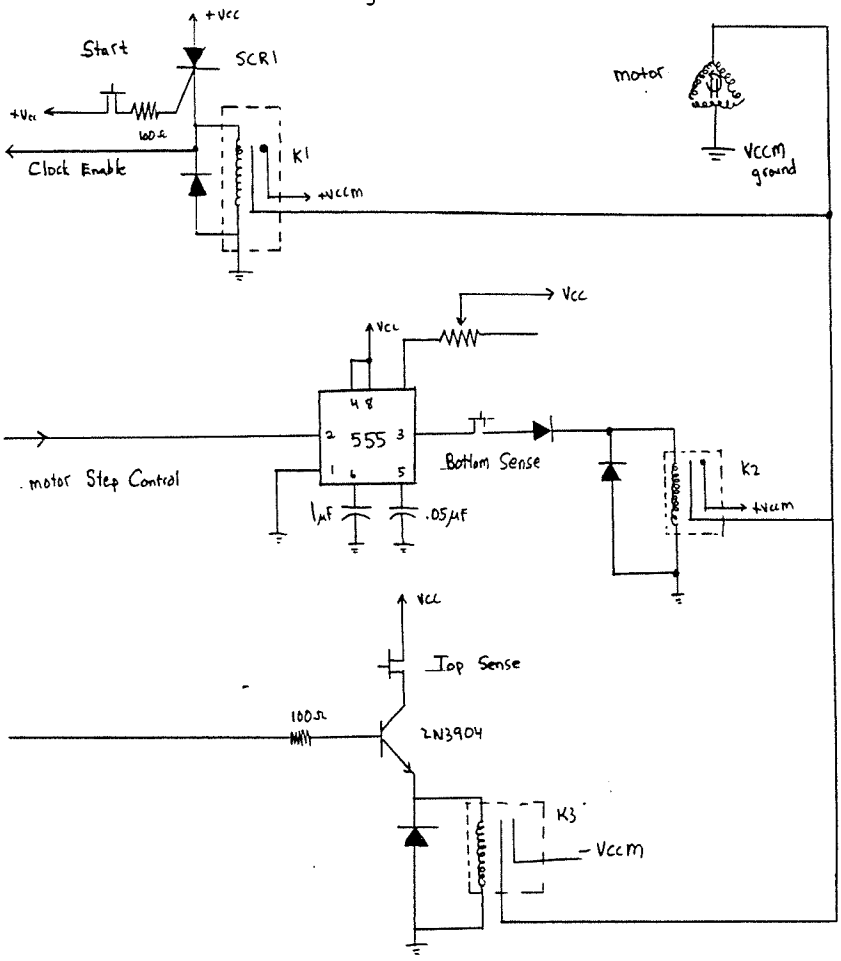
The motor works well, but the steel gear is not perfectly straight because of the work that the machine shop performed on it. As the drive gear turns, the platform tends to vibrate somewhat. A higher quality gear needs to be designed. The gear now is steel, but this will probably tend to rust under the fume hood. Stainless steel would be a good choice for a new gear. Plastic would also work well.

APPENDIX

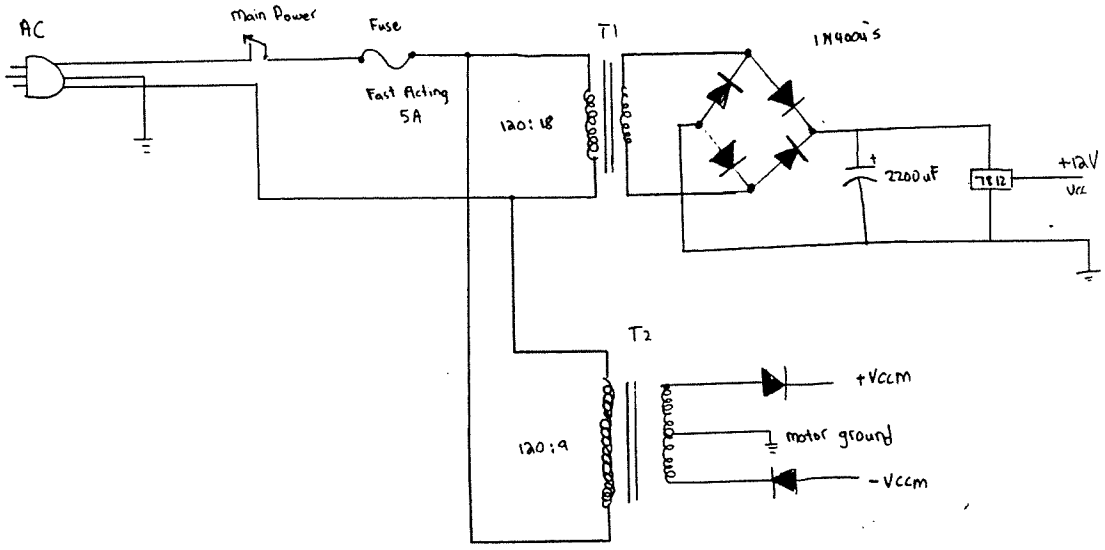


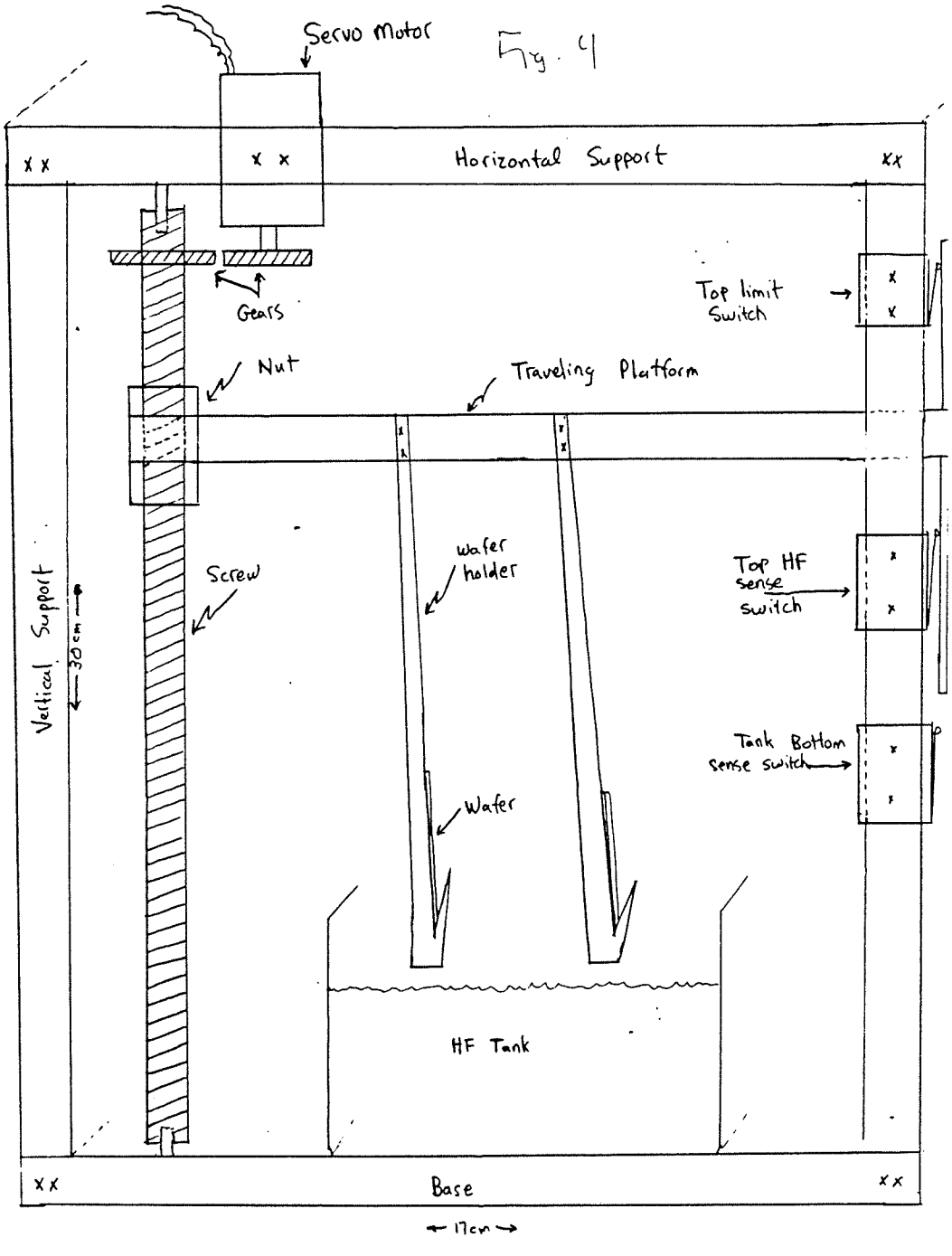
Analog Circuitry Schematic Diagram

Figure



Power Supply Schematic Diagram




Servo Motor
Fig. 4
Horizontal Support
Gears
Top limit Switch
Nut
Traveling Platform
Screw
wafer holder
Top HF sense switch
Vertical Support
30 cm
Tank Bottom sense switch
Wafer
HF Tank
Base
17cm