PROCESSING TECHNIQUES OF MOS CAPACITORS

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ABSTRACT

Variations in both MOS capacitor structure and fabrication process were characterized using 1MHz C-V measurements. This involved processing MOS capacitors with and without backside oxide, and wet etching versus plasma ashing photoresist. The experimental results show large flatband shifts in wafers that were plasma ashed. A longer than expected anneal was utilized to reduce the C-V shifts caused by positive charge build-up in the oxide. The backside oxide did not grossly affect the capacitance measurements.

INTRODUCTION

The MOS capacitor is used in both monitoring integrated circuit processing and studying the electrical properties of the MOS system. It is used because of its simplicity of fabrication and analysis. The understanding of its electrical behavior, and the influence of various processing techniques upon its properties are important to the microelectronic process engineer. Properties, such as oxide thickness, permittivity, fixed oxide charges, interface traps, mobile ion contamination, minority carrier lifetime, flatband voltage shift, and work function differences are obtainable through the C-V testing of a simple MOS capacitor.

A common capacitance measurement is the high frequency (1MHz) C-V plot. Capacitance meters measure capacitance by applying a small ac voltage on top of the dc bias and measures the reactive component of the resulting current. With a negative gate bias, p-type silicon is in accumulation, and one measures the capacitance of a a parallel plate capacitor with the oxide as the dielectric. At a gate voltage that is more positive than the flatband voltage Vfb, a depletion layer is formed in the semiconductor. This creates a capacitor in series with the oxide capacitor and produces a drop in total capacitance. When the dc gate voltage reaches and exceeds the threshold voltage Vt, a layer of inversion charge forms. Then if the dc gate voltage is slowly increased further, the inversion layer increases its charge to balance the gate and the depletion layer does not widen

further. However, since the capacitance measurement employs ac signals, the inversion charge cannot respond to it, thus majority carrier charge changes at the depletion region edges resulting in a constant capacitance. When the depletion-layer width reaches a maximum, the total ac capacitance is at a minimum [1].

To achieve accurate capacitance measurements good ohmic contact must be maintained. If contact is made to the substrate through the back of the wafer, then the back of the wafer should not have any oxide on it. Any oxide introduces a capacitance in series with the device, therefore, reducing all capacitance readings. Furthermore, good ohmic contact is required between the wafer and the test fixture. Therefore, both the capacitor structure and the test setup can affect the quality of the measurement.

Once good capacitor structure and test fixturing is obtained, processing studies can be done. One of the most commonly observed radiation effects in thermal SiO2, as revealed from measurements of the electronic properties of MOS devices, is a build-up of positive charge in the oxide. The amount of radiation-induced positive charge depends strongly on the accumulated total radiation dose absorbed in the SiO2. Exposing MOS devices to high enough incident energy can lead to the generation of electron-hole pairs in SiO2. Many of the electrons and holes recombine, but some are separated apart. Since the electrons have relatively high mobility in the SiO2 conduction band, they diffuse or drift out of the SiO2 very rapidly, leaving behind the excess holes. The holes have orders of magnitude with lower mobility than the electrons. Eventually some of them are trapped in the hole traps, giving rise to radiation-induced positive oxide charge [2].

A high concentration of hole traps can be found to exist near the SiO2-Si interface. The electrons readily pass through the oxide semiconductor interface while the holes are captured by traps. The presence of an electric field in the oxide serve to separate the electron-hole pairs, which in effect reduces the recombination rate and increases the net trapping of holes. This effect is enhanced as the field increases. The polarity of the oxide field influences the spatial distribution of the trapped holes, and results in an asymmetrical field dependence of the C-V shift. This flatband shift observed in the C-V plot can be annealed out at a low (450 C) temperature in a H2N2 atmosphere. Plasma induced radiation can also generate new interface traps and create electron traps near the interface. These will cause distortion and hysteresis in the C-V plot. However, these effects are not as severe a detriment as the trapping of holes [2].

In this project, the capacitor structure was studied to determine the affects of backside oxide on capacitance, and an O2 plasma asher was utilized to study plasma induced damage.

EXPERIMENT

Four p-type, {100}, 5-8 ohm-cm wafers were four point probed and scriber W1-W4. The wafers were then high pressure scrubbed and RCA cleaned to remove any surface contaminants, native oxide, and organic particles. A Trichloroethane clean was performed on the furnace tube prior to an oxide growth. The gate oxide was grown on all the wafers at 1100 C for 15 minutes in a dry O2 furnace. A 10 minute N2 oxide anneal followed.

Aluminum was evaporated on the front sides of the wafers and the gates with areas of 2.3E-4, 6.3E-4, 1.2E-3, and 2.6E-3 inches squared were patterned. A thick layer of photoresist was then spin coated over the front surfaces of all the wafers to protect the gate regions. This allowed for the backside oxide of W1 and W2 to be etched off using buffered HF. A back contact of aluminum was evaporated on the backsides of all the wafers. The photoresist was stripped on W1 and W3 using the plasma asher and on wafers W2 and W4 using acetone. All the wafers were then sintered at 425 C for 15 minutes in forming gas (10% H2/90% N2).

The capacitors were high frequency (1 MHz) tested on the model 410 C-V plotter with zero bias/room temperature conditions and a voltage range from -10 volts to +10 volts. After reviewing the results of the wafers that were processed utilizing a plasma, an additional sinter at 450 C for 15 minutes was performed on these wafers.

RESULTS/DISCUSSION

The C-V plots for the same size capacitor (.025" x .025") on each of the wafers that were processed differently are shown in Figure 1 (a-e).

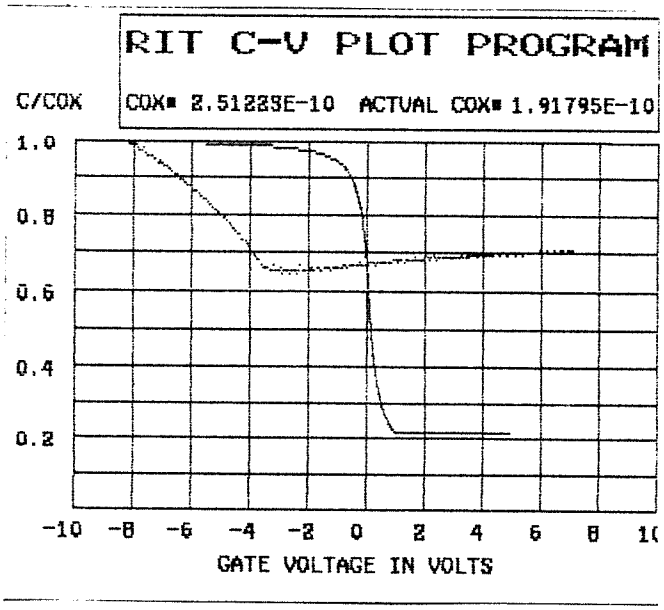

Figure 1a: wafer 1

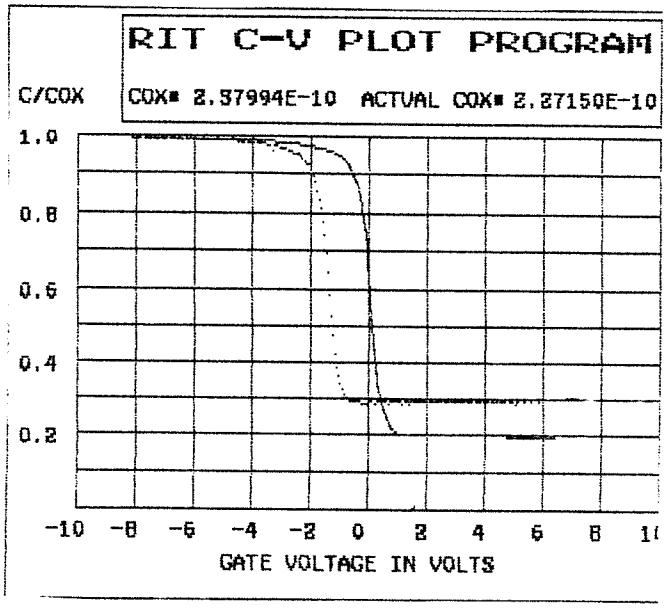

Figure 1b: wafer 2

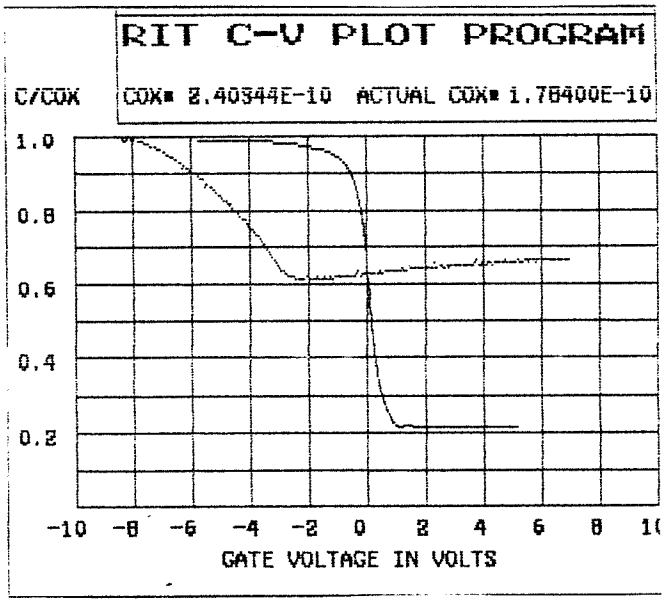

Figure 1c: wafer 3

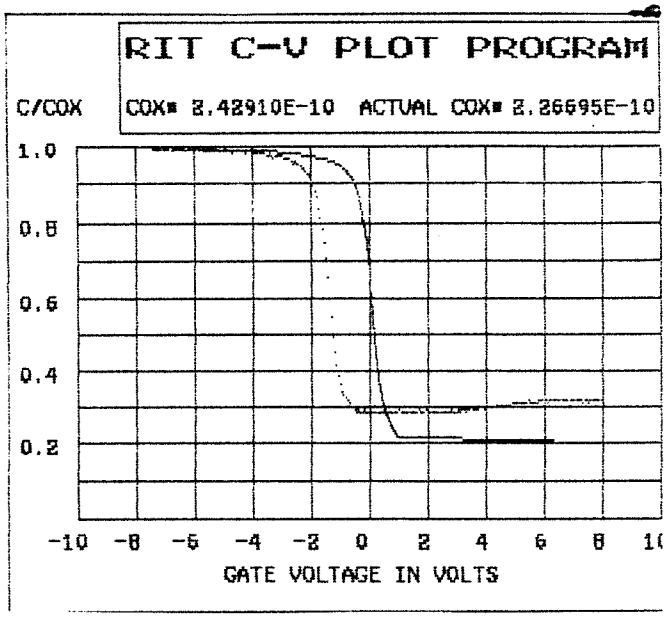

Figure 1d: wafer 4

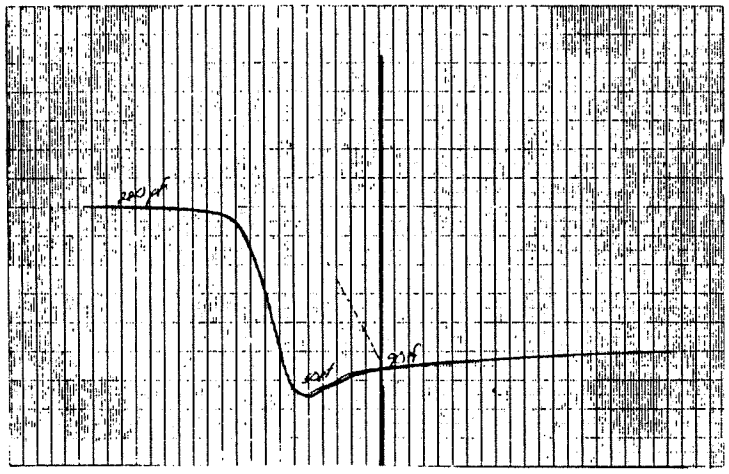

Figure 1e: wafer3
Annealed longer to reduce Vfb

From the C-V plots it is obvious from large flatband shifts that severe damage was caused due to the use of a plasma asher as a means for stripping away photoresist. The damage can be attributed to a build-up of radiation induced positive charge in the oxide. The positive charge build-up in the oxide gives rise to a negative shift in threshold voltage. Large differences in Cox values are witnessed in the plasma damaged wafers. Due to the unexpected severity of the plasma induced damage, the wafers that were processed with a plasma were further annealed at 450 C for 15 more minutes. The results showed a remarkable decrease in the amount of a flatband shift.

A comparison of C-V plots and parameters between capacitors with and without backside oxide were very similar in nature. The similarity in capacitance values reveals very little difference, therefore, the backside oxide did not prove to reduce the capacitance measurements. This can be attributed to the wafer being much larger in area as compared to the area of the capacitor in question. However, conductance measurements and or low frequency measurements may show effects of backside oxide.

SUMMARY

It was shown that a longer (30 minutes) than expected (15 minutes) anneal was effective in decreasing the plasma induced charge build-up in the oxide, therefore, reducing the shift in flatband voltage. The capacitance values were similar when comparing capacitors with and without backside oxide. To improve on this project in the future, one must utilize the plasma asher without inducing the amount of damage seen in this experiment. This may be done by varying the power used during plasma ashing. Another area that must be improved is the confidence in the data obtained from the C-V test system. Through calibration one must reduce the parasitics in the C-V test system to limit the variations in measurements from one test system to another.

ACKNOWLEDGMENTS

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REFERENCES

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[2] Howard R. Huff, Rudolph J. Kriegler, Semiconductor Silicon 1981, p