ION IMPLANTATION TO ADJUST NMOS THRESHOLD VOLTAGES

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ABSTRACT

NMOS processes require a variety of threshold voltages for differing applications. For this experiment, the threshold voltages of NMOS devices were altered by a using several different ion implant doses (none, 1, 2, 4, and 8e12/cm2) of boron. This shifted the threshold voltage in good agreement with literature values [1].

INTRODUCTION

One of the most important applications of ion implantation in MOS technology is the control of threshold voltages within the devices. By implanting a specific quantity of B atoms in the channels of an NMOS device will bring the threshold voltage to a more positive value. This change is in proportion to the amount of atoms implanted into the channel over the gate oxide capacitance per unit area [1].

Ion implantations are used to control the threshold voltage (Vt) of MOS devices, since they have the advantage of being able to introduce a precisely controlled amount of dopant material into the substrate. Implants can also be performed at lower temperatures, and can be masked with a wider range of materials than diffusions. Lattice damage may occur during an implant, as well as the fact that not all of the implanted atoms may be electrically active [1]. However, under the conditions where an amorphous layer is not formed, temperatures as high as 1000C are needed to anneal the crystal damage, and activate the implanted ions. Typical anneal times are on the order of thirty minutes, and result in virtually all of the species becoming electrically active [2,3].

NMOS devices have gained in popularity as their threshold voltages are typically half of that for the p-channel devices [4]. The smaller threshold voltage is benifical for several reasons; 1.) it allows for the use of smaller power-supply, and hence less power, 2.) it becomes compatible in operation with bipolar devices, and 3.) it makes room for a higher packing density [5].

To lower the threshold voltage, several methods can be used. The use of the crystal orientation <100> will yield a lower Vt (up to one third of <111> orientated silicon), but it will also cut down on the mobility of the holes. The addition of silicon

nitride (Si3N4) to the silicon (SiO2) dielectric layer will increase the dielectric constant, thereby lowering |Vt|. A silicon gate, polysilicon doped with phosphorus to be conductive, will have a lower work function difference with the oxide, than the metal (aluminum), lowering the threshold voltage. Ion implantation can also be used to fabricate both enhancement and depletion mode devices on the same wafer [5]. For this final reason the effects of ion implantation were chosen for study.

The onset of inversion exists when enough gate voltage is applied to bend the band edge to a point where p-type (n-type) material in bulk becomes equally n-type (p-type) at the surface. The inversion layer is formed when the gate voltage exceeds the threshold voltage [2]. The gate of the capacitor being the top (aluminum), deposited atop a SiO2 dielectric, with the bottom plate being the silicon substrate (doped p+).

A MOS device is considered to be in the depletion mode if it is on with the gate voltage equal to zero, and in the enhancement mode if it is off with a gate voltage equal to zero. NMOS devices are ideally enhancement mode devices, but nonidealities tend to shift the threshold voltage toward the negative. Until about 1977, PMOS technology was dominant due to the fact that NMOS transistors were typically of the depletion mode type [6]. For this reason, an experiment was designed to involve a preliminary investigation into threshold voltage adjustments performed with an ion implanter.

EXPERIMENT

Since a variety of threshold voltages may be required for various devices, a process for which differing threshold voltages could be obtained was designed. Several different implant doses (none, 1,2,4, and 8e12/cm2) were performed to examine the shift of the threshold voltage due to these doses. As the metal gate process is now in use at R.I.T., that is what was used for this experiment.

First a mask of several differing size capacitors was designed on 'ICE',an in house CAD tool, and the mask was fabricated through reversal processing of the retical. The capacitor sizes ranged from squares of 10x10 microns square, 400x400 microns square. Other shapes, both rectangles and hallow squares were designed, but overall differing shapes did not affect the threshold voltage.

Ten p-type wafers of <100> orientation were obtained, and scribed with numbers one through ten. The average resistivity of these wafers was 5.50 ohm-cm. The wafers were then cleaned with a standard RCA clean (fifteen minutes in NH4OH/H2O2/H2O (1:1:5), two minute rinse, two minute HF/H2O (10:1), two minute rinse, fifteen minutes in HCl/H2O2/H2O (1:1:5), and a final five minute rinse).

A blanket boron implant was then performed at 60KeV for the following:

wafers 1,2 -- no implant
wafers 3,4 -- implant 1e12/square cm.
wafers 5,6 -- implant 2e12/square cm.
wafers 7,8 -- implant 4e12/square cm.
wafers 9,10 -- implant 8e12/square cm.

After this a thin gate oxide was grown at 1000C for forty minutes. This resulted in an oxide thickness of approximately 470 angstroms, and was also long enough to anneal out damage as well as to make the boron electrically active [2-3].

Aluminum was then evaporated on the frontside of the wafers and patterned with KTI820 photoresist. The photoresist having been spun on with the wafertrac, exposed with a Kasper aligner, and developed with the wafertrac also. The aluminum was the patterned with aluminum etch, and rinsed. Then the photoresist was stripped of with the plasma asher in an oxygen ambient. Aluminum was then evaporated on the backside of the wafers to produce an extremely large capacitor in parallel with the much smaller frontside capacitors, to make the stray capacitance negligible. The odd numbered wafers were then sintered in a forming gas ambient for twenty-five minutes at 450C. Finally, the capacitors were tested with capacitance-voltage measurements.

RESULTS/ANALYSIS

Capacitance-voltage graphs were taken of all the wafers to determine the actual threshold voltages of the implanted doses. The plots were taken from the 400x400 micron squared capacitor, as it gave the most repeatable results. Figure 1 shows a plot of a capacitor which was not adjusted by implant or sintering after metal deposition. It shows a threshold voltage (marked Vt) of magnitude 0.89V.

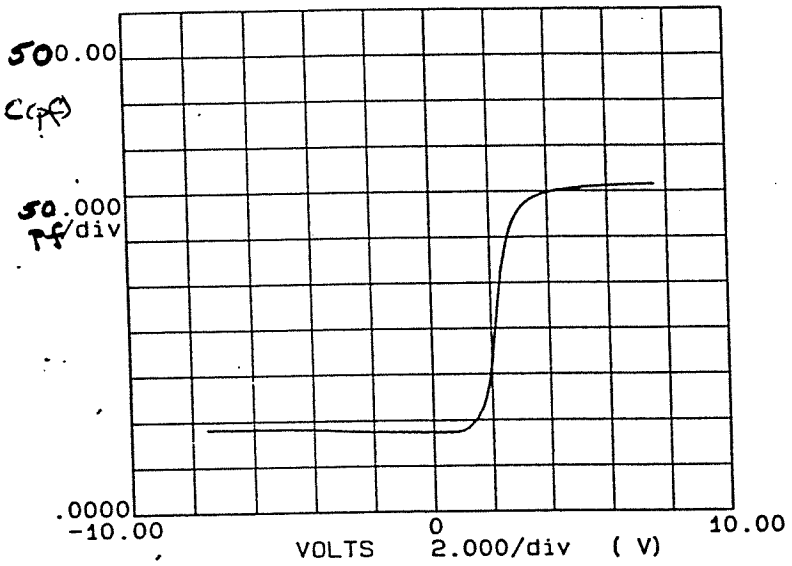

Figure 1: Capacitance vs. Voltage (no implant or sintering)

The positive accumulation voltage implies an n-type substrate, which was not the actual case since p-type substrates were used. This can be explained by the fact that the ramp voltage was applied to the substrate, and not the gate, during the capacitance-voltage measurement, which will invert the voltage.

Figure 2 shows a plot of a capacitor which received a dose of 4e12/square cm., and was not sintered after metal deposition. It shows that the magnitude of the threshold voltage has shifted to 1.85V, however the accumulation voltage had the same problem encountered in Figure 1.

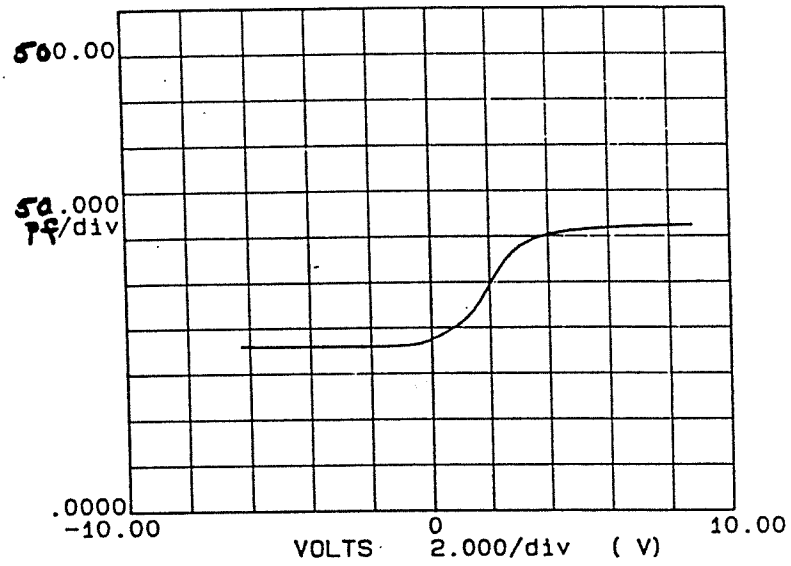

Figure 2: Capacitance vs. Voltage (4e12/cm2 dose, no sinter)

It is also noticed that the values for the maximum capacitance decrease with the increasing dose, assymtotically approaches 250 pf, and the value of the minimum capacitance increases with increasing dose, approaching about 200 pf.

These changing values of capacitance are due to the higher mobility in the substrate, the fact that there are more mobile species in the substrate. At a high enough implant dose, the capacitor would break down completely, and be of no use, as the capacitance-voltage plot would become a straight line.

Figure 3 shows a plot of threshold voltage magnitude versus implant dose for the values used. It can be seen from this graph that sintering the wafers after metal deposition to tie up the loose bonds between the metal and the oxide had little effect on the overall adjustment. Sintered capacitors had a slightly higher threshold voltage, but not appreciable.

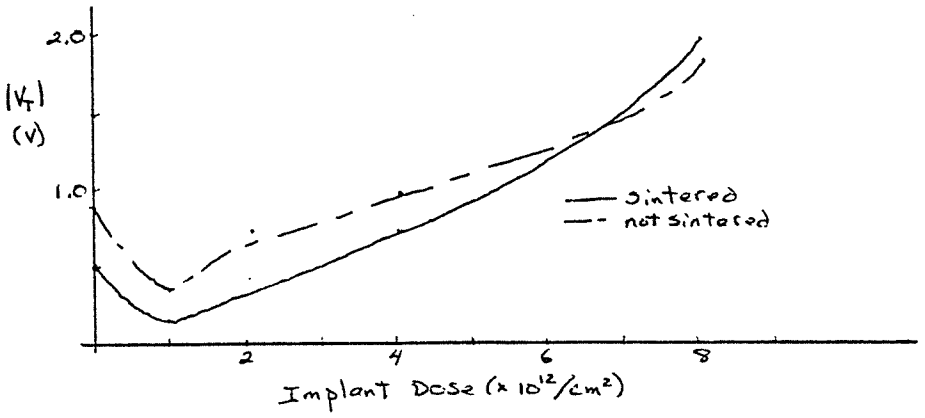

Figure 3: Threshold Voltage Magnitude vs. Implant Dose

CONCLUSIONS

It is now possible to predict the threshold voltage shift for various implant doses at 60KeV. This is of much use as threshold voltages will be important in the upcoming CMOS and NMOS projects. The oxide quality, and processing cleanliness of the NMOS/CMOS processes will also be evaluated through the comparison of past and future results.

The lowest dose implant preformed was 1e12/square cm. This was due to the fact that the implanter beam current was to high to accomplish any lower doses. It may be of use to study lower implant doses, as well as different implant energies and their effect on the threshold voltage shifting. More experimentation needs to be done to gain more insight into this process at R.I.T.

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