Cryogenic Operation of sCMOS Image Sensors

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Cryogenic Operation of sCMOS Image Sensors

by

Benjamin P. Stewart

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

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Dedication

To my girlfriend Audrey, for her endless encouragement and passion for space.

To my family: Jeanne, Cliff, and Abby. Without their love and support
none of my success would be possible.
Declaration

I hereby declare that except where specific reference is made to the work of others, that all content of this graduate thesis is original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This graduate project is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

Benjamin P. Stewart

July 2018
Acknowledgements

This thesis would not have been possible without the guidance and support of the CSTARS principal investigator, Dr. Michael Zemcov, and my thesis advisor, Dr. Patru. Also deserving of recognition are the past and present members of the CSTARS research team, whose combined efforts these past two years have been the foundation for this thesis. Finally, I’d like to thank the members of the CIBER-2 project who assisted with integration, specifically Chi Nguyen and Phil Korngut, and the staff at the Wallops Flight Facility.

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Abstract

Scientific CMOS image sensors have lower read noise and dark current than charge coupled devices. They are also uniquely qualified for operation at cryogenic temperatures due to their MOSFET pixel architecture. This paper follows the design of a cryogenic imaging system to be used as a star tracking rocket attitude regulation system. The detector was proven to retain almost all its sensitivity at cryogenic temperatures with acceptably low read noise. Once the star tracker successfully maintains rocket attitude during the flight of the CIBER-2 experiment, the technology readiness level of scientific CMOS detectors will advance enough that they could see potential applications in deep space imaging experiments.

*Keywords*— sCMOS, CCD, Star Tracker, Cryogenic, Deep Space, Rocket Attitude
# Table of Contents

- Dedication ........................................................................................................... ii
- Declaration .......................................................................................................... iii
- Acknowledgements ............................................................................................... iv
- Abstract ............................................................................................................... v
- Table of Contents ................................................................................................. vi
- List of Figures ....................................................................................................... x
- List of Tables ....................................................................................................... xii
- Glossary ............................................................................................................... xiii

## Chapter 1: Introduction ...................................................................................... 1

## Chapter 2: Background ....................................................................................... 4
  2.1 Extreme Temperature Electronics ................................................................. 4
  2.2 Photodiode Theory ......................................................................................... 5
  2.3 Noise Sources ............................................................................................... 7
  2.4 Star Tracking Systems .................................................................................. 9
  2.5 Related Work ................................................................................................. 10
  2.6 CIBER-1 / CIBER-2 History ......................................................................... 10
  2.7 CSTARS History ......................................................................................... 12

## Chapter 3: Design and Simulation ...................................................................... 14
  3.1 CSTARS-2 Star Tracker System Overview .................................................... 14
  3.2 System Requirements ................................................................................... 15
  3.3 Image Sensor Selection .................................................................................. 19
  3.4 Processor Selection ....................................................................................... 25
  3.5 Hardware Development .................................................................................. 26
    3.5.1 Focal Plane Board .................................................................................. 26
A1.2.1: CSTARS2 Focal Plane Board Hardware Documentation ............ 72
A1.2.2: CSTARS2 Interface Board Revision B Schematic Page 2 ............ 73
A1.2.3: CSTARS2 Interface Board Revision B Schematic Page 3 ............ 74
A1.2.4: CSTARS2 Interface Board Revision B Schematic Page 4 ............ 74
A1.2.5: CSTARS2 Interface Board Revision B Schematic Page 5 ............ 75
A1.2.6: CSTARS2 Interface Board Revision B Schematic Page 6 ............ 76
A1.2.7: CSTARS2 Interface Board Revision B Schematic Page 7 ............ 78
A1.2.8: CSTARS2 Interface Board Revision B Schematic Page 8 ............ 79
A1.2.9: CSTARS2 Interface Board Revision B PCB Mechanical Drawing 80
A1.2.10: CSTARS2 Interface Board Revision B PCB Top Layer ............ 81
A1.2.11: CSTARS2 Interface Board Revision B PCB Ground Layer ....... 81
A1.2.12: CSTARS2 Interface Board Revision B PCB Power Layer ......... 82
A1.2.13: CSTARS2 Interface Board Revision B PCB Bottom Layout ....... 84

Appendix A2: Firmware Documentation .......................................................... 85
A2.1: CSTARS-2 Detector Calibration Code Main.c ........................................... 86
A2.2: CSTARS-2 Detector Calibration Block Diagram........................................ 89
A2.3: CIS2521 Detector Simulation Block Diagram.......................................... 90
A2.4: CIS2521 Detector Simulation Waveform................................................ 91
A2.5: CIS2521 Controller IP ........................................................................... 92
   A2.5.1 CIS2521F Controller Block Diagram Module....................................... 92
   A2.5.2 CIS2521F Controller State Machine Verilog Code ............................... 92
A2.6: CIS2521F Axi Stream Controller IP

A2.6.1: CIS2521F Axi Stream Controller Block Diagram Module

A2.6.2: CIS2521F Axi Stream Controller Verilog Code

Appendix A3: Software Documentation

A3.1 MATLAB Code for Displaying Captured Images
List of Figures

Figure 1: CIS2521F Scientific CMOS Image Sensor ................................................. 1
Figure 2: 3-Transistor (left) and 4-Transistor (right) active pixel sensors [1] ............... 6
Figure 3: Noise Sources in CMOS Image Sensor Measurement Path [8] ...................... 7
Figure 4: Thermal Deflection of Rocket Skin in CIBER-1 Experiment [20] ................. 11
Figure 5: Cryogenic Testing of CSTARS-1 Detector (Left), .................................. 12
Figure 6: Block Diagram of CSTARS-2 System .................................................. 14
Figure 7: CIBER-2 3D Model [20] .................................................................. 15
Figure 8: 5T Photodiode Architecture [24] ....................................................... 21
Figure 9: Rolling Shutter Operation of CIS2521 ..................................................... 22
Figure 10: Global Shutter Operation of CIS2521 ................................................... 22
Figure 11: CIS2521 Dual Column Amplifiers [26] .............................................. 23
Figure 12: CIS2521 Pixel Layout, Including Inactive Pixels [24] ............................. 24
Figure 13: Focal Plane Board PCB 3D Model ..................................................... 27
Figure 14: CSTARS-2 Interface Electronics Board 3D Model ............................. 29
Figure 15: Microchip MCP1825S Linear Regulator with TO220 Package [33] ......... 32
Figure 16: Early prototype of rear-mounted heatsink on interface electronics board ..... 32
Figure 17: CSTARS-2 Warm Electronics Mounted in Rocket Skin [20] .................. 33
Figure 18: CSTARS-2 Data Pipeline .................................................................. 37
Figure 19: Simulated AXI-Stream of Detector Readout ...................................... 40
Figure 20: Synchronous Stream Simulation ....................................................... 40
Figure 21: Block Diagram of CIS2521 Calibration Mode Code ............................ 41
Figure 22: Focal Plane Assembly mounted to cryostat (Left) and ......................... 43
Figure 23: Enclosed Cryostat Aligned with Collimator ......................................... 43
Figure 24: Baseline CIS2521 Image Captured at 300K using RS mode ....................... 44
Figure 25: CIS2521 Rolling Shutter Image Captured using RIT Cryostat .................. 45
Figure 26: CIS2521 Global Shutter Image Captured using RIT Cryostat ................. 46
Figure 27: Detector Temperature Rise due to Self-Heating, Plotted Over Time .......... 46
Figure 28: CIBER-2 Telescope with CSTARS-2 Focal Plane Assembly Installed (Circled in Yellow) ........................................................................................................ 48
Figure 29: CIBER-2 Telescope Aligned with Collimator ........................................ 48
Figure 30: Focused Collimator Image Captured at Caltech using CSTARS-2 System... 49
Figure 31: Average Detector Readout v. Temperature, Rolling Shutter ..................... 52
Figure 32: Detector Readout Image Examples, with Increasing Temperature from Left to Right........................................................................................................ 52
Figure 33: Detector Read Noise v. Temperature, Global Shutter Operation within RIT Cryostat .......................................................................................................... 53
Figure 34: Detector Readout Noise Image Examples, with Increasing Temperature from Left to Right ................................................................. 53
Figure 35: Average Detector Readout v. Temperature, Rolling Shutter .................... 54
Figure 36: Detector Readout Image Examples, with Increasing Temperature from Left to Right ................................................................. 55
Figure 37: Detector Read Noise v. Temperature, Rolling Shutter Operation within CIBER-2 Experiment ...................................................................................... 56
Figure 38: Detector Readout Noise Image Examples, with Increasing Temperature from Left to Right ...................................................................................... 56
List of Tables

Table 1: CIBER-2 Experiment Requirements ................................................................. 16
Table 2: Asynchronous ACS Interface Parameters ......................................................... 18
Table 3: Asynchronous ACS Interface Message Format .................................................... 18
Table 4: CIS2521 Specifications [23] ............................................................................. 20
Table 5: MicroZed Features [28] ................................................................................... 26
Table 6: Interface Board Power Consumption Estimate .................................................... 30
Table 7: Interface Board Power Consumption with Linear Regulators ......................... 31
Table 8: Interface Board Power Dissipation Estimate ....................................................... 31
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCD</td>
<td>Charge-Coupled Device</td>
</tr>
<tr>
<td>CIS</td>
<td>CMOS Image Sensor</td>
</tr>
<tr>
<td>sCMOS</td>
<td>Scientific CMOS</td>
</tr>
<tr>
<td>PPD</td>
<td>Pinned Photodiode</td>
</tr>
<tr>
<td>FPN</td>
<td>Fixed Pattern Noise</td>
</tr>
<tr>
<td>APS</td>
<td>Active Pixel Sensor</td>
</tr>
<tr>
<td>CIBER</td>
<td>Cosmic Infrared Background Experiment</td>
</tr>
<tr>
<td>CSTARS</td>
<td>Cryogenic Star Tracking Attitude Regulation System</td>
</tr>
<tr>
<td>ACS</td>
<td>Attitude Control System</td>
</tr>
<tr>
<td>SoM</td>
<td>System on Module</td>
</tr>
<tr>
<td>SoC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>LVDS</td>
<td>Low Voltage Differential Signal</td>
</tr>
</tbody>
</table>
Chapter 1:  Introduction

Astronomical experiments demand the cutting edge of image sensor technology. Higher resolution and quantum efficiency, with lower noise and dark current, are just a few of the characteristics that modern image sensors strive for. Most image sensors are one of two architectures: the charge coupled device (CCD) or the CMOS image sensor (CIS).

CCDs transfer charge between the individual pixels to perform serial readouts within a row or column of the sensor. One distinct advantage to this approach is the minimal transistor overhead required to perform pixel readout, which made it the most popular architecture at larger technology sizes. The lack of amplification within the charge shuttling process make CCD architectures less susceptible to temporal noise and pixel to pixel variation. CMOS photodetectors, however, implement a transistor-based readout system to individually index through the array of pixels [1]. While this approach requires more transistors per pixel, it has several distinct advantages. CMOS sensors can be
fabricated using standard CMOS process, with amplification of the integrated charge can be performed at the pixel level. Active-pixel architectures are common among CMOS image sensors and provide a substantial boost to signal levels over their CCD counterparts, which must shuttle the charge off-chip before providing amplification. The ability to utilize traditional CMOS processes also provides the opportunity for more sophisticated CMOS circuits to be designed onto the sensor. This extra level of analog or digital processing can be application specific and heavily parallelized, lightening the processing load on the readout circuitry.

Traditionally, CCDs have remained the dominant form of photosensor technology among scientific applications for their historically low readout noise and high pixel density. Early CMOS image sensors utilized passive pixel sensors with much higher read noise than CCDs of the time. Adding active amplification to each pixel in the array would substantially improve sensor performance and smaller feature size fabrication processes made this a reality in the early 1990s. On-sensor digital processing lends CMOS sensors a significant advantage that will only continue to grow with shrinking technology sizes. Another significant difference between CMOS and CCD architectures is their ability to operate at extremely low temperatures. CCDs rely on doped charge wells to transfer charge. Electron freeze-out occurs near cryogenic temperatures, and progressively limits the effectiveness of the charge transfer mechanism as the device gets colder. CMOS architectures don’t suffer from the same weakness and can theoretically operate down to temperatures as low as 4K [2]. CMOS transistor operation improves at lower temperatures, due to an increase in carrier mobility. Scientific CMOS (sCMOS) detectors offer many of the same advantages as standard CMOS, while also exhibiting lower read noise and dark current [3].

One of the most compelling applications of any extreme temperature technology is space flight and exploration. The tremendous temperature gradients experienced in space, from over 800K on the surface of Venus, down to roughly 40K at the orbiting distance of Pluto, spacecraft need to be designed
with this tremendous temperature range in mind [4]. Typically, spacecraft utilize various heating, cooling, and insulation methods to keep electronics within normal operating temperatures. Designing systems that can operate at temperatures closer to the environment, however, simplifies the design and makes the spacecraft more efficient. This can also lead to new scientific opportunities, as instruments are better able to take measurements of their environment the more fully exposed they are to it. To this end, the development of extreme temperature electronics is highly relevant to space exploration.

If sCMOS detectors can be functionally validated in a flight environment, then their potential for future deep-space missions can be fully realized. The primary goal of this research project was to develop a system capable of operating a sCMOS image sensor in a cryogenic environment, to be used in a star tracking application.
Chapter 2: Background

2.1 Extreme Temperature Electronics

Extreme temperature electronics covers a wide breadth of temperatures, ranging from the millikelvin to the hundreds of degrees Celsius. Within this application, cryogenic temperatures are defined as anything below 77K, which is also the boiling point of liquid nitrogen. BJT's and MOSFETS behave vastly different in these environments, with the former barely operating at 80K, and the later operating as low as 4K [5].

Temperature dependencies of bipolar junction transistors and MOSFETs in CMOS processes can largely be explained by changes to the silicon substrate. As temperature decreases, the two most significant changes to the characteristics of the doped silicon are an increase in carrier mobility, and a decrease in carrier concentration. The former is due to a decrease in the size of the silicon lattice, while the latter is what is known as “freeze-out”. At these temperatures, dopant atoms are more likely to recombine than exist in an ionized state. In a BJT, this has the effect of increasing the base resistance and decreasing the current gain, which severely limits its usability. Bipolar transistors are available in any CMOS process, and are commonly used as band gap voltage references. Some experiments have shown that BJT bandgap references can potentially remain active as low as 80K [6].

MOS transistors see a performance increase at cryogenic temperatures. The charge carrier mobility is improved due to the reduction in lattice scattering, increasing the drive current of the transistor [4]. The equation modeling the drive current is listed below and shows that the mobility is proportional to $I_{DS}$ and $I_{dsat}$.

$$I_{DS} = \mu_{eff} C_{OX} \frac{W}{L} (V_G - V_T) V_{DS} ; I_{dsat} = \mu_{eff} C_{OX} \frac{W}{L} \frac{(V_G - V_T)^2}{2m}$$ (1)
This benefit is slightly offset by a temperature dependence of the threshold voltage. Decreasing carrier concentration means that for a given drain current, a higher gate voltage is necessary at lower temperatures. This effect has been observed to be roughly -1mV / K [4]. At 80K, this equates to a roughly 200mV increase in threshold voltage.

2.2 Photodiode Theory

The photodiode is the basis for all modern image sensing technologies, implemented in its simplest form as the humble P-N junction. When the junction is struck by a photon with energy greater than 1.14 eV, an electron-hole pair is created. These freed electrons form a voltage that can be directly correlated to the intensity of the light that is incident on the pixel. Using the 1.14eV photon above, and equation (2) below, the maximum wavelength that can be measured is calculated in (3).

$$\lambda = \frac{12.390}{E(eV)}$$  \hspace{1cm} (2)

$$\frac{12.390}{1.14eV} \approx 10900\text{nm}$$ \hspace{1cm} (3)

The sensitivity of a photodiode is characterized by two key factors: quantum efficiency and spectral response. The former is the fraction of incident photons that produce a useful charge within the sensor. Quantum efficiency is heavily influenced by the wavelength of the incident photon. This is measured as the spectral response of a photodiode, which is a measure of quantum efficiency at different wavelengths.

Dark current occurs through the thermal generation of minority carriers and is intrinsic to all semiconductor devices. These minority carriers are generated at many junctions, including the neutral bulk, the depletion region, surface states at the Si-SiO\textsubscript{2} interface, and potentially even the result of interface traps caused by processing defects [7]. Dark current generated within the neutral and depletion
regions of the photo-diode can be described using the Shockley-Read-Hall (SRH) process, shown below in equation (4).

\[
U = \frac{\sigma_p \sigma_n v_{th} N_t}{\sigma_n \left( n + n_i e^{-\frac{E_t - E_i}{kT}} \right) + \sigma_p \left( p + p_i e^{-\frac{E_t - E_i}{kT}} \right)} \left( np - n_i^2 \right) \tag{4}
\]

\( U \) represents the carrier generation/recombination rate, \( \sigma_n \) and \( \sigma_p \) are the electron and hole capture cross sections, \( v_{th} \) is the thermal velocity, \( N_t \) is the concentration of defects at energy level \( E_t \), \( n \) and \( p \) are the number of free electrons and holes, and \( E_i \) is the intrinsic Fermi level [6].

The CMOS pixel architecture requires additional transistor overhead to amplify and read out the integrated charge from individual photodiodes. Figure 2 demonstrates two of the most common CMOS photodetector structures, the 3-Transistor and 4-Transistor Active Pixel Sensors, which utilize a PN junction and pinned photodiode (PPD), respectively. The PPD approach utilizes a buried diode structure with a p+ layer to reduce transfer lag and dark current [1], [8].

While the 4-T pinned photodiode approach does have a slightly larger pixel area, its advantages over the PN junction include controllable photodiode capacitance, complete charge transfer, and a substantial reduction in dark current. These designs can be further improved with the addition of
additional transistors. The detector selected for this experiment utilizes a 5T architecture, with the additional transistor behaving as a global reset and anti-bloom drain. The details of this architecture are discussed in a later section.

2.3 Noise Sources

Throughout the readout process, there are several factors which introduce uncertainty into the final measurement. The path of the measurement from the photodiode to the ADC is illustrated below.

![Figure 3: Noise Sources in CMOS Image Sensor Measurement Path](image)

Noise is first introduced into the measurement at the photodiode, which can be broken down into several sources. The first of those is photo response non-uniformity. This is used to describe the non-uniformity of each individual pixel to light due to process variations [9]. Photon shot noise is due to the quantum nature of photons themselves, which means that the number of photons incident on the detector itself has some amount of variance. This is out of the control of the experiment and has no dependence on the temperature of the detector. Dark current, as mentioned previously, is the leakage current within the photodiode. Different pixels produce different amounts of dark current, however, resulting in a fixed pattern noise (FPN) in the measurement [7]. Dark current is highly dependent upon detector temperature, seen in equation (4) so it is reasonable to expect this noise source to decrease as temperature increases.

The dominant noise sources in the source follower transistor are flicker and random telegraph signal noise. Traps in the silicon lattice randomly capture and emit charge carriers, modulating the
channel conductance. The increased mobility of charge carriers could potentially increase this noise at cryogenic temperatures. Noise is also introduced at the row and column levels due to reset voltage noise and fabrication differences between the sample and hold capacitors, respectively. Distinguishing these two noise sources will become important for later analysis, as noise present in the pixel reset voltage is a direct result of design choices, whereas the noise introduced by the sample and hold capacitors cannot be controlled. The performance of these MOS capacitors is dependent upon temperature, and variance between the capacitors will increase as temperature decreases [10]. It is also worth considering the thermal noise of all circuits prior to the ADC, caused by the thermal generation and regeneration of carriers in the silicon. As the name suggests, this noise is highly dependent upon temperature, and decreases substantially at cryogenic temperatures [11]. Finally, a small amount of uncertainty is introduced by the conversion process of the ADC, referred to as quantization noise. This is due to the fundamental operation of the ADC, which has a lower bound to the precision of the converted measurement. Any signal below the minimum quantization of the ADC will not be captured in the measurement.

During normal operation of the detector, noise in the active pixel portion signal path prior to the ADC is reduced through a process called correlated double sampling. By sampling the reset voltage of the floating diffusion, and subtracting it from the converted charge voltage, the difference value should, theoretically, eliminate noise introduced by the charge to voltage conversion and the source follower transistor. This differencing takes place anytime a pixel is read out through the column amplifier. For the purposes of this project, the read noise of the detector is calculated as follows [12].

$$\text{Read Noise} = \frac{\text{Standard Deviation of Difference Frame} \times \text{Column Amplifier Gain}}{\sqrt{2}}$$  \hspace{1cm} (4)

A difference frame is obtained by taking two frames of 0ms exposure time and subtracting them. This eliminates any FPN from the estimation and provides an estimate which reflects only the system
read noise [12]. Effectively estimating this value is important for determining the detectors performance in a star tracking application.

2.4 *Star Tracking Systems*

At the most basic level, a star tracker is an image sensor controlled by a processor. Images are taken of a star field, which the processor then analyzes to determine which stars are the brightest. The coordinates of these stars are compared to their coordinates in the previous image, and the difference is computed as a change of attitude. For the CIBER-2 experiment, these changes in attitude are communicated to the attitude control system, which attempts to correct the orientation of the rocket using a closed loop control system. The equation for the recommended detection threshold is as follows.

\[
detection\ threshold = A_{\text{pixel}} + 5 \times \sigma_{\text{pixel}} \times \frac{1}{\int_0^1 \int_0^1 \frac{1}{2\pi\sigma_{\text{PSF}}} e^{-\frac{x^2 + \frac{y^2}{2\sigma_{\text{PSF}}}}}}
\]  

(5)

In this approximation, \(A_{\text{pixel}}\) is the average pixel value, \(\sigma_{\text{pixel}}\) is the standard deviation of the pixel values in a difference frame, and \(\sigma_{\text{psf}}\) is the point spread function, represented in pixels [13]. The viability of this system as a star tracker will depend on two main factors: the sensitivity of the detector, and the read noise. Both will have some temperature dependence, but for the detection limit to hold true, the sensitivity and read noise must remain high and low enough, respectively, to stay above the detection limit.

For the star tracker to remain functional at cryogenic temperatures, the quantum efficiency must not drop below a certain fraction of its room-temperature performance. Additionally, the read noise of the detector must remain low enough so that stars can be distinguished against a dark background. MOSFET transistors can theoretically remain operational down to 4K, and BJT transistors remain partially operational down to 80K. For these reasons, it is reasonable to assume that an sCMOS image sensor, and all its circuits, will remain mostly functional down to cryogenic temperatures.
2.5 **Related Work**

Previous research that was relevant to this project falls into a few different categories. CMOS image sensors have been used to great effect in several low noise, high sensitivity applications. The low dark current of these detectors makes them an excellent fit for low-light applications, where 5T pixel architectures are especially well suited due to global shutter operation [14]. A similar CIS architecture was evaluated in this study, and the low-light performance was deemed sufficient for low-light and astronomical applications [15]. A previous version of the CIS2521 detector was used as a low-light camera in a highly ruggedized military application [16]. These research efforts suggest that CMOS and sCMOS sensor have considerable potential in low-light instruments. Cryogenics have been a research topic for decades, so it should come as no surprise that researchers are constantly evaluating and testing new circuits in low-temperature environments. In one experiment, off the shelf FPGAs from Xilinx and Altera were evaluated at cryogenic temperature and realized a noticeable improvement [17]. These components have standard military grade temperature ranges, but due to their reliance on CMOS transistors, can be operated at much lower temperatures. Active pixel sensors (APS) are an especially enticing choice for cryogenic applications. One additional transistor per pixel is the minimum requirement for an active pixel architecture, resulting in lower read noise. Two papers focus on designing robust APS circuits specifically for cryogenic applications [18], [19]. From a fundamental standpoint, this preliminary research suggests that a cryogenic sCMOS detector is not only feasible, but has a wide variety of applications outside of space exploration.

2.6 **CIBER-1 / CIBER-2 History**

The cosmic infrared background imaging experiment, also referred to as CIBER, was a near infrared imaging experiment with the goal of capturing the extragalactic background light, an integrated emission from all sources outside the Milky Way [20]. The electromagnetic spectrum measured by the
experiment (0.8 to 2 microns) required the optics to be cooled to a cryogenic temperature of approximately 80 K, minimizing the effects of blackbody radiation on the measurements. Data was collected over the course of four sounding rocket flights between 2009 and 2013, which proved instrumental in studying the origins of the universe. Following the success of the CIBER project, the CIBER-2 project hopes to improve upon the results of its predecessor by increasing the sensitivity and the extending the wavelength captured.

One of the main flaws of the original experiment, however, was the method of maintaining rocket attitude. A side-looking star tracking camera was placed in a warm compartment of the rocket skin, beneath the main imaging sensors. During the powered phase of the mission, friction with air molecules heated up the rocket skin. Once the detection portion of the experiment began, the rocket skin began to cool down again. The deflection of the rocket skin caused by these thermal changes resulted in a noticeable drift in the measurements.

![Figure 4: Thermal Deflection of Rocket Skin in CIBER-1 Experiment [20]](image)

While the small amount of error this introduced into the experiment was acceptable for CIBER, the increased plate scale of CIBER-2 requires an entirely different approach. A cryogenically cooled
star-tracking system is proposed and implemented, one which could withstand the temperatures of the main experiment and more effectively maintain the rocket attitude.

2.7 **CSTARS History**

The cryogenic star tracking attitude regulation system, or CSTARS project, was an undergraduate research initiative started in the summer of 2016, with the goal of demonstrating the operation of CMOS image sensors down at cryogenic temperatures. Charge coupled devices are typically chosen for astronomical imaging applications, however the fundamental operation of charge transfer fails to work under roughly ~100 K. Thus, a CMOS image sensor was a necessity for the project. The team selected the STAR1000 CMOS image sensor, and designed their system around reading the analog outputs of the detector. Two ZYBO development boards were used to read and store the images from the detector. Between the summer of 2016 and the spring of 2017, the project would go on to validate the operation of a CMOS sensor at cryogenic temperatures, as well as design a system to be tested on its own sounding rocket flight [21].

![Figure 5: Cryogenic Testing of CSTARS-1 Detector (Left), Sounding Flight Configuration of CSTARS-1 System (Right) [21]](image_url)
Integration issues encountered in the final weeks before launch prevented the system from being tested in the relevant environment. A new team of undergraduates has resumed work on the project, with hopes of a sounding rocket flight at some future date. The lessons learned from the CSTARS project were used to develop a more reliable and effective star tracker for CIBER-2. Some of the significant differences between the two systems include a new hardware development board utilizing the same ZYNQ series processor, a higher resolution image sensor with digital output for more accurate starfield imaging, and entirely new hardware, to accommodate the challenging physical constraints of the CIBER-2 experiment. This improved star tracking system is referred to as CSTARS-2, the hardware and software design of which is outlined in the following chapter.
Chapter 3: Design and Simulation

3.1 CSTARS-2 Star Tracker System Overview

The star-tracking system can be divided into two major sections; the cold electronics, and the warm electronics. Because of the challenge of operating electronics in a cryogenic environment, discussed in previous sections, it was important to keep as much of the system as possible in the warm portion of the rocket. The limiting size requirement for the cold electronics further reinforced this approach. The block diagram illustrated in Figure 7 below demonstrates the various components of the star tracking system.

![Block Diagram of CSTARS-2 System](image)

**Figure 6: Block Diagram of CSTARS-2 System**

The hardware for the warm electronics is located on the interface printed circuit board. Acting as a carrier card to the MicroZed system on module, this interface board performs critical power regulation, digital interfacing, and analog thermometry readout functions. The cold electronics are entirely contained within the focal plane printed circuit board, consisting of the CIS2521 sensor and several thermal diodes, used to monitor the temperature of the system.
3.2 System Requirements

The design of this system was largely dictated by the requirements for the CIBER-2 project. Communication interfaces, electrical connections, and mechanical constraints were carefully evaluated and communicated with team at Caltech responsible for final integration. A 3D model of the CIBER-2 experiment, including the CSTARS-2 cryogenic star tracker, is shown below in Figure 6.

![CIBER-2 3D Model](image)

Figure 7: CIBER-2 3D Model [20]

The CSTARS-2 system will play a crucial role in the CIBER-2 experiment. The sCMOS detector will be mounted along the main optical spine in the cryogenic portion of the experiment. During the rocket’s ascent through the atmosphere, the attitude control system will rely on the primary, side-looking star tracker to maintain the alignment of the rocket. When the CIBER-2 detectors begin capturing data, the attitude control system will begin receiving tracking coordinates from CSTARS-2. The images obtained co-boresighted with the primary telescope will form a more accurate representation of the
current rocket attitude. In order to achieve these goals, the CSTARS-2 star tracker must meet a number of minimum specifications, listed below in table 1. This includes environmental, mechanical, electrical, and optical performance constraints.

Table 1: CIBER-2 Experiment Requirements

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Approximate Cold Electronics Temperature</td>
<td>80K</td>
</tr>
<tr>
<td>Approximate Cold Electronics Vacuum</td>
<td>&lt; $10^{-6}$ mbar</td>
</tr>
<tr>
<td>Approximate Warm Electronics Vacuum</td>
<td>&lt; $10^{-2}$ mbar</td>
</tr>
<tr>
<td>Size of image on detector</td>
<td>3mm x 5mm</td>
</tr>
<tr>
<td>Detector Readout Speed</td>
<td>10 Frames per Second</td>
</tr>
<tr>
<td>Approximate Harness Distance Between Warm and Cold Electronics</td>
<td>7 ft</td>
</tr>
<tr>
<td>Maximum Focal Plane Board Size</td>
<td>7cm x 7cm x 7cm</td>
</tr>
<tr>
<td>Maximum Warm Electronics Size</td>
<td>9 in x 10 in x 4.5 in</td>
</tr>
<tr>
<td>Synchronous Rocket Telemetry Stream Connection Speed</td>
<td>8Mbps</td>
</tr>
<tr>
<td>Asynchronous Attitude Control System Connection Speed</td>
<td>115.2kBaud</td>
</tr>
<tr>
<td>Attitude Control System Update Frequency</td>
<td>20 Hz</td>
</tr>
<tr>
<td>Maximum System Power Consumption</td>
<td>12V 1.6A continuous, 3A peak</td>
</tr>
</tbody>
</table>

The environmental requirements for the star tracker have been determined by the minimum achievable temperature for the cryogenic portion of the experiment. This is a worst-case estimate, as the mounting points for the detector are far away from the actively cooled portion of the spine. Nonetheless, such temperatures could be reached if the entirety of the system remains off for an extended period. It is important that the developed system is capable of being fully cooled down to 80K, and reliably power
on and resume operation. Additionally, it should be noted that both the warm and cold portions of the experiment will be operating under vacuum. Because of the atmospheric conditions of the experiment, the warm electronics will also be subjected to a vacuum. This makes heat dissipation especially challenging, as convection is no longer a viable option. Heat generated by the warm electronics must be effectively conducted into its enclosure, where it can then radiate out of the rocket skin.

The mechanical constraints for the project have been allocated based upon the remaining space surrounding the primary optics of the CIBER-2 experiment. This leaves an incredibly restrictive space for the cold electronics, which required careful consideration. The warm electronics, fortunately, were allocated a much larger region, allowing for an emphasis on ease of use and debugging. Another challenging aspect of the mechanical constraints was the separation between the warm and cold electronics. Nearly seven feet of harnessing is necessary to electrically connect the allocated space within the warm portion and the allocated space within the cold portion. Reliable operation of the detector at this distance is an important requirement of the design.

The frame rate for the detector and the star tracking system was determined by the minimum requirements of the attitude control system to maintain rocket attitude. 10 frames per second was an arbitrary estimate made by the team in charge of the attitude control system, based on experience with other star tracking setups. Otherwise, the specifics of the detector performance were entirely the decision of the CSTARS-2 team, with an emphasis on characteristics that would improve star-detection and reliability based on parameters reviewed earlier.

An asynchronous link between the attitude control system (ACS) and the star-tracker was developed using the UART protocol. A defined message structure is sent to the ACS every 50ms, providing update star-tracking coordinates to the system as the experiment proceeds. The UART parameters are listed in the following table, referenced from the Bock II Cold Tracker to ACS Interface document.
Table 2: Asynchronous ACS Interface Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>115.2 kBa</td>
</tr>
<tr>
<td>Data Bits</td>
<td>8</td>
</tr>
<tr>
<td>Parity</td>
<td>None</td>
</tr>
<tr>
<td>Stop Bits</td>
<td>One</td>
</tr>
</tbody>
</table>

Each transmitted message consists of 21 bytes of information, formatted as shown below. This information is also being referenced from the Bock II Cold Tracker to ACS Interface Document.

Table 3: Asynchronous ACS Interface Message Format

<table>
<thead>
<tr>
<th>Data name</th>
<th>Byte index</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Header</td>
<td>0,1</td>
<td>2 ascii characters, ‘C’ and ‘T’</td>
</tr>
<tr>
<td>Frame counter</td>
<td>2,3,4,5</td>
<td>A 32 bit counter that starts at zero and increments on every data frame to the ACS</td>
</tr>
<tr>
<td>Status word</td>
<td>6,7</td>
<td>A 16 bit unsigned short that should include enough health information to indicate to the ACS that the cold tracker is generating good position signals</td>
</tr>
<tr>
<td>Position X</td>
<td>8,9,10,11</td>
<td>32 bit signed integer where each count represents one milli-arc-second.</td>
</tr>
<tr>
<td>Position Y</td>
<td>12,13,14,15</td>
<td>32 bit signed integer where each count represents one milli-arc-second.</td>
</tr>
<tr>
<td>Position Z</td>
<td>16,17,18,19</td>
<td>32 bit signed integer where each count represents one milli-arc-second.</td>
</tr>
<tr>
<td>Checksum</td>
<td>20</td>
<td>An 8 bit sum of all of the bytes in the message up to the checksum byte. Ignore the overflow.</td>
</tr>
</tbody>
</table>
The success of the experiment will be determined not only by whether the cryogenic star tracker is fully operational, but if it can be determined that the system is operating correctly and make a corrective switch if necessary. To capture the information being sent to the ACS, and validate after the flight, a duplicate of this stream is sent to the telemetry encoder, to be captured along with the synchronous telemetry stream.

The purpose of the synchronous telemetry stream is to relay housekeeping information from the star-tracking system to the onboard telemetry encoder. This encoder requests 10-bit words from each of the instruments onboard the experiment, in a sequence defined by the 36.281 measurement matrix. A total of 161 10-bit words are sampled for each minor frame of the matrix, a pattern which is repeated a total of 32 times for each major frame. This results in an encoder data rate of 8 Mbps, 3Mbps of which is allocated to the CSTARS-2 housekeeping. The data is formatted following the IRIG16 Chapter 10 Data encoding standard [22] and relayed from the encoder through an antenna to a telemetry ground station. This ground station will provide the Chapter 10 packets via a UDP link, after which the various layers can be unpacked, and the information can be displayed to the experimenters. The purpose of this housekeeping stream is to validate the successful operation of the CSTARS-2 system. Unfortunately, no control exists from the experimenters to the rocket during flight, so this stream remains unidirectional. The specific implementation of both interfaces is discussed further in the firmware development section.

### 3.3 Image Sensor Selection

The image sensor selected for this application is the Fairchild Imaging CIS2521, a 5.5-megapixel sCMOS detector. When compared to traditional CMOS sensors, sCMOS detectors offer lower read noise and dark current, making it especially viable for this low-light application. [17]. Table 4 lists the specific characteristics of the detector.
| Table 4: CIS2521 Specifications [23] |
|-------------------------------|-----------------|
| Optical format                | 4/3’’           |
| Active Pixel Array Size       | 2560 (H) X 2160 (V) |
| Individual Pixel Size         | 6.5um x 6.5um   |
| Active Pixel Area             | 16.6 mm x 14.0 mm |
| Shutter Operation Modes       | Rolling Shutter (RS), Global Shutter (GS) |
| Maximum Frame Rate            | 100 fps (RS), 50 fps (GS) |
| Read Noise                    | < 2e- RMS (RS), <5e- (GS) |
| Dynamic Range                 | >83.5 dB        |
| Peak QE                       | >55%            |
| Dark Current                  | < 35 e-/pixel/sec |
| Power consumption             | <2W at 100 fps  |
| Operating Temperature         | -40C to +55C    |

The low read noise and high frame rate of this detector make it a perfect candidate for astrophysical applications. However, this detector was selected before the optical specifications were complete, resulting in the imaging area of the full detector being much larger than the size of the image on the detector. Fortunately, the CIS2521 has a unique feature to help mitigate this issue. To speed up the maximum frame rate of the detector, the full 5.5MP array is split into a top and bottom half, each with independent power and control. If the full detector was being utilized, this effectively doubles the throughput of the detector, as the ADCs on both halves of the detector will clock out a newly converted pixel every clock cycle [24]. In this application, it allows for only one half of the sensor to be operational. This saves power and complexity, in addition to reducing the necessary bandwidth to readout the detector. For this reason, all bandwidth and data transfer calculations will be performed with only the active pixels on the bottom half of the sensor. What follows is a brief overview of the detector readout architecture and modes of operation.
While three and four transistor CMOS architectures were discussed previously, the CIS2521 is designed with a five-transistor pixel, pictured below.

![Diagram of 5T Photodiode Architecture](image)

Figure 8: 5T Photodiode Architecture [24]

The standard readout mode of the detector is rolling shutter. Each row of the detector is sequentially read and reset, providing fast measurements with the lowest readout noise achievable on the CIS2521 [25]. The addition of a fifth transistor allows for the external reset of every photodiode simultaneously, allowing for a second readout mode known as global shutter. In this mode, the external connections to transistors TX1 and TX2 are responsible for charge transfer. This is incredibly effective at reducing blur and artifacts, as every pixel on the detector integrates charge simultaneously. This introduces another challenge, however, as the correlated double sampling performed by the column amplifiers cannot be used to fully reduce read noise, due to the global operation of TX1 [26]. Therefore, a process called correlated quadruple sampling must be performed. After every photodiode is globally reset, a reset value is read from the floating diffusion of every pixel on the detector. At this point the integrated charge is transferred to the floating diffusion using TX1. Figures 9 and 10 below help illustrate the differences between rolling and global operation.
Figure 9: Rolling Shutter Operation of CIS2521

In the above Figures a few additional signals have been added for clarity. SCLK is the main detector clock, which is continuous throughout both modes of operation. FVAL is the frame valid signal, an active high indication that the values currently being read out are in the active pixel region. DATASEL is only used in global shutter mode and selects between two internal readout sequences, and between the reset and the data frame. DOUT is a description of the current frame being read out of the detector. The pre-scan region is a user-selected region of non-existent pixels, which are added to the readout sequence to prevent charge transfer from affecting measurement results. The exposure time for
each of the modes has also been labeled and is inversely proportional to clock frequency. Finally, TX1 and TX2 control the charge transfer of the photodiode and can be seen in Figure 8.

Because a reset and a data frame must be read out for global shutter operation, twice the bandwidth is required to capture the same number of images. This plays a key factor in the comparisons between global and rolling shutter for this application. After charge has been transferred to the floating diffusion, the detector sweeps through a specified region of interest and selects the pixels of each row to be read by a dual channel ADC. Each time that a pixel is read from the detector, correlated double sampling is performed. By sampling the floating diffusion at reset and subtracting the value from the integrated charge, the FPN prior to the Column amplifiers can be reduced. The two channels are low and high gain amplifiers, with user programmable gain values [24]. The benefit to this setup is that reading out both results provides a very high dynamic range, which provided a great deal of flexibility in determining the appropriate gain settings for star detection.

![CIS2521 Dual Column Amplifiers](image)

Figure 11: CIS2521 Dual Column Amplifiers [26]
With the resolution of the bottom half of the detector equaling 2560 (H) x 1080 (V), the bottom half of the detector consists of 2,764,800 pixels. In addition to the active pixels, the default readout sequence also includes optically and electrically dark pixels; These are found at the ends of the row and columns, shown in Figure 12. This brings the total default pixel count to 2,840,832.

![Figure 12: CIS2521 Pixel Layout, Including Inactive Pixels](image)

This pixel arrangement is the result of the design and packaging of the detector. As mentioned previously, the pre-scan region also adds a few additional rows to the overall readout. These rows are clocked out while the frame valid signal is low, because they are not part of the main region of interest. Because they are user selectable, and are read out during the FVAL low period, they have not been included in the bandwidth calculations. Therefore, the total number of pixels in each frame is calculated as follows.
\[
\frac{\text{Total pixels}}{\text{frame}} = (2560 \text{ active columns} + 32 \text{ optically dark columns})(1080 \text{ active rows} + 16 \text{ optically dark rows}) = 2,840,832 \frac{\text{total pixels}}{\text{frame}}
\]  

Further, the necessary bandwidth to read frames off the detector at the required 10 fps is calculated below.

\[
2840832 \frac{\text{Total pixels}}{\text{frame}} \times 10 \frac{\text{frames}}{\text{second}} = 28,408,320 \frac{\text{pixels}}{\text{second}} = \sim30\text{MHz (RS)}, \sim60\text{MHz (GS)}
\]  

\[
2840832 \frac{\text{Total pixels}}{\text{frame}} \times 2 \frac{\text{bytes}}{\text{pixel}} \times 10 \frac{\text{frames}}{\text{second}} = \sim57\text{MBps (RS)}, 114\text{MBps (GS)}
\]  

These could be further improved using a selected region of interest. By only reading out the columns that are actively used in the experiment, the 10fps requirement could be achieved at a substantially lower operating frequency and bandwidth.

### 3.4 Processor Selection

The Zynq 7000 series offers a tremendous degree of flexibility when tackling the challenges of this project, as well as offering the processing power necessary to perform the necessary computations. This specific chipset utilizes a dual-core ARM Cortex-A9 processing system, in addition to a 28nm Xilinx programmable logic array [27]. The combination of an ARM processor and an FPGA allow for consistent, high-speed control of the detector, while simultaneously executing the timing intensive star-tracking algorithm.

To simplify hardware development for the project, a system on module development board was utilized. The CSTARS-1 project utilized a Zybo development board, with mixed success. While this board utilizes a Zynq-7000 series SoC device, it has limited hardware support for external IO. For this reason, two Zybo boards were required to reach the total number of IO required. For the CSTARS-2
hardware, a MicroZed development board was chosen. The MicroZed board has two 50 pin connectors
mounted on its underside, providing access to 100 IO pins routed to the programmable logic of the
ZYNQ chip. This makes connecting the MicroZed to the interface board simple and reliable and
provides a much greater number of available IO. This, combined with the smaller form factor, make it
an excellent choice for this application. Additional specifications for the system on chip (SoC) device
and the MicroZed system on module (SoM) listed below in table 5.

Table 5: MicroZed Features [28]

<table>
<thead>
<tr>
<th></th>
<th>1GB DDR3 SDRAM, 2.1Mb Block Ram, 128Mb QSPI Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>100</td>
</tr>
<tr>
<td>User I/O</td>
<td>28K</td>
</tr>
<tr>
<td>Logic Cells</td>
<td>866MHz</td>
</tr>
<tr>
<td>Maximum Processor Frequency</td>
<td></td>
</tr>
</tbody>
</table>

3.5 **Hardware Development**

The schematics and printed circuit board layouts were designed using Autodesk Eagle version
9.01. 3D models of the printed circuit boards were generated using Autodesk Fusion 360. The
schematics and board layout can be found in the hardware appendix and have also been included within
the project archive.

3.5.1 **Focal Plane Board**

A printed circuit board (PCB) was developed for the cold portion of the electronics. The
allocated space within the main CIBER-2 experiment for the star-tracking camera, including the
enclosure, was a measly 7cm cube to be mounted along the main optical spine. Because of this, the focal
plane board was designed to be as small as possible, while still adhering to common circuit layout
practices. Figure 13 is a 3D model generated using Autodesk EAGLE PCB designer and Fusion 360.
A four-layer PCB was designed with the two signal layers, a ground layer, and two power and reference layers. The top layer was dedicated to any high-frequency digital signals, with a continuous ground pour forming the layer directly underneath. This was to allow return currents the path of least impedance directly underneath the signaling lines [29]. The two power layers were necessary to adequately distribute the various voltage sources and references to their respective pins. Additionally, the ground plane prevents the capacitive coupling of noise from the noisier digital circuits into the analog references.

The complexity of the circuits on the focal plane board were kept to an absolute minimum, the reasoning for which is twofold. Firstly, the cryogenic environment will have an impact not only on the detector, but on any circuit component placed on this board. For this reason, voltage supplies and references were in the warm portion of the electronics on the interface board, to be discussed later. Secondly, the tight size constraints of the focal plane board left little room for additional hardware, especially considering the already challenging routing of the four-layer board. More complex circuitry would likely require either a larger PCB, or a higher layer count. For these reasons, the only components on this board, aside from the detector, are passive components, for power filtering and necessary support circuitry. Based on the information captured in reference [30], these passives were carefully selected, and the tolerances were chosen to guarantee their functionality at cryogenic temperatures. Carbon film
resistors and ceramic capacitors were chosen due to the low temperature coefficient of their resistance and capacitance, respectively.

Special care was taken during the manufacturing process for this board. An automated reflow setup was used, to gradually increase the temperature in very specific increments, to avoid overheating the detector. Despite the care that was taken, connectivity issues were still observed with certain solder connections to the detector, discussed further in the testing and verification section.

3.5.2 Harnessing

The interconnection between the cold and warm electronics presented another interesting challenge. The warm electronics and the cryogenic focal plane board are separated by roughly seven feet of harnessing, with a hermetic connector at the division between the warm and cold segments. To minimize the thermal load of these connections outside of the cryogenics, the wire material was carefully selected. Digital signals and references were connected with manganin, a material with higher resistivity and a much lower thermal conductivity than copper [31]. For the higher current supplies, thin gauge copper wire was used instead, to mitigate the voltage drop across the cable [32].

A harness of this length presents several limiting factors on the performance of the system. With regards to digital signal integrity, noise and signal reflection are two of the biggest concerns. To mitigate the effect of externally coupled noise on the harness, a shielded cable was used for the warm portion. Because of the potential thermal conduction, shielding was not implemented in the cold portion. For the full length of the harness, however, the highest frequency signals and sensitive references were wired in twisted pairs with ground. This was used to improve their ability to reject environmental noise, which could even be coming from other wires in the harness [29]. Physical separation was a valuable tool to reduce capacitively coupled noise from within the harness. 26 conductor cables were used for the warm
harness, and the most sensitive references were routed through a different cable than the noisy digital signals, to increase their separated distance.

### 3.5.3 Interface Board

Most of the hardware design for the CSTARS-2 system went into the warm electronics, also referred to as the interface board. The primary functions of this board are discussed in detail throughout the following sections.

![CSTARS-2 Interface Electronics Board 3D Model](image)

**Figure 14: CSTARS-2 Interface Electronics Board 3D Model**

The CSTARS-2 system receives a +12V power supply from the CIBER-2 experiment. This supply is used to provide power for the various supplies of the CIS2521 detector, the MicroZed SoM, and the circuits within the interface board itself. Table 6 below lists the initial power consumption estimates.
Table 6: Interface Board Power Consumption Estimate

<table>
<thead>
<tr>
<th>Device</th>
<th>Nominal</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>MicroZed</td>
<td>5V, 400mA</td>
<td>5V, 1.7A</td>
</tr>
<tr>
<td>CIS2521</td>
<td>1W</td>
<td>2W</td>
</tr>
<tr>
<td>Interface Board Circuits</td>
<td>1.8V, 50mA</td>
<td>1.8V, 200mA</td>
</tr>
<tr>
<td>Total</td>
<td>3.01W</td>
<td>10.86W</td>
</tr>
</tbody>
</table>

The decision was made, based on issues encountered with the CSTARS-1 hardware, to avoid the use of switching voltage regulators. Instead linear regulators were used to reduce the input voltage the necessary level for these circuits. Linear regulators introduce a voltage ripple that is typically an order of magnitude less than that of a switching regulator, making them an appropriate choice for low-noise applications. Additionally, the power supply rejection ratio of a linear regulator reduces any voltage ripple on the input voltage to the regulator. The tradeoff for these benefits is very poor efficiency. The power conversion method utilized by linear regulators is entirely lossy, dissipating the difference in energy at the input and output as heat. A simple equation to estimate the power dissipation of a linear regulator is shown below [33].

\[
\text{Power Dissipation} = (\text{Input Voltage} - \text{Output Voltage}) \times \text{Output Current} \quad (9)
\]

This is not a perfect approximation, due to small leakage currents in the feedback network used to regulate the voltage, but it is good enough for rough estimates. If all the regulation of the interface board is performed with linear regulators, the maximum necessary current at the input can be calculated as follows.
Table 7: Interface Board Power Consumption with Linear Regulators

<table>
<thead>
<tr>
<th>Device</th>
<th>Nominal</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>MicroZed</td>
<td>12V, 400mA</td>
<td>12V, 1A</td>
</tr>
<tr>
<td>CIS2521</td>
<td>12V, ~400mA</td>
<td>12V, ~800mA</td>
</tr>
<tr>
<td>Interface Board Circuits</td>
<td>12V, 50mA</td>
<td>12V, 200mA</td>
</tr>
<tr>
<td>Total</td>
<td>12V, 850mA</td>
<td>12V, 2A</td>
</tr>
</tbody>
</table>

Peak power consumption of the system is below the maximum specified within the requirements, and the nominal is almost half of the nominal current requirement. Further, the heat dissipation of the regulators can be estimated using equation 9 above in conjunction with tables 6 and 7.

Table 8: Interface Board Power Dissipation Estimate

<table>
<thead>
<tr>
<th>Device</th>
<th>Nominal</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>MicroZed</td>
<td>400mA (12V-5V) = 2.8W</td>
<td>1A (12V-5V) = 7W</td>
</tr>
<tr>
<td>CIS2521</td>
<td>400mA (12V-2.5) = 3.8W</td>
<td>800mA (12V-2.5) = 7.6W</td>
</tr>
<tr>
<td>Interface Board Circuits</td>
<td>50mA (12V-1.8) = 0.51W</td>
<td>200mA (12V-1.8) = 2.04</td>
</tr>
<tr>
<td>Total</td>
<td>7.11W</td>
<td>19.14W</td>
</tr>
</tbody>
</table>

Based on these estimations, the interface board needs to dissipate nearly 20W of heat to supply the system at worst-case power consumption. This required careful consideration, especially since the warm electronics will be in a rough vacuum. With very little air surrounding these electronics, effectively no heat can be dissipated through convection. Conduction and radiation are the most effective forms of heat transfer in this environment. Nearly every linear regulator has some form of heat sink, given the heat dissipation necessary. Some regulators are designed with higher temperatures and power levels in mind, though. TO-220 packages were carefully selected for all the high current power
regulation, because of their low thermal resistance. Of the evaluated packages, the TO-220 exhibited the most favorable thermal characteristics, with a thermal resistance from junction to case as low as 2 °C/W [33].

![Microchip MCP1825S Linear Regulator with TO220 Package](image)

Figure 15: Microchip MCP1825S Linear Regulator with TO220 Package [33]

Typical mounting configurations for the TO-220 will see the heatsink of the device mounted to a heatsink with fins. These are highly effective at removing heat from the device when it is operating in an environment with a reasonable amount of air flow. Given the environment of the warm electronics, this was not a viable solution. Instead, the regulators were mounted to solid chunks of aluminum on the underside of the board, seen in Figure 16.

![Early prototype of rear-mounted heatsink on interface electronics board](image)

Figure 16: Early prototype of rear-mounted heatsink on interface electronics board
These contact the aluminum enclosure, which is affixed to the rocket skin, as in Figure 17.

![Diagram of CSTARS-2 Interface Electronics Enclosure and CIBER-2 Rocket Skin](image)

**Figure 17: CSTARS-2 Warm Electronics Mounted in Rocket Skin [20]**

This provides a clear path for heat to be conducted out of the system. Assuming the enclosure behaves as an infinite heat sink, the following calculation can be used to estimate the worst-case temperature rise of any individual regulator.

\[ T_{\text{junction}} = T_{\text{ambient}} + (\theta_{\text{junction-case}}) \text{Power Dissipated} \]  

(10)

While the CIS2521 requires the most power dissipation, this is spread over several linear regulators, supplying different voltage levels to the detector. The benefit to this approach is that the thermal load is spread across different packages. The greatest potential thermal load would be on the regulator responsible for the MicroZed. The temperature rise of this component, under worst case power consumption, is calculated below. It should be noted that a thermally isolating pad was added in between the heatsink and the TO-220 package, which can be seen in Figure 16. This has been accounted for in the calculation.
\[ T_{\text{junction}} = T_{\text{ambient}} + (\theta_{\text{junction-pad}} + \theta_{\text{pad-case}}) \text{Power Dissipated} \]  
\[ T_{\text{junction}} = 50^\circ C + (2 \frac{W}{W} + 0.5 \frac{W}{W}) \times 7W = 67.5^\circ C \]

The calculated junction temperature, 67.5°C, is well below the maximum junction temperature for the component. With adequate heat sinking, the interface board can effectively conduct the generated heat away from the board, while still providing accurate, low-noise power supplies to the various circuits.

Digital buffers were chosen on all the input and output lines from the MicroZed. This is to improve the current drive of digital signals in both directions. Additionally, series and end termination resistors were added to all the digital lines. Because the exact impedance of the harness at the time of the design was not known, it was impossible to accurately select termination resistors. If terminators are deemed unnecessary, the two termination styles can either be de-populated or replaced with a zero-ohm resistor.

The synchronous and asynchronous interfaces required hardware interfaces to support the specified protocols. The synchronous stream signals received by the interface board from the telemetry encoder are low voltage differential signals (LVDS). LVDS is unique in that it is a current-mode differential signaling scheme. The current through the termination resistor at the receiving end of the line creates a voltage drop, which is measured as either a high or a low signal. For this reason, the signaling scheme will not work without proper termination [34]. All the LVDS receivers have been terminated with 100-ohm resistors. The asynchronous stream, conversely, utilizes an RS-488 connection. This protocol is a standard voltage-mode differential pair. Even though bidirectional transceivers are utilized on the interface board, only the transmitting channel has been connected to the telemetry harness. This was done for the simple reason that the communication between CSTARS-2 and the ACS is unidirectional.
Another feature of the interface board is the ability to monitor temperatures throughout the CSTARS2 system using thermal diodes. Given the importance of temperature within the design of this system, it should come to no surprise that it is important to capture as much temperature information as possible. The forward voltage drop across a diode is heavily dependent upon temperature. The consistency of this behavior across wide voltage ranges makes these an excellent choice for monitoring a cryogenic experiment. Lakeshore DT670 calibrated diodes were selected, and constant current sources were used to power the diode with as little as 10uA. The schematic of these current sources can be found in appendix A1.2.4.

It should be noted that the resistor network is necessary to drop the maximum voltage down to a range that can be tolerated by the Zynq ADC. The input voltage to an ADC pin must not exceed 1V. Further, an additional voltage measurement is performed on VPTAT, a voltage-proportional temperature provided by the CIS2521. This is the most accurate means of monitoring the die temperature of the detector and proved instrumental in capturing accurate temperature data while the CIS2521 was operating.

3.6 **Firmware Development**

Firmware development for the MicroZed was done using the Vivado design tools, version 2017.4. This software allows for the development of a configuration bitstream, to be instantiated within the programmable logic (PL), and a software development kit (Vivado SDK) for writing C code to be executed by the processor. The design flow of the software encourages the development and testing of firmware peripherals prior to the C code. The work done will be discussed in this order as well.
3.6.1 FPGA development

The hardware implemented in the programmable logic was designed in Vivado 2017.4. The design flow of this IDE heavily encourages the use of a block-diagram based design, which was carefully utilized. Each of the following sections is an overview of the individual sections of the FPGA. Even though the dual Cortex M9 processor is not synthesized within the PL, a processor block must still be added to the design. All the connections into and out of the processor and configured within the block diagram. Within the configuration settings, the following has been enabled: both UART channels, PL to PS interrupts, and external multipurpose IO.

An interconnect block was required to connect the various AXI peripherals to the processor. It is important to note that the AXI peripheral used to directly control the detector runs at the same clock frequency, 25MHz. This helps prevent timing issues when sequencing the various sensor states. An AXI clock converter block is used to seamlessly connect the higher frequency 100MHz AXI interface to this peripheral. The two clock domains also require separate processor reset blocks. Individually, these blocks ensure that reset signals sent from the processor, operating at 280MHz, are properly received within the slower clock domains.

Before the images can be read out of the detector, the first step is to configure the internal JTAG registers. These registers control important properties such as mode of operation, region of interest, and other fine-tuned parameters [26]. For the purposes of this project, the registers are loaded with values that enable Rolling Shutter mode, along with settings to maximize its effectiveness. The basis for the AXI to JTAG block used in this design is a Xilinx-created IP block. Modifications were necessary to support the unique instruction and data register sizes of the detector. The AXI registers are used to load a sequence of bits to be read out from the TDI and TMS pins to the detector. The register value read out from the detector, TDO, is also captured in an AXI register. This value is used to check the success of a JTAG write operation and is imperative to the successful power-on sequence of the detector.
The CIS2521F controller is a custom AXI peripheral used to control the current state of the detector. This module is responsible for resetting the detector, pausing and resuming detector operation, sequencing the power supplies, and controlling charge transfer in global shutter mode. The IP block has one adjustable parameter, used for adjusting the pulse width of TX1 and TX2 when operating in global shutter mode. The AXI-Lite interface allows the processor to select the current state of sensor operation, which includes off, reset, configuration, and read. The AXI-Lite registers also select the readout mode of the detector, rolling shutter or global shutter.

Once the detector has been configured and is clocking out pixels, the digital measurements must be read back into the FPGA. The data pipeline has been chosen such that it can support the full throughput dictated by the project requirements and is displayed end to end in Figure 18 below. The maximum throughput of each interface is listed where there is additional overhead required. Each of the steps in this pipeline were carefully selected to ensure the necessary bandwidth to operate the detector at 10fps, which is 57Mbps in Rolling Shutter and 114Mbps in Global Shutter.

Figure 18: CSTARS-2 Data Pipeline

The digital signals arrive at the detector at a frequency of 25MHz, with some phase shift resulting from the propagation delay of the cable. If the rising or falling edges of these signals were to
occur during the setup time of a flip flop on the FPGA, potential metastability issues could arise [35].
The signal sync blocks are a simple solution and common solution to this problem. By passing the incoming signals through two shift registers any metastability issues are eliminated early on. The signal that leaves this block still has a clock frequency of 25MHz, but the rising and falling edges are synchronous to the local clock speed. The downside to this implementation is a small input delay of two clock cycles before a signal is updated, a delay that is negligible in this application.

The second stage of the digital signal path is the edge detection block, which plays two important roles. First, it detects falling edges on the output clock from the detector and uses these to capture the current detector output. The falling edge was chosen because of a quirk in the detector operation: the output clock, which is intended for use in synchronizing the changing output data, is not actually synchronous to it. This simple difference causes a host of issues when not considered, as the output data is in an unstable state when the rising edge of the clock arrives. The simplest solution to this problem was to clock the output data on the falling edge instead. The second role of this block is to convert the incoming grey-encoded binary back to standard binary values. To mitigate the computational delay necessary to perform this conversion, a simple lookup table was implemented with all 2048 binary values.

The final stage of the digital signal path, prior to being stored via direct memory access, is the AXI Stream Controller. This custom AXI block receives signals from the processor which tell it when to enable or disable the stream used for direct memory access. Prior to entering the DMA IP block, the detector readout is transmitted as an AXI stream. This protocol is similar in execution to the AXI-Lite protocol used elsewhere, but it has the distinct advantage of a substantially higher throughput. This is necessary to keep up with the output data stream of the detector (57MHz RS, 114MHz GS). Rather than sending individual bus transactions, the AXI-Stream protocol begins and ends under a specific set of conditions, allowing for the continuous transmission of data. To that end, the purpose of the
CIS2521_stream_controller is to enable and disable the AXI-Stream at the beginning and end of each frame. The frame valid signal from the detector is crucial in making the distinction between consecutive frames. It is used with a byte counter to verify that a frame has successfully been read out of the detector. When the stream controller reaches the last byte of the transmission, it uses the TLAST signal to inform the receiving slave. If this signal is not sent, such as the case where the incorrect number of bits are clocked out of the detector, then the DMA transmission is not completed. Prior to entering the DMA block, a small AXI-Stream data FIFO is used to prevent data loss. This buffer compensates for the delay between the enabling of the AXI-Stream, and the start of the DMA transfer.

Direct Memory Access (DMA) is arguably the most important, and the most challenging, part of the data path. The main benefit of DMA as a data transfer method is to minimize processor involvement. The FPGA is allocated a specific region in the memory map, which it then uses to store data. Because the processor is only responsible for starting and stopping the transfer, it can spend more time executing the time-intensive star tracking algorithm. A Xilinx IP block was used to handle the transfer. As mentioned previously, this block receives the detector output in the form of an AXI-Stream. The simplest mode of operation is utilized, where a start address and a byte count are specified. The processor begins the transfer over the AXI-Lite interface. In its final implementation, the DMA will trigger a processor interrupt once the byte count has been reached.

The data pipeline was simulated prior to testing with the actual sensor. A simple sensor output tester was designed to accept the same inputs as the CIS2521 and produce an incrementing value for the pixel measurement. A diagram of this simulation can be found in firmware appendix A2.3. By matching the exact number of pixels as the real detector, this setup was able to verify most of the FPGA data pipeline. The DMA transfer was not included in this simulation, because it requires a Zynq processor to control it. A screenshot of the simulation has been included below, demonstrating the AXI-Stream created by the CIS2521F stream controller. Additional waveforms can be found in appendix A4.2.
The synchronous telemetry stream discussed in the requirements section also required a custom Verilog module. Within the scope and timeframe of this project, a simple interface was created to produce synchronous stream packets. The creation and testing of this block was a collaborative effort with other members of the CSTARS team. After developing an interfacing block, the packet requests sent by the telemetry encoder were simulated. The successful transmission of packets in response to these requests can be seen in the waveform in Figure 20.

### Figure 20: Synchronous Stream Simulation

#### 3.6.2 Processor Development

After developing the various blocks within the programmable logic, the next step was to write code for the dual Arm- Cortex M9 processors to run. The software discussed in this thesis, and included in the project archive, is intended as a demonstration of the detector under operating conditions similar to the actual flight. To demonstrate sensor functionality, the execution speed of the code was not of the utmost importance. For this reason, the code currently being executed is single-threaded, and runs on
one core of the Zynq. These features will likely be necessary for the flight version of the software and
are discussed in detail in the future work section.

The demonstration code, also referred to as the CIS2521 calibration code, performs the
sequencing and setup that is essential to operating the detector. A high-level flow chart of the code can
be seen in Figure 21. The drivers written for the execution of this code will be an important part of the
flight code and have been carefully documented and organized. The full code can be found in firmware
appendix A2.1.

Figure 21: Block Diagram of CIS2521 Calibration Mode Code
Chapter 4: Testing

4.1 Preliminary stages of Testing

Before the detector could be fully characterized, several stages of preliminary testing were necessary to validate the functionality of various parts of the design. This included verification of the power supplies, the JTAG interface, and the clocking and readout of the detector. Additionally, the harnessing was tested in three different stages: a short harness, a long harness, and a long cryogenic harness. The intent was to verify that the detector was operational using ideal connections. Changes to performance would then be observed and measured as the signal integrity degrades over the different harnesses. The design documented above was the result of intensive testing over these various scenarios.

4.2 Cryogenic Testing of the Detector

After the room-temperature operation of the detector was validated, the next step was to test its cryogenic performance at the Center for Detectors at the Rochester Institute of Technology. The focal plane board was mounted into a mechanical assembly designed specifically for the cryostat on-hand. The two figures below demonstrate the mounting configuration and the cryostat with the radiation shield in place.
A telescope was mounted to the front of the cryostat, to focus light onto the surface of the detector. A collimator was mounted to the optical bench, and a small, star-like grouping was used as the light source. Figure 23 below shows the aligned cryostat and collimator.

Figure 22: Focal Plane Assembly mounted to cryostat (Left) and Cryostat with Radiation Shield (Right)

Figure 23: Enclosed Cryostat Aligned with Collimator
The first issue that arose with the pictured setup was caused by the selected telescope lens. Because the focal length of the lens was shorter than predicted, the mechanical setup did not allow for the image to be entirely focused onto the detector. As a result, the images taken within the RIT cryostat appear as a series of out of focus circles. However, these large areas contain only the photons that were produced by the star grouping, verifying that the detector is sensitive enough to detect the individual stars. Figure 24 demonstrates an image captured at room temperature (~300K) using Rolling Shutter mode. The color scale displayed in this figure, and every image that follows, goes from a minimum of blue for the digital number zero, to a maximum of yellow for a digital value of 2047. These digital values correspond to the readout of the detector, converted from grey code to binary.

Figure 24: Baseline CIS2521 Image Captured at 300K using RS mode

After verifying that the detector was still functional inside of the enclosed cryostat, several baseline readings were obtained to determine the room temperature performance of the detector in both RS and GS modes. Once baseline frames were captured, it was time to begin cooling down the cryostat. The cooling process was tedious and resource intensive; due to time constraints, this configuration of the
The cryostat was only fully cooled twice. Images were captured at set intervals to evaluate the changes to detector performance as temperature decreased. The temperature of the setup was monitored via thermal diodes, mounted to the back of the focal plane PCB. This would prove troublesome for the captured results, to be discussed later. An interesting benefit of cooling CMOS detectors, prior to reaching cryogenic temperatures, is a decrease in blemish pixels. These pixels are primarily caused by leakage currents in the photodiode [36], [37] and can be seen to dramatically decrease in the measured frames below roughly 180K.

As the cryostat reached a steady-state temperature, the focal plane board remained at roughly 180K. This is largely due to the detector’s high-power consumption and dissipation, as discussed in the hardware design. To test the full temperature range of the detector, the system was powered down and left overnight. This allowed the detector to fully cool to the ambient cryostat temperature. After being fully cooled, the detector was powered back on, and images were immediately captured. Some of the first cryogenic images are displayed below.

![CIS2521 Rolling Shutter Image Captured using RIT Cryostat](image)

Figure 25: CIS2521 Rolling Shutter Image Captured using RIT Cryostat

(Detector Temperature Approximately 100K)
Additionally, the graph in Figure 27 below show the measured temperature of the detector during continuous operation, when it begins running at cryogenic temperatures.
The digital functions of the detector remained fully functional at temperatures as low as 80K. The sensitivity and readout noise of the detector will be discussed in a later section. An interesting observation can be made when comparing the detector performance in Global Shutter and Rolling Shutter mode. Initial observations seem to indicate that the read noise of the detector increases, while the sensitivity remains consistent. This is supported by the fact that global shutter mode, which subtracts a reset frame from the integrated charge frame. Because of the increase in read noise, the full range of sensitivity decreases in Global Shutter mode, but not in Rolling Shutter, due to its inherently lower read noise. The decrease in dynamic range, and the increased reliability of the lower frequency operation, led to the decision to take the remaining measurements in rolling shutter mode. The specific behavior of the detector at these temperatures is further discussed in the next section.

After proving that the system was operational at the desired temperature, the focal plane assembly was ready for integration with the main CIBER-2 experiment. The purpose of the integration trip was twofold. Firstly, it was important to verify that the detector remained functional after transportation and installation into the CIBER-2 experiment. Secondly, the CIBER-2 team at Caltech was interested in determining the point spread function of the main experimental optics as the temperature decreased. For this reason, it was decided to mount the CSTARS-2 focal plane assembly in the main optical path, using a custom mechanical enclosure. This has been illustrated below in Figure 28.
Figure 28: CIBER-2 Telescope with CSTARS-2 Focal Plane Assembly Installed (Circled in Yellow)

The CIBER-2 telescope was pointed at an electronically adjustable collimator, shown in Figure 29 below. This was crucial in determining the changes to the PSF as temperature decreased.

Figure 29: CIBER-2 Telescope Aligned with Collimator
Similar to the testing performed at RIT, the detector was first tested for functionality at room temperature, and then the temperature was slowly brought down to cryogenic levels. One significant difference between the two setups, however, was the total time required to bring the environment down to cryogenic temperatures. Because of the size of the CIBER-2 experiment, it was necessary to wait almost three full days before the detector approached cryogenic levels. Even then, the detector temperature only reached a steady state of approximately 90K.

One of the most significant changes made prior to the testing done at Caltech was the implementation of the on-die temperature sensor. By reading a purpose-built temperature output from the detector, and storing the information with each captured frame, it was possible to obtain a more accurate reading of the detector temperature during operation. Because of this, the results obtained at Caltech were used for the analysis performed in later sections. A picture obtained with the detector operating at cryogenic temperatures, in the CIBER-2 experiment, is shown below.

Figure 30: Focused Collimator Image Captured at Caltech using CSTARS-2 System
4.3  

**Rocket Integration Testing**

In addition to testing the operation of the detector, it was important to verify that the various interfaces to the experiment worked. The synchronous and asynchronous streams were mostly validated during a trip to the Wallops Flight Facility. The power connections and consumption were validated by plugging the CSTARS-2 system into a flight power supply. The asynchronous stream successfully communicated with the attitude control system and can be considered fully validated. The synchronous stream testing was mostly successful, with some minor issues prevent consistent operation. These remaining issues were later resolved by members of the CTSARS-1 team.
Chapter 5: Results and Discussion

To determine whether the detector remained suitably operational at cryogenic temperatures, it was important to characterize how the performance of the detector changed with decreasing temperature. Briefly mentioned in the background section, the most important metrics used to characterize the detector performance were sensitivity and read noise. Working from the assumption that the detector sensitivity at room temperature is adequate to perform star tracking, relative sensitivity was used to determine by what proportion the sensitivity decreases with temperature. For a given frame, a relatively uniform region was captured, and the average was computed. Secondly, the read noise of the detector is important in determining the maximum possible signal to noise ratio when imaging a star field. If the read noise of the detector is too great, then it becomes impossible to distinguish stars, regardless of the sensitivity. The read noise was calculated using equation (4), and dark frames were captured at various temperatures. This equation is especially important, since fixed pattern noise is ignored through the subtraction of two dark frames. The result is an estimate of the read noise inherent in the detector.

The first experimental setup to be analyzed was the RIT cryostat, with the detector operating in Global Shutter mode. The most valuable data was obtained after letting the detector completely cool down, as this was the lowest achievable temperature in this setup. The average and median detector readouts were calculated for each captured frame, and the result was plotted against its corresponding thermal diode measurement. In the case of the large, uniform readout levels of this setup, median remains a relatively effective measurement of the detector sensitivity. These two trendlines are plotted in Figure 31 below.
Figure 31: Average Detector Readout v. Temperature, Rolling Shutter

Operation within CIBER-2 Experiment (Moving Average Applied)

The most obvious trend that can be observed from this data is the relatively stable readout down to roughly 130K. After that point, the mean value becomes noisier, and begins to taper off. The reasoning behind this trend is made clearer from the sample images in Figure 32 below.

Figure 32: Detector Readout Image Examples, with Increasing Temperature from Left to Right

At first glance, the detector sensitivity was drastically decreased with decreasing temperature. The left-most image in Figure 32 is visibly lower in value than the two images to the right of it. This can
likely be explained by an increase in the read noise of the detector, coupled with the Global Shutter operation. As mentioned previously, Global Shutter operation requires that a reset frame be subtracted from the integrated charge frame. Therefore, an increase in read noise could lead to an apparent decrease in sensitivity. This is further proven through the read noise measurements plotted in Figure 33, alongside the read noise sample images in Figure 34.

Figure 33: Detector Read Noise v. Temperature, Global Shutter Operation within RIT Cryostat

Figure 34: Detector Readout Noise Image Examples, with Increasing Temperature from Left to Right
It is clear from these noise measurements that the read noise of the detector increases to an unacceptable level when operating in Global Shutter mode. It was observed in initial testing, however, that Rolling Shutter operation was a viable alternative that exhibited less read noise. For these reasons, the Caltech measurements were performed by operating the detector in Rolling Shutter mode.

In addition to the low-noise readout of Rolling Shutter mode, the Caltech measurements were more effective at characterizing the detector because of the optical arrangement and the improved temperature measurements. The collimator and telescope lenses were able to correctly focus on the detector, with the collimator being electronically adjustable. This resulted in a highly consistent point-source shining on the detector, which made average readout measurements more reliable. The implementation of the on-die thermal diode measurements allowed for much more precise monitoring of detector temperature, as well as being precisely timed with frame capture. The sensitivity of the detector was evaluated first, shown below in Figures 35 and 36.

Figure 35: Average Detector Readout v. Temperature, Rolling Shutter Operation within CIBER-2 Experiment (Moving Average Applied)
The median detector readout was no longer an effective measure of sensitivity, due to the small number of illuminated pixels. Additionally, the frame capture process was fully automated, resulting in a tenfold increase in the number of captured frames. While good for data analysis, a moving average filter was applied to the data in Figure 35 to better visualize the behavior of the output. With the reduced read noise of the detector operation in Rolling Shutter mode, the sensitivity remains almost entirely constant throughout the roughly 40K range of interest. The variations around 120K and 130K can likely be explained by drift in the light source or optics throwing off the average pixel value slightly. This drift can be seen in the sample detector images in Figure 36, below.

Figure 36: Detector Readout Image Examples, with Increasing Temperature from Left to Right

These measurements confirm that the decrease in sensitivity observed in the RIT cryostat testing was due to the increased read noise of Global Shutter operation. This conclusion is further confirmed by the markedly lower detector read noise that was calculated throughout the temperature range, shown below in Figure 37.
Figure 37: Detector Read Noise v. Temperature, Rolling Shutter Operation within CIBER-2 Experiment

(Moving Average Applied)

Once again, a moving average filter was applied to help visualize the data, and to compensate for the roughly 800 frames of data. While the read noise does increase below 100K, the maximum value is more than an order of magnitude less than what was observed when running with Global Shutter mode. The sample images in Figure 38 have had their color scales adjusted to better visualize the noise pattern.

Figure 38: Detector Readout Noise Image Examples, with Increasing Temperature from Left to Right
Based on the read noise sources identified previously, this could be a result of increased noise in the column amplifier circuit, which is most likely reliant upon BJT-based voltage references. The most important takeaway, though, is that the roughly 50% increase in read noise is not large enough to impact the operation of the detector. Further, due to the self-heating of the detector, it is likely to heat itself into an ideal temperature range within roughly one minute of powering on. Based on the performance of the detector at these two ranges, it is fair to conclude that the performance of the detector is suitable for this star tracking application.
Chapter 6: Conclusions and Future Work

Between the year of development spent on the CSTARS-1 project, and the fourteen months spent developing CSTARS-2, the collective work that has gone into developing a cryogenic CMOS star tracking system is staggering. The progress made by the original CSTARS-1 team laid the foundation for CSTARS-2 by proving that cryogenic CMOS detector operation was feasible. From there, each aspect of the star tracking system was improved upon, resulting in a higher performance, higher reliability system.

The first major milestone of this experiment was the verification that the CIS2521F digital circuitry remained fully functional at cryogenic temperatures. Theoretical research indicated that this would be the case, but its repeatability and consistency increase confidence that system will remain operational for many thermal cycles. Further, the observations and measurements used to characterize the detectors performance indicate that not only is the impact to read noise and sensitivity acceptable, but the self-heating nature of the detector will heat itself to a more favorable operating temperature.

While initial results were used to prove the detectors cryogenic capabilities, there is still work remaining before the overall system is ready for flight. A small number of changes are necessary to the first revision of the focal plane board and the second revision of the interface board. While the hardware delivered to Caltech is sufficient for flight, it still contains a small number of jumper wires. These changes are documented in the CSTARS2 users guide and can be referenced if either more boards need to be assembled, or if the corrections are going to be made to an updated revision.

A considerable amount of work remains on the firmware side of things, where the full star tracking algorithm has yet to be implemented. The delivered software is intended to be a demonstration
of the functionality of the detector, with small changes necessary to support continuous operation. A summary of these changes has also been included within the CSTARS-2 users guide.

Further research into cryogenic sCMOS applications could be performed with minor changes to the focal plane board. The use of a more direct cooling plate to the ceramic packaging of the detector could reduce the effect of self-heating. This would lead to greater confidence in the detector measurements and would better reflect the operating conditions for many deep-space applications. The research done in the process of developing this system was instrumental in advancing the technology readiness level of cryogenic sCMOS detectors. After CIBER-2 completes its first flight, sCMOS will be proven to be a reliable platform for cryogenic imaging applications, especially deep-space applications.
REFERENCES


Appendix A1: Hardware Documentation

The schematics and PCB layouts for the focal plane board and the interface board are listed in the appendices below. These files have also been included in the project archive, if changes are necessary.
A1.1 CSTARS2 Focal Plane Board Hardware Documentation

A1.1.1: CSTARS2 Focal Plane Board Schematic Page 1
A1.1.3: CSTARS2 Focal Plane PCB Mechanical Drawing

(All Dimensions are in Inches)
A1.1.4: CSTARS2 Focal Plane PCB Top Layer
A1.1.5: CSTARS2 Focal Plane PCB Ground Layer
A1.1.6: CSTARS2 Focal Plane PCB Power Layer
A1.1.7: CSTARS2 Focal Plane PCB Bottom Layer
A1.2: CSTARS2 Interface Board Hardware Documentation

A1.2.1: CSTARS2 Focal Plane Board Hardware Documentation
A1.2.9: CSTARS2 Interface Board Revision B PCB Mechanical Drawing

(All Dimensions in Inches)
A1.2.10: CSTARS2 Interface Board Revision B PCB Top Layer
A1.2.11: CSTARS2 Interface Board Revision B PCB Ground Layer
A1.2.12: CSTARS2 Interface Board Revision B PCB Power Layer
A1.2.13: CSTARS2 Interface Board Revision B PCB Bottom Layout
Appendix A2: Firmware Documentation

The following appendices contain block diagrams describing the firmware run on the MicroZed, in addition to some critical pieces of code from the design. These are only intended as a surface level reference into the operation of the program. If changes need to be made, or more detailed information is necessary, the full Vivado project can be found within the project archive.
/* CSTARS-2 Detector Calibration Code
 * Ben Stewart
 * July 12th, 2018
 *
 * This code is used to capture images with the CIS2521
 * detector and store them as *.bin files on the SD-Card
 *
 * ---------------
 * | UART TYPE | BAUD RATE |
 * ---------------
 *
 * Open a serial terminal at the following speed to begin
 * communication with CSTARS2 interface board
 *
 * ps7_uart 115200 (configured by bootrom/bsp)
 */

#include "ciber2_platform.h"

XGpioPs PS_Gpio;
XAxiDma AxiDma;
XScuTimer Timer;
XAdcPs XAdc;

char imageDataBufferPtr = (char *) IMGS_DATA_BASE_ADDR; // Memory space dedicated for image DMA transfer

FIL fil; // File object
FATFS fatfs;
FRESULT Res;
TCHAR *Path = "0:/";

char dataFileNameStr[256];
int fileCount;
uint8 pauseReadout = 0;

int main()
{
    int Status;
    PS_GpioConfig(&PS_Gpio);
    init_platform();

    PS_GpioOutput(&PS_Gpio, MIO_TEST1_LED, LOW);
    PS_GpioOutput(&PS_Gpio, MIO_TEST2_LED, LOW);

    xil_printf("CSTARS2 Detector Calibration Mode\r\n");
    xil_printf("Last updated July 12th, 2018 by Ben Stewart\r\n");
    xil_printf("using Xilinx SDK version 2017.4\r\n\n");

    longDelay();
    xil_Out32(AXI_CIS2521F_CTRL_BT_BASE + SENSOR_STATE_OFFSET, RESET_STATE);
    longDelay();
    xil_Out32(AXI_CIS2521F_CTRL_BT_BASE + SENSOR_STATE_OFFSET, CFG_STATE);
    longDelay();

    xil_printf("\nConfiguring JTAG Registers\r\n");

    JTAG_LoadAndVerify(sensorBT, 0x08, 0x0000000020, &PS_Gpio); // Sets Region of Interest 1 (Pre-Scan Region);
JTAG_LoadAndVerify(sensorBT, 0x02, 0x01263FDE, &PS_Gpio); // Enables rolling shutter operation

Xil_Out32((AXI_CIS2521F_CTRL_BT_BASE + SENSOR_STATE_OFFSET, (READ_STATE | ROLLING_SHUTTER)))
//print("CTRL state changed to READ \n\r");
longDelay();
XAxidma_Setup(&AxiDma);
XAdc_Setup(&XAdc);

xil_printf("\nMounting the SD card. This may take a minute...\r\n");
Res = f_mount(&fatfs, Path, 0);
if (Res != FR_OK) {
  xil_printf("ERROR: SD MOUNT FAILURE \n\r");
  return XST_FAILURE;
}
xil_printf("\r\nPress pushbutton to begin capture\n\r");
WaitForButton(&PS_Gpio);

while(1){
  // These delays are artifically inserted to extend the interval between captures.
  // They can be removed, or additional ones can be added.
  longDelay();
  longDelay();
  longDelay();
  longDelay();
  longDelay();
  xil_printf("Starting DMA transfer\n\r");
  // Once the frame start has been detected, the DMA transfer begins
  Status = XAxidma_SimpleTransfer(&AxiDma, (UINTPTR) imageDataBufferPtr, IMG_BYTE_LEN, XAXIDMA_DEVICE_TO_DMA);
  Xil_Out32((AXI_CIS2521F_STREAM_CONTROLLER_BT_BASE + STREAM_CONTROL_OFFSET, (ENABLE_STREAM | ROLLING_SHUTTER)))
  xil_printf("%d\n", (u16)Xil_In32((AXI_CIS2521F_STREAM_CONTROLLER_BT_BASE + STREAM_CONTROL_OFFSET)));
  xil_printf("Stream Enabled\n\r");
  // This first loop waits for the stream state to enter the 'WAIT FOR NEXT FRAME' state
  while(Xil_In32((AXI_CIS2521F_STREAM_CONTROLLER_BT_BASE + STREAM_STATE_OFFSET) == 0));
  Xil_Out32((AXI_CIS2521F_STREAM_CONTROLLER_BT_BASE + STREAM_CONTROL_OFFSET, (DISABLE_STREAM | ROLLING_SHUTTER)))
  //xil_printf("%d\n", (u16)Xil_In32((AXI_CIS2521F_STREAM_CONTROLLER_BT_BASE + STREAM_CONTROL_OFFSET)));
  while(XAxidma_Busy(&AxiDma, XAXIDMA_DEVICE_TO_DMA));
  xil_printf("DMA transfer of length %u \r\n", Xil_In32(XPAR_AXI_DMA_0_BASEADDR + 0x58));
  Xil_DCacheInvalidateRange((UINTPTR) imageDataBufferPtr, IMG_BYTE_LEN);
  //Reads all temp channels, stores result with image
  XAdc_Read_All_Temps(&XAdc);
xil_printf("Saving File %d Now\n", fileCount);

UINT numBytesWritten = 0;

// Each file is zero padded so that each image has a total of four digits
// ex: 0001, 0002, 0003

if(fileCount<10){
    sprintf(dataFileNameStr, "D00%d.bin", fileCount);
} else if(fileCount<100){
    sprintf(dataFileNameStr, "D0%d.bin", fileCount);
} else if(fileCount<1000){
    sprintf(dataFileNameStr, "D%d.bin", fileCount);
} else {
    sprintf(dataFileNameStr, "D%d.bin", fileCount);
}

fileCount++;

// Save file to the SD card

Res = f_open(&fil, dataFileNameStr, FA_CREATE_ALWAYS | FA_WRITE | FA_READ);
if (Res != FR_OK) {
    xil_printf("ERROR: SD MOUNT FAILURE 1\n");
    return XST_FAILURE;
}

Res = f_lseek(&fil, 0);
if (Res != FR_OK) {
    xil_printf("ERROR: SD MOUNT FAILURE 2\n");
    return XST_FAILURE;
}

Res = f_write(&fil, imageDataBufferPtr, IMG_BYTE_LEN, &numBytesWritten);
if (Res != FR_OK) {
    xil_printf("ERROR: SD MOUNT FAILURE 3\n");
    return XST_FAILURE;
}

Res = f_close(&fil);
if (Res != FR_OK) {
    xil_printf("ERROR: SD MOUNT FAILURE 4\n");
    return XST_FAILURE;
}

xil_printf("File Saved \n");

cleanup_platform();
return 0;
A2.2: CSTARS-2 Detector Calibration Block Diagram
A2.3: CIS2521 Detector Simulation Block Diagram
A2.5: CIS2521 Controller IP

A2.5.1 CIS2521F Controller Block Diagram Module

```
module cis2521f_controller_BT (#
    parameter integer TX_PULSE_WIDTH = 101)
#

// Inputs FROM AXI Bus
input wire clk_60, // input clock frequency
input wire resetn, // active low module reset
input wire [1:0] sensorControlState, // active high sensor config setting
input wire readoutModeSelect, // Controls global or rolling shutter operation

// Signals FROM Sensor
input wire chargeTrans,
input wire frameValid, // Frame valid output signal
input wire lineValid, // Line valid output signal
//input wire [10:0] dataOUT, // Data output from sensor pixels

// Signals TO Sensor
```

A2.5.2 CIS2521F Controller State Machine Verilog Code

```
`timescale 1ns / 1ps

/////////////////////////////////////////////////////////////////////////////
// CIS2521F State Machine Logic v3.0
// Ben Stewart
// The purpose of this block, in conjunction with an AXI slave interface, is to
// pause and resume sensor readout. This code MUST be used with an AXI interface.
/////////////////////////////////////////////////////////////////////////////

module cis2521f_state_machine_logic #
(
    parameter integer TX_PULSE_WIDTH = 101)
#

// Inputs FROM AXI Bus
input wire clk_60, // input clock frequency
input wire resetn, // active low module reset
input wire [1:0] sensorControlState, // active high sensor config setting
input wire readoutModeSelect, // Controls global or rolling shutter operation

// Signals FROM Sensor
input wire chargeTrans,
input wire frameValid, // Frame valid output signal
input wire lineValid, // Line valid output signal
//input wire [10:0] dataOUT, // Data output from sensor pixels

// Signals TO Sensor
```
output reg sensorResetB, // Active low sensor reset
output reg enableDVDD, enableAVDD, // Active high digital /
// analog sensor power enable
output wire sCLK, // Sensor Clock
output reg TX1, TX2; // Charge transfer controls
output reg dataSEL; // Switches programmable wavetables for sensor
output reg read;

); // Local Variables
reg [7:0] sCLKCount = 0;
reg [7:0] TX1PulseCount, TX2PulseCount;
reg sensorReadState;
reg startofFrame;

// Local Parameters
parameter OFF_STATE = 0;
parameter RESET_STATE = 1;
parameter CFG_STATE = 2;
parameter READ_STATE = 3;

parameter DATA_FRAME = 0;
parameter RESET_FRAME = 1;

// ------------------ CIS2521F Sensor Control State Machine ------------------
assign sCLK = clk_60;
always @(posedge clk_60) begin
    if (!resetn) begin
        enableDVDD = 0;
        enableAVDD = 0;
        TX1 = 0;
        TX2 = 0;
        TX1PulseCount = 0;
        TX2PulseCount = 0;
        dataSEL = 0;
        read = 0;
        startofFrame = 0;
        sensorResetB = 1;
        sensorReadState = RESET_FRAME;
    end
    else case (sensorControlState)

        OFF_STATE : begin // Prior to JTAG configuration, the sensor is
            // completely powered down.
            enableDVDD = 0;
            enableAVDD = 0;
            TX1PulseCount = 0;
            TX2PulseCount = 0;
            dataSEL = 0;
            read = 0;
            sensorResetB = 0;
        end

        RESET_STATE : begin
            enableDVDD = 1;
            enableAVDD = 0;
            TX1PulseCount = 0;
            TX2PulseCount = 0;
            dataSEL = 0;
            read = 0;
            sensorResetB = 0;

end
CFG_STATE : begin // The CFG_STATE should be enabled prior to JTAG
  // register configuration
  enableDVDD = 1;
  enableAVDD = 0;
  TX1PulseCount = 0;
  TX2PulseCount = 0;
  dataSEL = 0;
  read = 0;
  sensorResetB = 1;
end

READ_STATE : begin // Sensor is currently being clocked in Global
  // Shutter mode.
  enableDVDD = 1;
  enableAVDD = 1;
  read = 1;
  sensorResetB = 1;

  if(readoutModeSelect) begin // If readoutModeSelect == 1, then
    // Global Shutter operation is enabled,
    // begin clocking data select, TX1, and
    // TX2.
    if(!frameValid & !startofFrame) begin // When frameValid is
      // low, the sensor is in the
      // pre-scan period
        case (sensorReadState)
          DATA_FRAME : begin
            TX1PulseCount = TX_PULSE_WIDTH;
            startofFrame = 0;
          end

          RESET_FRAME : begin
            TX2PulseCount = TX_PULSE_WIDTH;
            startofFrame = 0;
          end

        endcase
    end

  else if(frameValid & !startofFrame) begin
    startofFrame = 1;
    sensorReadState = !sensorReadState;
  end

  case (TX1PulseCount)
    1 : begin
      TX1 = 0;
      dataSEL = 1;
      TX1PulseCount = TX1PulseCount - 1;
    end

    0 : TX1 = 0;

    default : begin
      TX1 = 1;
      TX1PulseCount = TX1PulseCount - 1;
    end
endcase

case (TX2PulseCount)

1 : begin
    TX2 = 0;
    dataSEL = 0;
    TX2PulseCount = TX2PulseCount - 1;
end

0 : TX2 = 0;

default : begin
    TX2 = 1;
    TX2PulseCount = TX2PulseCount - 1;
end

endcase

default : begin
    endcase
end

endcase

end

endmodule
A2.6: CIS2521F Axi Stream Controller IP

A2.6.1: CIS2521F Axi Stream Controller Block Diagram Module

A2.6.2: CIS2521F Axi Stream Controller Verilog Code

`timescale 1ns / 1ps

// AXI STREAM Controller
// Ben Stewart
// July 2018
// Overview: Clocks pixel measurements from the CIS2521F sensor, and generates an AXI stream
for the clocked out pixels. When global shutter mode is enabled, a reset and
data frame are read out concurrently. When rolling shutter mode is
enabled, only a data frame is read out

module cis2521f_axi_stream_controller #
(  
  parameter integer C_M_AXIS_TDATA_WIDTH = 32,
  parameter integer PIXEL_COUNT = 2840832
//parameter integer PIXEL_COUNT = 2764800

// ----------------- EXPLANATION OF ACTIVE REGION & TOTAL PIXEL COUNT -----------------
//
// 1080 active rows, 8 optically dark, and 8 electrically dark form total the number of
active lines (1096)
// 2560 active columns and 32 optically dark columns form the total number of active columns
// (2592)
//
// While FVAL is high, the total number of pixels that will be clocked out of the sensor is
1096 x 2592 = 2,840,832 pixels
//


While FVAL is low, the sensor is clocking virtual rows of pixels, which are NOT measured.)

```vhdl
input wire clk_100,
input wire clkOUT,
input wire resetn,
input wire frameValid,
input wire dataSelect,
input wire streamEnable,
input wire readoutModeSelect,
input wire [10:0] dataOUT,
output reg [1:1] streamState,
output reg [31:0] totalPixelCount,
output reg M_AXIS_TVALID,
output reg M_AXIS_TLAST,
output reg [C_M_AXIS_TDATA_WIDTH-1 : 0] M_AXIS_TDATA
);
```

-- Cis2521f Sensor Output AxI Stream -----------------------------------

```vhdl
reg dataPosition; // Indicates whether the next pixel value is packed in the upper or lower two-bytes of the AXIS_DATA line
reg nextPixelCapture; // Indicates whether or not the next dataOUT is ready for capture
reg [31:0] pixelCounter; // Counts the total number of pixels in the current frame
reg [31:0] dataTemp;
reg frameLock; // Used in global shutter mode to guarantee consecutive frames are read

// Define the AXI Stream states
parameter STREAM_IDLE = 2'b00;
parameter STREAM_RUN_RESET_FRAME = 2'b01;
parameter STREAM_RUN_DATA_FRAME = 2'b10;

parameter UPPER_HALF = 1'b1;
parameter LOWER_HALF = 1'b0;

parameter GLOBAL_SHUTTER = 1'b1;
parameter ROLLING_SHUTTER = 1'b0;

always @(posedge clk_100) begin
    if (!resetn) begin
        M_AXIS_TVALID = 0;
        M_AXIS_TLAST = 0;
        M_AXIS_TDATA [C_M_AXIS_TDATA_WIDTH-1 : 0] = 0;
        streamState = STREAM_IDLE;
        dataPosition = LOWER_HALF;
        nextPixelCapture = 1;
        dataTemp = 0;
        pixelCounter = 0;
        totalPixelCount = 0;
        frameLock = 0;
    end
    else if(readoutModeSelect == ROLLING_SHUTTER) begin // If rolling shutter operation is selected, enabling the stream will continuously
        // read out data frames
            case(streamState)
                STREAM_IDE : begin // Idle State, axi stream is waiting to resume readout
                    M_AXIS_TVALID = 0;
                    M_AXIS_TLAST = 0;
                    M_AXIS_TDATA [C_M_AXIS_TDATA_WIDTH-1 : 0] = 0;
```
if(!frameValid & streamEnable) begin  // This specific combination
  // guarantees the complete readout of a
  // data frame.
  streamState = STREAM_RUN_DATA_FRAME;
end
else
  streamState = STREAM_IDLE;
end

STREAM_RUN_DATA_FRAME : begin
  if(clkOUT & nextPixelCapture & frameValid) begin
    if(dataPosition == LOWER_HALF) begin  // Data position is
      // used to pack two pixels of
      // information into each four-
      // byte AXIS transaction
        dataTemp[15:0] = dataOUT;
        dataPosition = UPPER_HALF;
      end
    else begin
      dataPosition = LOWER_HALF;
      if(pixelCounter == PIXEL_COUNT - 2) begin  // Max
        pixel readout count has been reached
        M_AXIS_TLAST = 1;
        totalPixelCount = totalPixelCount +
        pixelCounter;
        pixelCounter = 0;
        streamState = STREAM_IDLE;  // Switch
        the STREAM_STATE back to IDLE
      end
      else begin
        pixelCounter = pixelCounter + 2;
        M_AXIS_TLAST = 0;
      end
      M_AXIS_TVALID = 1;
      M_AXIS_TDATA [C_M_AXIS_TDATA_WIDTH-1 : 16] = dataOUT;
      M_AXIS_TDATA [15 : 0] = dataTemp;
    end
  end
  nextPixelCapture = 0;
else if(!clkOUT) begin
  nextPixelCapture = 1;  // Prepare to capture next pixel
  value
  M_AXIS_TVALID = 0;
  M_AXIS_TLAST = 0;
  M_AXIS_TDATA [C_M_AXIS_TDATA_WIDTH-1 : 0] = 0;
end
else if(readoutModeSelect == GLOBAL_SHUTTER) begin  // If global shutter operation is
  // selected, reset and data frames are
  // read out of the detector
case(streamState)

STREAM_IDLE : begin  // Idle State, axi stream is waiting to resume
    M_AXIS_TVALID = 0;  // necessary for capturing the reset and data frames
    M_AXIS_TLAST = 0;
    M_AXIS_TDATA [C_M_AXIS_TDATA_WIDTH-1 : 0] = 0;
    if(!frameValid & streamEnable & dataSelect) begin  // This specific combination guarantees the complete readout of a reset frame and its corresponding data frame.
        totalPixelCount = 0;
        frameLock = 1;
    end
    if(!frameValid & streamEnable & !dataSelect & frameLock) begin
        totalPixelCount = 0;  // and its corresponding data frame.
        frameLock = 0;
        streamState = STREAM_RUN_RESET_FRAME;
    end
    else
        streamState = STREAM_IDLE;
end

STREAM_RUN_RESET_FRAME, STREAM_RUN_DATA_FRAME : begin  // These states indicate that the stream is currently running
    if(clkOUT & nextPixelCapture & frameValid) begin
        if(dataPosition == LOWER_HALF) begin  // Data position is used to pack two pixels of information into each four-byte AXIS transaction
            dataTemp[15:0] = dataOUT;
            dataPosition = UPPER_HALF;
        end
        else begin
            dataPosition = LOWER_HALF;
            if(pixelCounter == PIXEL_COUNT - 2) begin  // Max pixel readout count has been reached
                M_AXIS_TLAST = 1;
                totalPixelCount = totalPixelCount + pixelCounter;
                pixelCounter = 0;
            endcase
            if(streamState == STREAM_RUN_RESET_FRAME) streamState = STREAM_RUN_DATA_FRAME
            else streamState = STREAM_IDLE;
        end
    endcase
else begin
    pixelCounter = pixelCounter + 2;
    M_AXIS_TLAST = 0;
end

M_AXIS_TVALID = 1;
M_AXIS_TDATA [C_M_AXIS_TDATA_WIDTH-1 : 16] = dataOUT;
M_AXIS_TDATA [15 : 0] = dataTemp;
end

nextPixelCapture = 0;
end

else if(!clkOUT) begin
    nextPixelCapture = 1; // Prepare to capture next
    // pixel value
    M_AXIS_TVALID = 0;
    M_AXIS_TLAST = 0;
    M_AXIS_TDATA [C_M_AXIS_TDATA_WIDTH-1 : 0] = 0;
end
endcase
end
endmodule
Appendix A3: Software Documentation

The following appendix contains one of the MATLAB scripts used to display images saved by the CSTARS2 detector. All of the MATLAB code utilized, in displaying and processing the captured data, can be found in the project archive.
A3.1 MATLAB Code for Displaying Captured Images

% CSTARS2 Binary file read script
% July 12, 2017
% Ben Stewart
% This code cycles through all of the binary image files in the current directory, and displays them
% in a 2048 (11-bit) color scale. The temperature of the detector, readout as a voltage from the chip itself, is also converted and displayed on the image. These values are contained within the first five pixels of the read image.

close all

fileCount = 0;
while fileCount < 20
    fileName = sprintf('D%04i.BIN', fileCount) %Binary file should be formatted as 'D0000.BIN'
    fileID = fopen(fileName);
    dataFrame = fread(fileID, [2875904, 1], 'uint16');

    %Conversion left unsimplified for clarity
detectorTemp = (dataFrame(1)/65563); %Convert raw ADC value to voltage
    detectorTemp = detectorTemp*2.5; %Compensate for voltage division
    detectorTemp = (detectorTemp*158.75)-46.29; %Apply linear fit to approximate temperature
    %Rough calibration performed 7/3/2018, using thermal diode mounted onto the back of the detector. Uncertainty is +/- 2K
    % --- Thermal diode channel readout conversion has been included ---
    % Conversion left unsimplified for clarity
    tempCh1 = (dataFrame(2)/65563); %Convert raw ADC value to voltage
    tempCh1 = (tempCh1*-640.41)+578.6; %Apply linear fit to approximate temperature
    % Conversion left unsimplified for clarity
    tempCh2 = (dataFrame(3)/65563); %Convert raw ADC value to voltage
    tempCh2 = (tempCh2*-634.5)+570.6; %Apply linear fit to approximate temperature
    % Conversion left unsimplified for clarity
    tempCh3 = (dataFrame(4)/65563); %Convert raw ADC value to voltage
    tempCh3 = (tempCh3*-634.5)+570.6; %Apply linear fit to approximate temperature
    % Conversion left unsimplified for clarity
    tempCh4 = (dataFrame(5)/65563); %Convert raw ADC value to voltage
    tempCh4 = (tempCh4*-634.5)+570.6; %Apply linear fit to approximate temperature

    if (detectorTemp > 330) || (detectorTemp < 70)
        detectorTemp = 'INVALID DETECTOR TEMP';
    else
        detectorTemp = num2str(detectorTemp, 5);
        detectorTemp = ['Detector Temp: ' detectorTemp 'K'];
    end

    dataFrameMatrix = reshape(dataFrame, [2624,1096]);
    dataFrameMatrix = transpose(dataFrameMatrix);

    figure('Name', ['Frame ' num2str(fileCount)], 'units','normalized','outerposition',[0 0 1 1])
    imagesc(dataFrameMatrix);
    colorbar;
rectangle('Position', [25 25 10 50], 'FaceColor','white','EdgeColor','b',
'LineWidth',3);
text(50,50, detectorTemp, 'Color', 'red', 'FontSize', 14);
% text(50,100, tempCh1, 'FontSize', 14);
% text(50,150, tempCh2, 'FontSize', 14);
% text(50,200, tempCh3, 'FontSize', 14);
% text(50,250, tempCh4, 'FontSize', 14);

% Labels to orient captured image
text(-100,700, 'LEFT', 'FontSize', 14, 'Rotation', 90);
text(1200,-25, 'TOP', 'FontSize', 14);
caxis([0 2048]);

% Change this increment to skip frames, speeding up runtime of code
fileCount = fileCount + 1;
end