PROCESS DEVELOPMENT OF MULTILEVEL METALLIZATION UTILIZING NATIONAL SEMICONDUCTOR POLYIMIDE EL-5510

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ABSTRACT

This project is concerned with double-layer metal using National Polyimide EL-5500 as the of an aluminum /dielectric/ aluminum scheme. The polyimide was an attractive candidate for the dielectric die to its use in trilayer resist schemes. However, results obtained showed incomplete via clear-out.

INTRODUCTION

The use of multilevel metallization is common in VLSI fabrication to overcome the limitations encountered with single level metal. The need for more than a single metal layer is evident in circuit performance characteristics. A significant limitation on the switching speed comes from the propagation delay of fine-line interconnects placed on an insulating film [1-3]. The relationship between the delay time, RC, is seen to be directly proportional to the square of the interconnect length, as shown in the following equation:

$$RC = (Rs \times (L^2) \times Eox)/Xox$$

where, Rs and L are the sheet resistance and length of the interconnect line; Eox and Xox are the dielectric constant and the thickness of the insulating film, respectively. The length of the interconnect line must be minimized, to obtain desired device performance. Thus chip size and switching speeds are essentially limited by the interconnect network of VLSI devices.

The microelectronic engineering department at RIT has conducted several preliminary investigations of aluminum /dielectric/aluminum multilevel metallization schemes. A brief critique of procedures and results is in order, followed by a statement on this project.

The project by Chris Knaus [4] concentrated on using a DuPont photosensitive polyimide as the dielectric between the two metal layers. His study found that during the development and a subsequent O2 plasma etch of the photosensitive polyimide for the vias, that insufficient clean out and possibly Al-oxide formation caused very high contact resistance. After a dc voltage of 2-36 volts a dielectric breakdown in the via occurred and low contact resistance was observed. O2 plasma processes, overdevelopment

and a buffered hf dip were tried with little success resulting in high contact resistance.

Eric Westerhoff's project [5] extended the above work and considered SOG, photoresists Kodak 820 and Shipley 1400-27, and thermally deposited silicon monoxide for the dielectric. Test features that he used were via chain resistance, step coverage, capacitance, and electrical interference. Upon repeating for photosensitive polyimide, he found that development specs by Knaus were less than adequate, mainly due to the use of the same container of polyimide as Knaus used. Increasing the dose and a longer development time also produced a poor image. Attributed cause was the polyimide was over 1 year old. For resist as a dielectric between the metal layers, it was found that the resist could not stand up to 2nd metal imaging in adhesion. SiO could not be evaporated with the vacuum system at RIT and thus was not tested. For the SOG, he found it to be a good planarization layer but no further accomplishment with it is noted.

The project done by Robert Newcomb [6] consisted of trying to characterize SOG by breakdown voltage vs. dielectric thickness. He also obtained very high via resistance which he attributed to the fact that he did not have oxide insulation between first metal and the substrate. The breakdown voltage results properly showed increasing voltage for increasing dielectric thickness.

Manuel Carneiro's project [7] attempted characterization of both polyimide and SOG as the dielectric. The SOG attempt failed due to severe underetching of the vias. The polyimide processing resulted in good breakdown characteristics but very high via contact resistance. In Manny's design he experimentally tried different size vias for the via chains and also attempted results from various thicknesses of the dielectric.

This project proposed to try to resolve the high via contact resistance utilizing National Semiconductor polymide EL-5510 as a dielectric. The major cause of the high contact resistance is due to incomplete via clean-out [4-7]. Incomplete via cleanout can be due to many factors [8], such as: Polyimide reflow, insufficient etching, polyimide scum formation and aluminum oxide growth. Figure 1 shows results of an open and short circuit due to improper via etching. An open circuit is seen when the via is insufficiently cleared-out, whereas a short circuit is seen when the dielectric is overetched causing undesirable contact between metal layers. The dielectric used, polyimide EL-5510 series was chosen for its superior characteristics over other polyimides and the fact that it is well documented at RIT.

EXPERIMENTAL

The process sequence shall be presented in abbreviated form, where the complete process flow is given in Appendix A. The same process mask set from the previous study by Manny

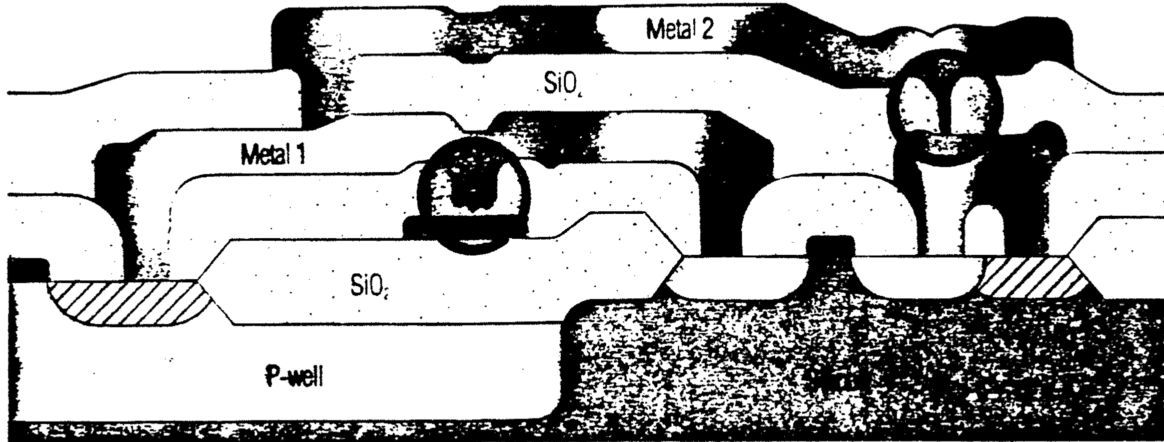

FIGURE 1: An open circuit and short circuit due to improper via etching

Carneiro were used. This mask set could only be successfully aligned for two rows of die due to intial mask generation on the GCA photo-repeater caused differing spaces between die. The mask set contained various via dimensions and capacitor areas. As such, hopes that the larger vias of 30 microns would be cleared out sufficiently to enable proper metal to metal interconnect, and analysis as to the lowest via size obtainable could be realized.

Different areas of processing touched upon included: utilizing an aluminum/silicon alloy metal for 1st and 2nd metallization, a buffered HF dip prior to 2nd metal deposition, an aluminum etchant dip to remove aluminum oxide from the via, and an argon sputter prior to 2nd metal deposition to attempt enough damage in the via to breakthrough to the 1st metal layer.

Intial processing of five wafers showed adhesion problems of the alloyed metal after two weeks from deposition. The photoresist lifted during aluminum etching and etched away desired aluminum. Upon rework only three wafers were processed to completion for parameter testing.

The processed wafers were subsequently tested using the HP-parameter analyzer for measurement of via resistance, capacitance value and dielectric breakdown.

RESULTS

Problems with resist adhesion to the metal layers occurred beyond a week from deposition. This strongly suggests trying to do the entire processes between 1st and 2nd metallization within the shortest time span possible. This will provide the best potential for metal to metal connection.

Etching of the vias using the plasma ash process involved a "trial and error" approach, where visual inspection with an optical microscope was not capable of detecting complete via etch. Polyimide coated silicon wafers, which were flat with no metal, were used to determine the etch rates of the polyimide in the plasma asher. Application of these etch rates to processing via etch led to incomplete clean out in many cases. Complete clear out could not be detected with microscope inspection, but showed up as opens in electrical test. This would suggest creating a program on the nanospec for polyimide on metal such that it could be used to analyze via clean out.

The test structures for measuring capacitors [4-7] consisted of various dimensions of vias and capacitor sizes. Upon testing capacitance, poor data was obtained due to bad connection through the via of the 1st metal structure to the 2nd metal pad. Also, the test masks limited the number of die aligned properly due to mask error during manufacture on the GCA photo-repeater.

Several recommendations to address or possibly fix these issues exist. Future test masks should include various via dimensions as in the case of Manny Carneiro's study and also should include via clean-out detection structures to enable comprehensive analysis into the capacity of etching through the via. Formulation of a program on the nanospec for determining polyimide thickness on a metal layer would enable inspection for complete via clear out of device wafers. Also, a SEM study of via clean out utilizing dielectric on 1st metal could enable determination of an optimal etch process, including etch time, to clear out the vias. Planarization and step coverage examinations would study the capabilities of the materials to reduce hillock formation, opens and short circuits. Lastly, investigations into silicides or barrier metals including refractory metals could resolve the metal to metal contact problem.

CONCLUSIONS

This study showed that incomplete via clean out caused insufficient contact between the two metal layers. However, the superior characteristics and well defined process for the polyimide make it a potentially useful dielectric material for a multilevel process. Continued investigations should follow to try to resolve the via clean out with the polyimide EL-5510.

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