The Influence of Alternative Electrode Configurations and Process Integration Schemes on IGZO TFT Operation

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ELI P. POWELL
August 2, 2017

A Thesis Submitted in Partial Fulfillment of the Requirements for the Degree of Master of Science in Microelectronic Engineering

R·I·T | KATE GLEASON
College of ENGINEERING

Department of Electrical and Microelectronic Engineering
The Influence of Alternative Electrode Configurations and Process Integration Schemes on IGZO TFT Operation

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I dedicate this work to my father, Dr. Saul R. Powell, without whom I would not be where I am today. He may not be with us today but his legacy lives on through the hearts and minds of all those that he touched. Thank you for everything you’ve done for me and know that I will always appreciate and love you. May you rest in peace and continue to watch over everyone.
Abstract

Amorphous oxide semiconductors (AOS) have been extensively studied for their application in thin-film electronics; an area which is currently dominated by hydrogenated amorphous silicon (a Si:H) technology. Indium-gallium-zinc oxide (IGZO) has garnered most of the AOS materials focus due to its high carrier mobility and process simplicity. When modifying an existing process flow for fabrication of TFTs, the effect of each modification on the electrical characteristics must be determined. The compatibility of the process with the constraints of a glass substrate must also be considered. A new test chip layout was created that enables the fabrication of TFTs with a variety of electrode configurations including top-gate, bottom-gate, double-gate, and either staggered or co-planar source/drain regions. TFTs were fabricated on glass and oxidized silicon substrates, consisting of sputter-deposited IGZO surrounded by SiO2 dielectric layers, an oxidizing ambient anneal treatment, and a capping layer deposited by atomic layer deposition (ALD). Electrical characteristics from each process treatment and gate configuration were compared, with some noted differences in device operation related to process integration. A SPICE level 2 compatible IGZO TFT model was developed, with extracted parameter values providing quantitative measures for comparison.
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<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
<th>Units/Value</th>
</tr>
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<tbody>
<tr>
<td>(C'_{ox})</td>
<td>Oxide capacitance per unit area</td>
<td>F/cm²</td>
</tr>
<tr>
<td>(E_g)</td>
<td>Band gap energy</td>
<td>eV</td>
</tr>
<tr>
<td>(E_{OV})</td>
<td>Energy of oxygen vacancies</td>
<td>eV</td>
</tr>
<tr>
<td>(g_m)</td>
<td>Transconductance</td>
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<td>(I_D)</td>
<td>Drain current</td>
<td>A</td>
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<tr>
<td>(L)</td>
<td>Channel length</td>
<td>μm</td>
</tr>
<tr>
<td>(N_{OV})</td>
<td>Energy density of oxygen vacancies</td>
<td>cm⁻³ eV⁻¹</td>
</tr>
<tr>
<td>(N_{TA})</td>
<td>Energy density of acceptor-like tail-states</td>
<td>cm⁻³ eV⁻¹</td>
</tr>
<tr>
<td>(N_{TD})</td>
<td>Energy density of donor-like tail-states</td>
<td>cm⁻³ eV⁻¹</td>
</tr>
<tr>
<td>(R_{SD})</td>
<td>Source/Drain series resistance</td>
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<td>Subthreshold swing</td>
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<td>(V_{DS})</td>
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<td>Width of acceptor-like tail-states (gaussian distribution)</td>
<td>eV</td>
</tr>
<tr>
<td>(W_{TD})</td>
<td>Width of donor-like tail-states (gaussian distribution)</td>
<td>eV</td>
</tr>
<tr>
<td>(\chi)</td>
<td>Electron affinity</td>
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<tr>
<td>(\varepsilon_{IGZO})</td>
<td>Relative permittivity of IGZO</td>
<td></td>
</tr>
<tr>
<td>(\Delta V_G)</td>
<td>Sub-threshold separation</td>
<td>V</td>
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<td>(\mu_0)</td>
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<tr>
<td>(\mu_0)</td>
<td>Effective electron mobility</td>
<td>cm²/Vs</td>
</tr>
<tr>
<td>(\mu_{TH})</td>
<td>Threshold mobility</td>
<td>cm²/Vs</td>
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<tr>
<td>(\theta)</td>
<td>Mobility modulation</td>
<td>V⁻¹</td>
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1.1 Background

Prior to the development of active-matrix LCDs (AM-LCDs) the passive-matrix was the standard for LCDs. In a passive matrix LCD, a grid is created by using one glass substrate to address the rows and the other substrate to address the columns. In order to turn on a pixel, a voltage signal is sent to the corresponding column and the respective row is grounded to complete the circuit. However, direct addressing of the pixel has two major drawbacks; slow response time and poor voltage control. Also, when directly addressing a pixel a leakage path is present that allows adjacent pixels to be turned on. On the other hand, an active matrix LCD addresses the pixel through a transistor which eliminates the leakage paths. As such, AM-LCDs have dominated the display industry. An example of a simple active-matrix circuit can be seen in Fig. 1.1 which consists of a switching Thin-Film Transistor (TFT), storage capacitor, and liquid crystal.

In order for a pixel to be turned on in an AM-LCD there must be an appropriate voltage applied to the data line and the pixel must be addressed through the scan line. Once the storage capacitor has fully charged the scan line is disconnected, thus the pixel is no longer addressed, and the TFT is turned off. Voltage is maintained across the liquid-crystal by the storage capacitor until the pixel is addressed again. High contrast ratios may be achieved by precisely controlling the voltage applied to
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Figure 1.1: Equivalent circuit of active matrix display. A liquid crystal and storage capacitor are connected in parallel being driven by a TFT that is connected to the scan and data circuits.

the liquid crystal, thus allowing a precise amount of light through the display. For organic light-emitting diode (OLED) displays precise control of pixel illumination can be achieved by controlling current injected into the OLED.

With advances in display technology, more stringent manufacturing and performance requirements are necessary. As display technology progresses to generation 10, which uses a substrate that is roughly 3 m $\times$ 3 m, large area uniformity becomes a major concern. Electrical uniformity requirements are more demanding for OLED displays due to the high sensitivity of brightness on the drain current of the driving TFT. Another requirement is that the semiconductor material must be low-temperature compatible, as they are typically fabricated on glass substrates with a thermal tolerance around 600$^\circ$C. Finally, with decreasing aspect ratios in high pixel density displays it is advantageous for TFTs to be transparent to visible light.

1.2 Current Technology and Limitations

In the semiconductor industry, crystalline silicon is the undisputed leading technology platform. As a result silicon has been extensively studied over the past 60 years making it the most understood semiconducting material. Not surprisingly silicon became the dominant technology in the display industry. Rather than crystalline bulk
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silicon, thin-film hydrogenated amorphous silicon (a-Si:H) is the channel material for TFTs.

The use of a-Si:H is attractive as it is low-temperature compatible and can be deposited with plasma-enhanced chemical-vapor deposition (PECVD) below 350°C. It has good large area uniformity due to its amorphous structure and it is a well understood, low-cost material.

![Figure 1.2: Mobility requirements for current and future displays [1].](image)

Several challenges emerge with the demanding requirements of next generation displays. High pixel density displays and fast switching speed applications require a high-mobility semiconductor for improved current drive to minimize delay times [2, 3]. A 50-inch AM-LCD with copper bus lines was used to determine the estimated mobility requirements shown in Fig. 1.2. These values roughly double when considering a 70-inch AM-LCD due to increased delay times [1]. This is a major drawback for a-Si:H whose mobility is around 1 cm²/Vs. Another disadvantage with a-Si:H is its bias stress instability. A 20% change in brightness can occur if the driving TFTs $V_T$ shifts by 0.1 V [4]. As such, a-Si:H is not a viable material for TFTs driving organic
light emitting diodes (OLEDs). While compensation circuits exist which cancel out $V_T$ errors exist and make it possible to use a-SI:H as an OLED driver, the added complexity reduces yield, driving costs up. One example of such a circuit can be seen in Fig. 1.3.

### Figure 1.3: Active matrix $V_T$ compensation circuit utilizing 4 TFTs and 2 storage capacitors [5].

#### 1.3 Candidates to Replace a-SI:H

In order to meet the driving demand of the display industry, several candidates to replace a-SI:H are being investigated; some can be seen in Table 1.1. Low-temperature polycrystalline silicon (LTPS) fulfills the mobility requirements and is at least an order of magnitude greater than its amorphous counterpart. It is also stable enough under bias stress that it can be used to drive OLEDs without a compensation circuit. Also, as a result of the fabrication process CMOS transistors are able to be realized and as such their benefits may be utilized. LTPS is formed by depositing a-SI:H and then crystallized by excimer laser annealing (ELA). This technique is appealing because of its ability to crystallize the a-SI:H without heating the substrate. Significant issues
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with this process are the high cost and large-scale electrical uniformity issues. As such, it is a suitable candidate for small form displays like cellphones and tablets rather than larger substrates, like Gen 10 displays. Amorphous-oxide semiconductors, such as IGZO, are another contender to replace a-Si:H. This is due to their high electron mobility compared to a-Si:H. These materials can have a lower density of tail-states associated with the conduction band making them less sensitive to bias stress than a-Si:H [2, 4]. They also don’t suffer from electrical non-uniformities like LTPS due to their amorphous structure and are low-temperature compatible. As such, unlike LTPS, they are suitable candidates for large form displays.

Table 1.1: Comparison of a-Si:H, Poly-Si, and a-IGZO as TFT channel materials [2, 4].

<table>
<thead>
<tr>
<th>Channel Material</th>
<th>TFT Type</th>
<th>Channel Mobility ($cm^2/ Vs$)</th>
<th>Leakage Current</th>
<th>TFT Uniformity</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si:H</td>
<td>NMOS</td>
<td>&lt;1</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>LTPS</td>
<td>CMOS</td>
<td>&gt;100</td>
<td>Fair</td>
<td>Fair</td>
</tr>
<tr>
<td>IGZO</td>
<td>NMOS</td>
<td>≈ 10</td>
<td>Excellent</td>
<td>Good</td>
</tr>
</tbody>
</table>

1.4 Brief History of Oxide-Semiconductors

The first oxide-semiconductors came into use after the publication of a CdS TFT in 1962 [6]. Following this, several binary TFTs were demonstrated including In$_2$O$_3$ in 1964, ZnO in 1968 and SnO$_2$ in 1970. The first AM-LCD was demonstrated in 1973 using CdSe TFTs and following this a-SI:H took over the market. ZnO saw revitalized interest in 2003 when shortcomings of a-SI:H TFTs were first becoming apparent. Since then several new ternary and quaternary AOS have been developed to address electrical performance and stability challenges present in binary oxide-semiconductors [2].
1.5 Motivation For The Development of IGZO TFTs

Amorphous indium-gallium-zinc-oxide (a-IGZO) is a promising material that has gained interest in the flat panel display (FPD) industry due to its high electron mobility, which is about an order of magnitude larger than a-Si:H and similar to that of ZnO. The 4 atom composition frustrates crystallization even under higher temperature annealing ($\geq 400^\circ C$). This is in contrast to ZnO and as a result the film can achieve better large area uniformity while being deposited by sputtering. The threshold voltage of IGZO is also much lower than ZnO. It is hypothesized that this is due to gallium suppression of the free electrons [7]. IGZO is low-temperature deposition compatible and exhibits high ON/OFF current ratios [2, 4]. IGZO is also less sensitive to illumination induced instability than a-Si:H, resulting in improved device reliability. Additionally it is compatible with processing techniques currently used with a-Si:H ensuring a quick transition when integrating with high-volume manufacturing at a low cost [2, 3, 8]. AOS are typically more stable than a-Si:H with regard to temperature bias stress, and illumination bias stress testing. This is the result of a lower number of tail states near the conduction band [9]. The performance improvement of IGZO over a-Si:H is especially evident in Fig. 1.4 where, when normalized by device width the IGZO TFT current drive is approximately 1.5 times larger than the a-Si:H TFT despite being roughly 10 times longer in channel length. This allows IGZO devices to operate at lower voltages and can result in reduced power consumption.
Several challenges with a-IGZO must be overcome before it is widely adopted in the flat panel display industry. Storage ambient could cause the electrical properties of the film to change, necessitating a passivation material being deposited on the back-channel of a bottom-gate TFT to ensure device stability. IGZO is not a chemically robust material, necessitating lift-off processing following the active area etch. Process-induced damage is also a concern whenever plasma processes are considered as it may generate defects in the IGZO, degrading I-V characteristics.
Chapter 2

This chapter will provide an overview of the preliminary research that was performed. This consists of a discussion of bottom- and double-gate device fabrication and their respective electrical characteristics. The bottom gate device was staggered with a TEOS passivation layer and the double gate device was a staggered passivated bottom gate with the addition of a coplanar top gate. The response of these devices to bias stress will be discussed. Finally, proposed mechanisms for voltage shifts due to bias stress will be explored.

2.1 Device Fabrication

In order to simulate a glass substrate a 6-inch Si wafer is oxidized. A 50 nm Mo gate is sputter deposited and then patterned by subtractive wet etch. A 100 nm SiO$_2$ gate dielectric is deposited by plasma-enhanced chemical-vapor deposition (PECVD), with TEOS as the precursor. The dielectric is then densified in a nitrogen ambient for 2 hours at 600°C. A 50 nm IGZO film is deposited by RF sputter from a target with an In:Ga:Zn:O atomic ratio of 1:1:1:4, and then patterned by subtractive etching in a dilute HCl mixture. Gate contacts are patterned and etched in 10:1 buffered HF. A 300 nm Mo/Al bilayer is deposited by DC sputter for a source and drain region having been previously defined by lift-off processing. A 100 nm SiO$_2$ passivation layer is then deposited by PECVD, with TEOS as the precursor. A 4-hour anneal in an oxygen ambient is then performed followed by a 5-hour oxygen ramp-down. The gate
contact regions were opened, and top-gate electrodes were then defined for double gate devices using evaporated aluminum with a lift-off resist process. Source/drain contacts were then opened for electrical probing. A top-down micrograph and cross-sectional illustration of the resulting structure may be seen in Fig. 2.1.

![Cross-section schematics of bottom and double-gate TFTs. The bottom gate device has staggered gate-source/drain electrodes. The double-gate device has the staggered electrode configuration of the bottom gate device, with the addition of a co-planar top gate.](image)

**Figure 2.1:** Cross-section schematics of bottom and double-gate TFTs. The bottom gate device has staggered gate-source/drain electrodes. The double-gate device has the staggered electrode configuration of the bottom gate device, with the addition of a co-planar top gate.

### 2.2 Device Performance

Electrical testing was done on TFT structures using an HP-4156 parameter analyzer. TFT channel dimensions were width of 100 $\mu$m and length as indicated. All $I_D$-$V_{GS}$ transfer characteristics presented were taken with a gate voltage up-sweep unless otherwise noted, with low-drain and high-drain bias conditions at 0.1 V and 10 V, respectively.

#### 2.2.1 Long-Channel Behavior

The transfer characteristics of long-channel ($L = 24 \ \mu m$) bottom and double-gate TFTs fabricated using the process flow described in 2.1 are shown in Fig. 2.2. The bottom gate device demonstrated weak control over back-channel interface traps, with a relatively shallow sub-threshold and DIBL-like separation between low-drain and high-drain characteristics. The double-gate device demonstrated steep sub-threshold, a threshold voltage that is right shifted from the BG device, as expected, and added current drive due to the additional accumulated electron charge. [12]
2.2.2 Bias Stress Response

After initial transfer characteristics were collected the response of 24 µm devices to negative (NBS) and positive (PBS) bias stress was observed. The gate was held at -10 V and 10 V with all other terminals at 0 V for negative and positive bias stress, respectively. Measurements were taken at various intervals over an accumulated time of 10,000 seconds under bias-stress. Under positive bias stress the bottom gate device showed a negligible shift; however, negative bias stress resulted in a pronounced left shift, approximately 1.5 V, as shown in Fig. 2.3. The pre-stress characteristic indicates poor control over interface traps as shown by a shallow sub-threshold slope. Time under negative bias stress appears to ionize oxygen vacancies which manifests as fixed positive charge. As such, a lower gate voltage for electron channel charge results in a left shift in threshold voltage\[12\]. Sub-threshold slope steepening was also observed and is attributed to fixed charge behavior; fewer interface traps filling and emptying, for example.
Double-gate devices, on the other hand, exhibited a significant parallel right shift in transfer characteristics under both negative and positive bias stress, as shown in Fig. 2.4. Due to the overlapped co-planar top-gate and source/drain electrodes the double-gate devices experience electron injection and trapping in the oxide regions between those overlapped terminals. This effect is hypothesized to be responsible for the parallel right shift observed under positive bias stress. Similar to positive bias stress, the double-gate device also experiences charge injection and trapping in the oxide regions under negative bias stress, which supports a right-shift; however the magnitude of the observed shift is less than that under positive bias stress. It is hypothesized that the negative bias stress left shift response of the bottom gate device is simultaneously operative on the double-gate device. The resulting stress response is then attributed to the superposition of the two distinct charge mechanisms. \[12\]
CHAPTER 2. PRELIMINARY RESEARCH

Figure 2.4: Response of double-gate devices to a) positive bias stress and b) negative bias stress. (c) Double gate device transfer characteristic voltage shift over time under negative and positive bias stress.

2.3 1-D Device Model

2.3.1 Initial Model

A SPICE level-2 model which uses an effective mobility model to account for mobility enhancement, was derived. This model was developed starting with (2.1).

\[
I_{D_{\text{lin}}} = \frac{W}{L} \mu C_ox' (V_{GS} - V_T) V_{DS} \tag{2.1a}
\]

\[
I_{D_{\text{sat}}} = \frac{W}{L} \mu C_ox' \frac{(V_{GS} - V_T)^2}{2} \tag{2.1b}
\]

where an effective mobility model, shown in (2.2), is used to account for the normal field mobility enhancement seen in a-IGZO by allowing the fitting parameter, \( \theta \) to be negative.

\[
\mu = \frac{\mu_{TH}}{1 + (V_{GS} - V_T) \theta} \tag{2.2}
\]
This substitution for mobility results in (2.3).

\begin{align}
I_{D_{\text{lin}}} &= \frac{W}{L - \Delta L} \frac{\mu_{TH}}{1 + (V_{GS} - V_T) \theta} C_{ox}' (V_{GS} - V_T) V_{DS} \tag{2.3a} \\
I_{D_{\text{sat}}} &= \frac{W}{L - \Delta L} \frac{\mu_{TH}}{1 + (V_{GS} - V_T) \theta} C_{ox}' \frac{(V_{GS} - V_T)^2}{2} \tag{2.3b}
\end{align}

Using a least mean squares method the threshold voltage, field-dependent mobility, and theta term were extracted. An example fit for the linear mode of operation can be seen in Fig. 2.5.

![Measured and modeled linear ID-VGS transfer characteristics.](image)

\begin{align*}
V_T &= -2.5 \text{ V} \\
\mu_{TH} &= 8.10 \text{ cm}^2/\text{Vs} \\
\theta &= -0.035 \\
\text{NRMSE} &= 2.1 \%
\end{align*}

\textbf{Figure 2.5:} Measured and modeled linear } I_D-V_{GS} \text{ transfer characteristics.}
2.3.2 Model Refinement

Even though the initial model was able to describe on-state behavior it had one major flaw. Linear and saturation were coupled together with a common mobility but were given separate threshold voltages. This degree of freedom was given in order to determine the current at any drain voltage, however, it is not an accurate metric. For any device all modes of operation should have the same threshold voltage. In order to fix this issue a new model was created that couples all modes of operation together with the same parameter set. As shown in Eq. 2.4 the gradual channel approximation and a new effective mobility model were used to model device behavior.

\[
I_D = \frac{W}{L - \Delta L} C'_{ox} \mu_{eff} [V_{DS}(V_{GS} - V_T) - \frac{(V_{DS})^2}{2}]
\]

\[
\mu_{eff} = \frac{\mu_0}{1 + \theta [V_{DD} - (V_{GS} - V_T)]}
\]

Using a least mean squares method the threshold voltage, field-independent mobility, and theta terms were extracted. An example fit for the linear and saturation modes of operation can be seen in Fig. 2.6.

![Figure 2.6: Measured and modeled linear and saturation $I_D$-$V_{GS}$ transfer characteristics. The measured data and model are represented by circles and a solid line, respectively.](image-url)
2.4 Terada-Muta Analysis of IGZO TFTs

To make full use of the parameter extraction method previously described, Terada-Muta analysis was performed on IGZO TFTs to determine $\Delta L$. The measured $\Delta L$ and from Fig. 2.7 was $3\mu m$ for both a Ti/TiN and a Mo/Al contact metal. There is good correlation between the lithography bias shown in Fig. 2.8 and the Terada-Muta extracted $\Delta L$. The lithography bias is a result of the lift-off resist undercutting the photoresist and is intrinsic to any device configuration which utilizes lift-off processing.

![Terada-Muta analysis of IGZO TFTs.](image1)

**Figure 2.7:** Terada-Muta analysis of IGZO TFTs.

![S/D lift-off lithography bias with a mask defined channel length of 6µm.](image2)

**Figure 2.8:** S/D lift-off lithography bias with a mask defined channel length of 6µm.
2.5 Summary of Preliminary Research

Bottom- and double-gate devices were fabricated using the process flow presented in 2.1. Electrical testing was performed on 24 µm devices and device transfer characteristics were compared. In comparison to the bottom gate, double-gate devices showed a steeper sub-threshold slope and a right-shifted transfer characteristic. The response of these devices to negative and positive bias stress was then observed. The bottom gate devices exhibited a negligible shift and a significant left shift under positive and negative bias stress, respectively. The left shift under negative bias stress is attributed to ionized oxygen vacancies manifesting as fixed positive charge. The double-gate devices, on the other hand, exhibited a significant right shift under both positive and negative stress. Under positive bias stress the coplanar top gate exhibits charge injection and trapping in the underlying oxide, resulting in a right shift. The right shift under negative bias stress is attributed to a superposition of the charge mechanisms present in bottom gate devices under negative bias stress and double-gate devices under positive bias stress. A device model that utilized an effective mobility model was presented. Using a least mean squares method the operation mode independent threshold voltage, field-dependent mobility, and theta terms were extracted. This model presented a 2-3% root mean squared error.
Chapter 3

Single and Double Gate TFTs

In order to properly assess the compatibility of a silicon substrate based IGZO TFT process flow with glass substrates a series of experiments was designed. First, a new photomask was designed that enabled fabrication of all gate electrode configurations within each test chip. Using the process flow described in Sec. 3.2 IGZO TFTs were fabricated on four wafers, two glass substrates and two silicon substrates with a thick grown oxide. Of those wafers one of each substrate type was fabricated without ALD Al$_2$O$_3$ in order to determine the effect of a capping layer on device performance.

3.1 New Mask Design

When comparing the electrical performance of varying gate electrode configurations it is of paramount importance that the interface between channel and gate dielectric regions be the same for all devices. One way for this to be achieved is for devices with all possible gate electrode configurations be processed under the exact same conditions. To this end, a new layout has been created that enables the fabrication of all gate configurations within each test chip. There are also several options in electrode overlaps and underlaps for an additional study on the susceptibility to bias-stress. An image of the test chip can be seen in Fig. 3.1. In order to fully assess the electrical characteristics of fabricated TFTs the test chip contains double, bottom, and top gate transistors with combinations of widths and lengths ranging from 48 $\mu$m to 6 $\mu$m. These combinations are then replicated twice in order to accommodate
differing electrode overlaps for the top and bottom gate. For example, one iteration of devices has the top gate overlapping the source/drain region by 4 μm and the bottom gate under-lapping the source/drain region by 2 μm, and vice-versa. A depiction of gate overlap and underlap can be seen in Fig. 3.2. These variations of overlap and underlap are to be used to test the hypothesis of charge injection in the gate dielectric causing an exaggerated bias stress susceptibility. Besides stand-alone transistors the test chip also contains the following test-structures: square capacitors, inter-digitated capacitors (IDCs), Van-Der Pauws, ring oscillators, and inverters.

Figure 3.1: An image of the new reticle design for IGZO TFTs. This reticle enables all electrode configurations to be present on one wafer.
CHAPTER 3. SINGLE AND DOUBLE GATE TFTS

3.2 Device Fabrication

In order to simulate a glass substrate a 650 nm oxide is grown on a silicon substrate. A 50 nm Mo gate is sputter deposited and then patterned by subtractive wet etch. A 100 nm SiO$_2$ gate dielectric is deposited by plasma-enhanced chemical-vapor deposition (PECVD), with TEOS as the precursor. The dielectric is then densified in a nitrogen ambient for 2 hours at 600°C. An optional 10-15 nm ALD Al$_2$O$_3$ capping layer can then be deposited. A 70 nm Ti/TiN bilayer is deposited on half the wafer by DC sputter for a source and drain region having been previously defined by lift-off processing. A 50 nm IGZO film is deposited by RF sputter from a target with an In:Ga:Zn:O atomic ratio of 1:1:1:4, and then patterned by subtractive etching in a dilute HCl mixture. A 300 nm Mo/Al bilayer is deposited on the remaining half of the wafer by DC sputter for a source and drain region having been previously defined by liftoff processing. A 100 nm TEOS SiO$_2$ passivation layer is then deposited by PECVD. An 8-hour anneal in an oxygen ambient is then performed followed by a 2-hour oxygen ramp-down. An optional 10-15 nm ALD Al$_2$O$_3$ capping layer can then be deposited. Gate and source/drain contact regions are then patterned and opened in a 10:1 BOE etch for 5 min. A 500-750 nm pure aluminum film is then deposited by evaporation. Top gate electrodes and metal traces are then defined and patterned by subtractive wet etch. A step by step illustration of the process flow as well as a top-down micrograph and cross-sectional illustration can be seen in Fig. 3.3 and Fig. 3.4. A summary of the fabrication differences for each wafer can be seen in Table 3.1.
Figure 3.3: A step by step illustration of device fabrication. Process flow is as follows: a) Barrier oxide growth, b) Bottom gate deposition and patterning, c) Bottom gate dielectric deposition, d) DGTS S/D deposition and patterning, e) IGZO deposition and patterning, f) DGBS S/D deposition and patterning, g) Top gate dielectric deposition, and h) Top gate deposition and patterning. An ALD capping layer can be deposited on top of either or both gate dielectric.
CHAPTER 3. SINGLE AND DOUBLE GATE TFTS

Figure 3.4: Fabrication results in a) double-gate from top gate on the left hand half and b) double-gate from bottom gate on the right hand half of the wafer. c) An optical microscope image of a double-gate with a staggered bottom gate IGZO TFT.

Table 3.1: Summary table of fabrication differences between each wafer. All wafers contain all possible device configurations.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Substrate Type</th>
<th>Capping Layer</th>
<th>Electrode Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Silicon</td>
<td>None</td>
<td>All</td>
</tr>
<tr>
<td>2</td>
<td>Silicon</td>
<td>10 nm Al₂O₃</td>
<td>All</td>
</tr>
<tr>
<td>3</td>
<td>Glass</td>
<td>None</td>
<td>All</td>
</tr>
<tr>
<td>4</td>
<td>Glass</td>
<td>10 nm Al₂O₃</td>
<td>All</td>
</tr>
</tbody>
</table>
CHAPTER 3. SINGLE AND DOUBLE GATE TFTS

3.3 Bottom Gate TFTs

Figure 3.5: $I_D$-$V_{GS}$ transfer characteristics of staggered bottom gate devices, with different rest times.

The $I_D$-$V_{GS}$ transfer characteristics for staggered bottom gate devices with $W/L = 24/24$µm and $W/L = 24/12$µm can be seen in Fig. 3.5. Upon testing these devices exhibited a poor subthreshold slope and a 1 to 2 volt separation between low and high drain characteristics. Subthreshold separation usually occurs for one of two reasons, either the device was under-oxidized or over-oxidized during anneal. From the results of previous research [13] it was determined that the devices were over-oxidized rather than under-oxidized. For the process lot used in this study, the only difference in fabrication was that the passivation TEOS was deposited 2-3 days after IGZO deposition. In previous process lots, the passivation material generally was not deposited until a week or two after IGZO deposition. Since remarkable staggered bottom gate transfer characteristics were successfully realized with an eight hour O$_2$ anneal it is believed that a difference in the IGZO channel material caused the over-oxidation. Mainly, it is suspected that the IGZO process lot in this study was not given enough time to sit in room ambient before the passivation layer was deposited. In order to test this hypothesis, passivated staggered bottom gate devices were fabricated using IGZO that was sputtered approximately two months prior.
After mesa and source/drain patterning the wafer was cleaved and half of the wafer was annealed for 8-hours in an O\textsubscript{2} ambient. Directly after anneal, a 10 nm ALD Al\textsubscript{2}O\textsubscript{3} film was deposited and contacts were patterned.

As per Fig. 3.5, devices that underwent an 8-hour O\textsubscript{2} anneal and were delayed for 2-months before passivation have a right-shifted $V_T$ and a superior subthreshold slope. In comparison, devices that were delayed for 2-days before passivation are severely distorted, displaying a left-shifted $V_T$ and subthreshold separation. From this data, a hypothesis has been developed to explain this aging phenomenon. It is believed that after deposition the IGZO film contains a high amount of interstitial oxygen. As the film sits in a room ambient the oxygen is released into the air until an equilibrium level is reached. As such, the longer the film sits in room ambient the more oxygen is released. However, if a passivation material is deposited immediately after IGZO deposition the interstitial oxygen is not allowed to release. As such, upon introduction to an O\textsubscript{2} anneal the film contains a super-saturated amount of oxygen which results in an over-oxidation of the film if the anneal is too long, as shown in Fig. 3.5.

This aging effect is thought to affect the electrostatics of the TFT back channel. Therefore, an electrical comparison of bottom gate TFTs between each process difference was not able to be collected as all processed wafers appear to be compromised. All other gate electrode configurations, however, appear to be able to compensate for this effect and regain control over the IGZO back channel. This being the case a statistical analysis and electrical comparison of all other gate-electrode configurations was obtained. However, a definitive conclusion towards a superior gate-electrode configuration and differences between processes cannot be made as these devices are most definitely compromised.
3.4 Double Gate with Staggered Bottom Gate (DGBS) TFTs

3.4.1 Electrical Characteristics

The $I_D-V_{GS}$ transfer characteristics of double-gate with staggered bottom gate devices on wafers 1–4 \(^1\) outlined in Table 3.1 can be seen in Fig. 3.6. Representative extracted parameters for the four treatments can be seen in Table 3.2. On silicon wafers with an ALD capping layer a right shift in $V_T$ is observed along with a decline in mobility and subthreshold slope. The opposite trend appears on the glass wafers for $V_T$ and subthreshold slope. With an ALD capping layer, a left shift occurred in $V_T$ and the subthreshold slope steepened on the glass wafer. One possibility for this reversal in device behavior is that the gate dielectric thickness could be slightly different on the glass wafers as compared to the silicon ones. Also, it must be noted that all device parameters were extracted assuming the electrostatics of a single gate configuration and the same oxide capacitance.

\[ I_D-V_{GS} \text{ transfer characteristics of } W/L = 24/24\mu m \text{ double-gate from bottom gate TFTs.} \]

\[ V_{DS} @ 0.1V & 10V \]

\[ \begin{array}{c|c|c|c|c}
\hline
& Wafer 1 & Wafer 2 & Wafer 3 & Wafer 4 \\
\hline
\text{Drain Current (A)} & \times 10^{-14} & \times 10^{-12} & \times 10^{-10} & \times 10^{-8} \\
\text{Gate Voltage (V)} & -5 & 0 & 5 & 10 \\
\hline
\end{array} \]

\(^1\)Process differences on wafers as follows: W1-Si/No ALD, W2-Si/ALD, W3-Glass/No ALD, W4-Glass/ALD
Table 3.2: Extracted electrical characteristics of $W/L = 24/24\mu m$ double-gate from bottom gate TFTs.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$V_T$ (V)</th>
<th>$\sigma$ (V)</th>
<th>$\mu_0$ (cm$^2$/Vs)</th>
<th>$\sigma$ (cm$^2$/Vs)</th>
<th>SS (mV/dec)</th>
<th>$\sigma$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.2</td>
<td>0.2</td>
<td>14.35</td>
<td>1.24</td>
<td>267</td>
<td>48</td>
</tr>
<tr>
<td>2</td>
<td>1.1</td>
<td>0.3</td>
<td>12.92</td>
<td>1.98</td>
<td>354</td>
<td>77</td>
</tr>
<tr>
<td>3</td>
<td>-0.1</td>
<td>0.3</td>
<td>15.47</td>
<td>0.68</td>
<td>323</td>
<td>81</td>
</tr>
<tr>
<td>4</td>
<td>-0.6</td>
<td>0.2</td>
<td>13.64</td>
<td>1.02</td>
<td>229</td>
<td>74</td>
</tr>
</tbody>
</table>

Figure 3.7: Box plots of extracted parameters for DGBS on wafers 1 – 4.
To determine the behavior of the population of wafers 1−4 a sample of 25 devices were measured from each wafer. The notch of a boxplot represents the confidence interval of the median. When the notches of separate boxplots overlap it can be assumed with a 95% confidence level that the sample set is from the same population. Since there are no overlapping notches, Fig. 3.7 shows that there are clear difference in \( V_T \), \( \mu_0 \) and \( SS \) between each of these treatments. When considering device operation wafer one shows a superior subthreshold slope and mobility; however, wafer three is close runner up with a tight distribution in mobility.

3.4.2 Summary of Results DGBS

Silicon substrates show a right shift in threshold voltage but a decline in subthreshold slope with the inclusion of an ALD capping layer. Glass substrates, however, show a left shift in threshold voltage and an improvement in subthreshold slope with the inclusion of an ALD capping layer. Glass substrates also demonstrate a slight improvement in mobility in comparison to silicon substrates.

\(^2\)Process differences on wafers as follows: W1-Si/No ALD, W2-Si/ALD, W3-Glass/No ALD, W4-Glass/ALD
3.5 Double Gate with Staggered Top Gate (DGTS) TFTs

3.5.1 Electrical Characteristics

The $I_D$-$V_{GS}$ transfer characteristics of double-gate with staggered top gate devices on wafers 3 and 4 \(^3\) outlined in Table 3.1 can be seen in Fig. 3.8. Representative extracted parameters for the two treatments can be seen in Table 3.3. Device results are missing for the oxidized silicon substrates because of an error in fabrication that resulted in the deposition of two source/drain regions for these devices. Ignoring noise floor differences between the treatments it can be seen that an almost perfect overlay exists between the two transfer curves. As shown in Fig. 3.3 the only difference between the two treatments is a higher mobility for wafer three. It is believed that the mobility would be similar if the series capacitance of the ALD capping layer was considered. As such, it can be claimed that an ALD capping layer has little to no effect on the transfer characteristics of a double-gate device with staggered top gate and coplanar bottom gate configuration.

\(^3\)Process differences on wafers as follows: W3-Glass/No ALD, W4-Glass/ALD
Table 3.3: Extracted electrical characteristics of $W/L = 24/24\mu m$ double-gate from top gate TFTs.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$V_T$ (V)</th>
<th>$\sigma$ (V)</th>
<th>$\mu_0$ (cm$^2$/Vs)</th>
<th>$\sigma$ (cm$^2$/Vs)</th>
<th>SS (mV/dec)</th>
<th>$\sigma$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0.4</td>
<td>0.3</td>
<td>16.51</td>
<td>1.52</td>
<td>294</td>
<td>33</td>
</tr>
<tr>
<td>4</td>
<td>0.4</td>
<td>0.5</td>
<td>14.94</td>
<td>2.32</td>
<td>296</td>
<td>37</td>
</tr>
</tbody>
</table>

Figure 3.9: Box plots of extracted parameters for DGTS on wafers 3 – 4.
To determine the behavior of the population of wafers three and four, a sample of 25 devices were measured from wafer three. Due to a yield issue on the wafer only a sample of 15 devices was able to be measured on wafer four. It is believed that this issue was caused by non-uniformity during the dielectric deposition step. As a result, the true median of the devices is not able to be determined with a 95% confidence level. In Fig. 3.9 this is represented by a notch going beyond the interquartile range. Even with this issue, however, it can be seen that an overlap occurs for $V_T$ and subthreshold slope, which means that the sample sets are possibly from the same population. To truly determine if the sample sets are similar a larger sample size is needed.

### 3.5.2 Summary of Results DGTS

For both treatments on the glass substrates no difference can be observed between the transfer curves. In the transfer characteristics a decline in mobility can be seen for the ALD capping layer treatment. However, it is believed that the mobility would be similar if the series capacitance of the ALD capping layer was considered when extracting parameters.

---

4Process differences on wafers as follows: W3-Glass/No ALD, W4-Glass/ALD
3.6 Staggered Top Gate (TGS) TFTs

3.6.1 Electrical Characteristics

The $I_D-V_{GS}$ transfer characteristics of staggered top gate devices on wafers 3 – 4\(^5\) outlined in Table 3.1 can be seen in Fig. 3.10. Representative extracted parameters for the four treatments can be seen in Table 3.4. As with the double-gate with staggered top gate devices results are missing for the oxidized silicon substrates because of an error in fabrication that resulted in the deposition of two source/drain regions for these devices. The device from wafer three shows a right shifted curve and little to no separation between low and high drain curves. The wafer three device also shows a superior subthreshold slope however, the current drive of both devices is identical. As such, it the device on wafer four displays weaker control over defect states and the channel than that on wafer three.

![Graph showing $I_D-V_{GS}$ transfer characteristics](image)

Figure 3.10: $I_D-V_{GS}$ transfer characteristics of $W/L = 24/24\text{µm}$ staggered top gate TFTs.

---

\(^5\)Process differences on wafers as follows: W3-Glass/No ALD, W4-Glass/ALD
Table 3.4: Extracted electrical characteristics of $W/L = 24/24 \mu m$ staggered top gate TFTs.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$V_T$ (V)</th>
<th>$\sigma$ (V)</th>
<th>$\mu_0$ (cm$^2$/Vs)</th>
<th>$\sigma$ (cm$^2$/Vs)</th>
<th>$SS$ (mV/dec)</th>
<th>$\sigma$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
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<td>0.5</td>
<td>9.60</td>
<td>0.32</td>
<td>398</td>
<td>25</td>
</tr>
<tr>
<td>4</td>
<td>$-0.1$</td>
<td>0.1</td>
<td>9.45</td>
<td>0.40</td>
<td>502</td>
<td>98</td>
</tr>
</tbody>
</table>

Figure 3.11: Box plots of extracted parameters for $TG_{stg}$ on wafers 3 – 4.
To determine the behavior of the population of wafers 3 and 4, a sample of 25 devices were measured from each wafer. As with the double-gate with staggered top gate devices a smaller sample set, 10 devices, was obtained for wafer four because of a yield issue. As such, the true medians of the wafer four device characteristics are not able to be determined with a 95% confidence level. If the region of the notch beyond the interquartile range is considered invalid then only the mobility of the two samples overlap. From transfer characteristics alone, a glass substrate without an ALD encapsulation layer can be considered superior for the staggered top gate configuration.

3.6.2 Summary of Results TGS

Characteristics for the silicon substrates were not extracted due to a fabrication issue that resulted in two source/drain regions for these devices. On the glass substrates, a steeper subthreshold is observed for the no-ALD barrier treatment. The characteristic of wafer four seems to lend itself to a different distribution of trap states in the channel. This is believed to cause the spreading out and separation in the transfer curve.

---

6Process differences on wafers as follows: W3-Glass/No ALD, W4-Glass/ALD
3.7 Coplanar Top Gate (TGC) TFTs

3.7.1 Electrical Characteristics

The $I_D-V_{GS}$ transfer characteristics of coplanar top gate devices on wafers $1 - 4$ outlined in Table 3.1 can be seen in Fig. 3.12. Representative extracted parameters for the four treatments can be seen in Table 3.5. While all the treatments show reasonable off-state characteristics the subthreshold and on-state operation is a bit challenged. For starters, all treatments show a suboptimal average subthreshold slope. Also wafer three shows a separation between the low and high drain characteristics while wafer one shows a hysteresis-like effect. While wafers 2 and 4 don’t show separation between the low and high drain curves their current drive is slightly less than that of wafers 1 and 3. The lower current drive of coplanar top gate devices is the result of thicker oxide near the edge of the channel due to the topology of the metal S/D regions. The lowered capacitance in these areas makes it difficult to control the channel where this topology occurs.

![Graph showing $I_D-V_{GS}$ transfer characteristics of coplanar top gate TFTs.](image)

**Figure 3.12:** $I_D-V_{GS}$ transfer characteristics of $W/L = 24/24\mu m$ coplanar top gate TFTs.

---

*Process differences on wafers as follows: W1-Si/No ALD, W2-Si/ALD, W3-Glass/No ALD, W4-Glass/ALD*
Table 3.5: Extracted electrical characteristics of $W/L = 24/24 \mu m$ coplanar top gate TFTs.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$V_T$ (V)</th>
<th>$\sigma$ (V)</th>
<th>$\mu_0$ (cm$^2$/Vs)</th>
<th>$\sigma$ (cm$^2$/Vs)</th>
<th>$SS$ (mV/dec)</th>
<th>$\sigma$ (mV/dec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.3</td>
<td>1.0</td>
<td>4.86</td>
<td>1.72</td>
<td>404</td>
<td>73</td>
</tr>
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<td>0.6</td>
<td>1.1</td>
<td>4.77</td>
<td>2.51</td>
<td>544</td>
<td>209</td>
</tr>
<tr>
<td>3</td>
<td>$-1.3$</td>
<td>1.2</td>
<td>2.08</td>
<td>1.58</td>
<td>404</td>
<td>57</td>
</tr>
<tr>
<td>4</td>
<td>$-0.5$</td>
<td>1.4</td>
<td>3.06</td>
<td>1.53</td>
<td>329</td>
<td>59</td>
</tr>
</tbody>
</table>

Figure 3.13: Box plots of extracted parameters for $TG_{cop}$ on wafers 1 – 4.
To determine the behavior of the population of wafers 1 – 4, a sample of 25 devices were measured from each wafer. As can be seen in Fig. 3.13 the coplanar top-gate configuration appears inferior to other electrode configurations. Each treatment appears to have a wide spread on all device characteristics. To truly determine if the sample sets are similar and to get more defined distribution a larger sample size is required.

3.7.2 Summary of Results TGC

While the coplanar top gate configuration is the easiest and quickest to fabricate the low quality electrical characteristics outweigh the efficiency gains. For all process modifications a low mobility and high subthreshold swing is observed. Also, when devices were fabricated on glass the electrical performance was degraded. These devices also presented a lower current drive as a result of thicker oxide near the edge of the channel due to the topology of the metal S/D regions. The lowered capacitance in these areas makes it difficult to control the channel where this topology occurs.

---

8Process differences on wafers as follows: W1-Si/No ALD, W2-Si/ALD, W3-Glass/No ALD, W4-Glass/ALD
CHAPTER 3. SINGLE AND DOUBLE GATE TFTS

3.8 Evaluation of Electrode Configurations

This section presents a quantitative analysis of DGBS, DGTS, $TG_{cop}$, and $TG_{stg}$ configurations with a glass substrate and an ALD capping layer. An overlay of $I_D$-$V_{GS}$ transfer characteristics can be seen in Fig. 3.14. It is important to note that the coplanar top gate configuration has a max current roughly one order of magnitude less than the other configurations. This is thought to be the result of thicker oxide near the edge of the channel due to the topology of the metal S/D regions. The lowered capacitance in these areas makes it difficult to control the channel where this topology occurs. Maximum current roughly one order of magnitude less than the other configurations.

![Figure 3.14: $I_D$-$V_{GS}$ transfer characteristics of $W/L = 24/24 \mu m$ devices with a glass substrate and ALD capping layer.](image)

To further quantify the difference in these configurations box plots were generated in Fig. 3.15. The sample size of all device configurations was 25. There is a noted improvement in $\mu_0$ when going from a top-gate configuration to either double-gate configuration. This is a result of the double-gate $\mu_0$ being calculated with a $C_{OX}'$
value consistent with a single-gate. Due to its improved subthreshold performance the double-gate with a staggered top gate could be the optimal electrode configuration; however, a larger sample size is required to make a definitive conclusion.

![Graphs showing extracted parameters](image)

**Figure 3.15:** Extracted parameters from $W/L=24/24\ \mu m$ devices with a glass substrate and ALD capping layer.

### 3.8.1 Bias Stress Stability

The bias-stress stability of TFTs is an important parameter when considering the lifetime of a display. Over time bias-stress can lead to $V_T$ shifts which affect the display brightness and may eventually result in sub-pixels not turning either on or off. To evaluate the stability of the TFTs each device configuration will be considered.
but only devices fabricated on a glass substrate will be evaluated. The TFT channel dimensions are $W/L = 24/24\,\mu m$. An initial measurement was performed, then devices were put under stress according to the conditions listed in Table 3.6. Immediately following the stress the devices were measured again. These $I_D-V_{GS}$ transfer characteristics can be seen in Figs. 3.16–3.19.

**Table 3.6**: Bias stress conditions.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS}$ (V)</td>
<td>$\pm 10$</td>
</tr>
<tr>
<td>$V_{DS}$ (V)</td>
<td>0</td>
</tr>
<tr>
<td>$V_{SS}$ (V)</td>
<td>0</td>
</tr>
<tr>
<td>Stress Time (min)</td>
<td>60</td>
</tr>
</tbody>
</table>

**Figure 3.16**: Negative (right) and positive (left) bias stress response for devices of $W/L = 24/24\,\mu m$ for DGBS configuration of wafer three and four.
As seen in Fig. 3.16 the double-gate with a staggered bottom gate on wafer 3 shows moderate instability after both negative bias stress (NBS) and positive bias stress (PBS). Notably, a parallel left shift is seen after NBS and a parallel right shift is seen after PBS. On the other hand wafer four showed a very slight parallel left shift after PBS and no shift after NBS. Due to a lack of sampling it is impossible to conclude if an ALD capping layer really improves bias stress stability or if this is an anomaly.

Figure 3.17: Negative (right) and positive (left) bias stress response for devices of $W/L = 24/24\mu m$ for DGTS configuration of wafer three and four.

As seen in Fig. 3.17 the double-gate with a staggered top gate on wafer 3 shows significant instability after PBS. Notably, a parallel right shift is observed after PBS. Stability was better with NBS with no discernible shift observed after one hour under stress. With an ALD capping layer, the transfer characteristics seem more stable
under both bias conditions. For both NBS and PBS no discernible shift was observed after one hour under stress. Much like the double-gate with a staggered bottom gate configuration, additional sampling is required to conclude that an ALD barrier improves bias stress stability.

For wafer three the staggered top gate configuration behaves much like its respective double-gate configuration, as can be seen in Fig. 3.18. No discernible shift was observed after one hour under NBS and a significant right shift, $\approx 3$ volts, was observed after one hour under PBS. On the other hand, wafer four showed a significant left shift after PBS. Interestingly, an improvement in subthreshold slope and separation can be seen after PBS. However, due to lack of sampling it is unknown if this is an anomaly. Much like wafer three no discernible shift was observed after one hour under NBS.

**Figure 3.18**: Negative (right) and positive (left) bias stress response for devices of $W/L = 24/24\,\mu m$ for TGS configuration of wafer three and four.
Figure 3.19: Negative (right) and positive (left) bias stress response for devices of \( W/L = 24/24 \mu m \) for TGC configuration of wafer three and four.

For wafer three the coplanar top gate shows significant instability after PBS, as can be seen in Fig. 3.19. Notably, a parallel right shift and slight subthreshold separation is seen after PBS. Stability was better after NBS with only a slight left shift being observed. After PBS, wafer four showed the same amount of subthreshold separation but not as significant of a right shift as wafer 3. Under NBS however, no shift in the transfer curve can be seen. Instead, a large subthreshold separation and degradation of subthreshold slope can be observed.
3.9 Summary of Single and Double Gate TFTs

A new photomask was created that enables the fabrication of all gate configurations within each test chip. Using the process flow outlined in Sec. 3.2 all possible device configurations were fabricated on glass and oxidized silicon substrates. In order to determine if an ALD capping layer affects device electrical characteristics one of each substrate type was fabricated without ALD Al\(_2\)O\(_3\) on top of the TEOS layers. Transfer characteristics for each configuration were then extracted and compared.

Due to a possible IGZO aging phenomena all devices experienced an over-oxidizing anneal. As such, the staggered bottom gate devices displayed a degraded subthreshold slope and a one volt separation between the low and high drain characteristics. This aging effect is hypothesized to be the result of interstitial oxygen being released from the IGZO material into room ambient.

Compared to the other device configurations both double-gate configurations show an improved subthreshold slope, a right-shifted \(V_T\), and an improvement in mobility. It was also observed that an ALD capping layer has little to no effect on the electrical performance of double-gate configurations. The staggered top gate configuration was superior to the coplanar top gate which suffered from low current drive, poor subthreshold slope, and degraded mobility. The single gate configurations showed a discernible difference between devices with and without an ALD capping layer. This, however, may be a consequence of the devices being over-oxidized.

More lateral shifting is observed in the single gate configurations under positive bias stress. For the double-gate configurations no discernible shift is observed under both positive and negative bias stress when an ALD capping layer is present in the device structure. This may show that an ALD capping layer is useful for the suppression of bias stress instabilities; however, as previously stated this may be a consequence of over-oxidation and as such more future research is required. The combined results
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indicate that the double-gate with a staggered top gate configuration is superior for transfer characteristics and bias stress susceptibility. Variants on source/drain to gate overlap were not bias stress tested as the results would not be conclusive, due to the device compromise. A qualitative summary of all electrical results can be seen in Table 3.7.

Table 3.7: A qualitative summary of all electrical tests carried out on all electrode configurations.

<table>
<thead>
<tr>
<th></th>
<th>DGBS</th>
<th>TGC</th>
<th>DGTS</th>
<th>TGS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Oxidized Si</td>
<td>Glass</td>
<td>Oxidized Si</td>
<td>Glass</td>
</tr>
<tr>
<td>$V_T$</td>
<td>Good</td>
<td>Ok</td>
<td>Good</td>
<td>Bad</td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>Good</td>
<td>Good</td>
<td>Bad</td>
<td>Bad</td>
</tr>
<tr>
<td>SS</td>
<td>Good</td>
<td>Glass</td>
<td>Bad</td>
<td>Bad</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>DGBS</th>
<th>TGC</th>
<th>DGTS</th>
<th>TGS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ALD</td>
<td>No ALD</td>
<td>ALD</td>
<td>No ALD</td>
</tr>
<tr>
<td>PBS</td>
<td>Good</td>
<td>Bad</td>
<td>Ok</td>
<td>Bad</td>
</tr>
<tr>
<td>NBS</td>
<td>Good</td>
<td>Bad</td>
<td>Ok</td>
<td>Ok</td>
</tr>
</tbody>
</table>

These results are promising and future work will include larger sampling and more aggressive bias stress testing as well as determining the effect of source/drain to gate overlap on bias stress susceptibility. These results indicate that the condition of the secondary interface, which is exposed to processing after the IGZO sputter, is critical to the final electrical performance of IGZO TFTs. Further understanding of what is occurring at this interface is required to refine the scope of future research into IGZO TFTs.
Chapter 4

Comprehensive Device Model

4.1 Motivation

The development of a consistent and reliable parameter extraction model is of paramount importance if a quantitative analysis and comparison of different treatments is required. It is important for this method to add minimum error so that any differences observed can be accounted for by processing differences. IGZO TFTs do not show normal field degradation when operated in linear mode as silicon devices do as shown in Fig. 4.1. Thus, traditional methods used for silicon devices, such as extracting \( V_{GS} \) at the maximum transconductance for \( V_T \) do not work. An attempt to use this method will result in a grossly overestimated \( V_T \) and subsequently \( \mu_{TH} \) and \( \mu_0 \). Traditional methods used for IGZO TFTs calculate \( V_T \) at the maximum of the derivative of \( g_m \). This method provides an acceptable, albeit conservative measurement of \( V_T \); however, this is not a robust method when attempts are made to automate it.
4.2 Refinement of Spice Level 2 Model

4.2.1 Initial Model Shortcoming

Even though a good match exists between the measured and modeled data, the original device model was far from perfect. When attempting to model the family of curves an issue arose where the model could accurately predict the initial and saturation currents but nothing else, as shown in Fig. 4.2. In the initial model an effective channel mobility model was used, as shown in Eq. 4.1.

\[ \mu_{\text{eff}} = \frac{\mu_{\text{ch}}}{1 + (V_{GS} - V_{T_{\text{lin}}})\theta} \]  

(4.1)

This approximation is appropriate if the carrier mean free path is on the order of the chemical bond length. In the case of IGZO however, the electron mean free path is significantly larger than the inter-atomic distance and electron transport is dominated by band conduction behavior. Therefore, a charge model that separates the free-charge ratio and channel mobility is required [14].

Figure 4.1: Linear $I_D-V_{GS}$ measurements of a-Si:H (left) and IGZO (right) TFTs.
4.2.2 Two Dimensional Charge Model

As shown in Fig. 4.1, IGZO TFT transfer characteristics typically exhibit a concave upward trend as the gate bias is increased. Also, in IGZO devices the combination of applied gate and drain voltages determines the occupancy condition of band tail states, and thus establishes the amount of free-electron charge available, at $V_{GS}$ above $V_T$. This mechanism, known as drain-impressed deionization, causes the distribution of occupation of band-tail states to become significantly two dimensional as $V_{DS}$ is increased. As $V_{GS}$ gets greater than $V_{DS}$ the gate reclaims control over state occupation however, the 2D effect remains. This effect translates to an effective potential loss at applied $V_{DS}$ lower than $V_{DSat}$ and as such a loss in saturation current. This can then be expressed by applying a proportionality constant, $\alpha$, to $V_{DS}$, as in Eq. 4.2 [14].

$$V'_{DS} = \alpha V_{DS}$$  \hspace{1cm} (4.2)
Combining these two mechanisms, the free-electron charge can be expressed as in Eq. 4.3.

\[ \eta_{2D} = \frac{1}{1 + \theta'[V_{DD} - (V_{GS} - V_T)]} \left( 1 + \frac{V_{DS}}{V_C} \right) \] (4.3)

Using \( \mu_0 \eta_{2D} \) in place of \( \mu_{ch} \) in the gradual channel approximation, the on-state device can be represented by Eq. 4.4[14].

\[ I_D = \frac{W}{L - \Delta L} C'_{Ox} \mu_0 \eta_{2D} [V'_{DS}(V_{GS} - V_T) - \frac{(V'_{DS})^2}{2}] \] (4.4)

### 4.2.3 Short Channel Refinement

A family of curves for a 6 \( \mu \)m unpassivated bottom gate IGZO TFT, can be seen in Fig. 4.3. As can be seen, the family of curves fit is overestimating in areas below saturation and underestimating in areas above saturation. When this was seen, it was determined that the channel length is smaller than the mask defined length and therfore, the smaller length devices display channel-length modulation. From the Terada-Muta analysis shown in Fig. 2.7 the \( \Delta L \) for IGZO TFTs fabricated with the process flow described in Sec. 3.2 was determined to be approximately 3 \( \mu \)m. This means that the 6 \( \mu \)m device in Fig. 4.3 actually had a channel length of 3 \( \mu \)m.

In order to properly model these smaller length devices, channel-length modulation needed to be included into Eq. 4.4. In order to account for channel-length modulation the following term is multiplied with Eq.4.4.

\[ \frac{1}{1 - \lambda V_d} \] (4.5)

This modification fixes the model up until the drain reaches saturation. Once the drain voltage reaches saturation, the current will start to decrease as a parabolic slope since Eq. 4.4 models a concave down parabola. In order to stop the modeled current from decreasing the slope of the curve at saturation is determined and assumed to
be constant from that point forth. In order to determine the slope, the derivative of Eq. 4.4 multiplied by Eq. 4.5 with respect to $V_d$ at $V_{dsat}$ is taken, which results in Eq. 4.6.

$$
\left( \frac{\partial}{\partial V_d} I_D \frac{1}{1 - \lambda V_d} \right)@V_{dsat} = \frac{\partial}{\partial V_d} I_D \ast \frac{1}{1 - \lambda V_d} + \frac{\partial}{\partial V_d} \frac{1}{1 - \lambda V_d} \ast I_D = I_{Dsat} \frac{1}{1 - \lambda V_d}
$$

This results in the following piece-wise function as the final device model.

$$
I_D = \frac{W}{L - \Delta L} C'_{Ox} \mu_o \eta D \left[ V'_{DS} (V_{GS} - V_T) - \frac{(V'_{DS})^2}{2} \right] \frac{1}{1 - \lambda V_d}, V_d \leq V_{dsat}
$$

$$
I_D = \frac{W}{L - \Delta L} C'_{Ox} \mu_o \eta D \left[ V'_{Dsat} (V_{GS} - V_T) - \frac{(V'_{Dsat})^2}{2} \right] \frac{1}{1 - \lambda V_d}, V_d > V_{dsat}
$$

4.3 Methodology

Fitting parameters are extracted from the refined model by means of a least squares regression strategy with a family of curves of $V_{DS}$ between 0 and 10 V by 0.1 V and $V_{GS}$ between -5 and 10 V by 0.2 V. First, Eq. 4.4 is modified for use in the linear
mode of operation where \( V_{DS} = 0.1 \text{ V} \). For this mode of operation, the effects of drain-impressed deionization are considered negligible so alpha is taken as 1 and \( V_c \) is taken as \( \infty \), as shown in Eq. 4.8.

\[
I_D = \frac{W}{L - \Delta L} C'_{Ox} \mu_o \eta_{2D} \left[ 0.1(V_{GS} - V_T) - \frac{(0.1)^2}{2} \right] \quad (4.8a)
\]

\[
\eta_{2D} \approx \eta_G = \frac{1}{1 + \theta'[10 - (V_{GS} - V_T)]} \quad (4.8b)
\]

From the linear form of Eq. 4.4 an initial \( V_T, \mu_o \), and \( \theta \) are extracted. Since this model can’t predict gate voltages less than \( V_T \) all data below \( V_T \) is removed and \( V_T \) is extracted again. This procedure is then repeated until \( V_{GS_{min}} - V_t \geq 0 \). Next, the parameters extracted from the linear mode of operation are used in the complete form of Eq. 4.4 in order to extract an initial \( V_C \) and \( \alpha \). \( V_C \) and \( \alpha \) are then used in a linear mode version of Eq. 4.4 where the effects of drain-impressed deionization are not taken as negligible. This allows for new \( V_T, \mu_o \), and \( \theta \) to be extracted. Again, this process is repeated until \( V_{GS_{min}} - V_t \geq 0 \). Finally, all five parameters are used as start locations in Eq. 4.4 and the final values of \( V_T, \mu_o, \theta, V_C \), and \( \alpha \) are determined for a long channel device fit.

If the device displays channel-length modulation, a short channel fit must be used. First the long channel procedure described above is used in order to determine an initial guess for each parameter. Next, a least means square analysis is done on Eq. 4.7 using the long channel obtained parameters. For this procedure, \( V_T \) is fixed, a channel-length modulation parameter is added, and all other parameters are allowed to vary. Once the least means square analysis is complete a short channel parameter set is obtained. A flowchart detailing this procedure can be seen in Fig. 4.4. In order to allow for convergence, the boundary conditions from 4.9 are used. Using this routine, the fit in Fig. 4.5 and parameters in Table 4.1 were achieved.
Figure 4.4: Detailed Flowchart of Parameter Extraction Method

\begin{align}
0 &\leq \alpha \leq 1 & (4.9a) \\
0 &\leq \lambda \leq 0.1 & (4.9b) \\
1 &\leq \mu \leq 30 & (4.9c) \\
0 &\leq \theta \leq 1 & (4.9d) \\
0 &\leq V_C \leq 50 & (4.9e) \\
-10 &\leq V_t \leq 10 & (4.9f)
\end{align}
Table 4.1: Parameters extracted from a staggered bottom gate device with \(W/L=100/12\,\mu m\)

<table>
<thead>
<tr>
<th>(\alpha)</th>
<th>(\lambda) ((V^{-1}))</th>
<th>(\mu_o) ((cm^2/Vs))</th>
<th>(\theta) ((V^{-1}))</th>
<th>(V_c) (V)</th>
<th>(V_T) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.83</td>
<td>0.017</td>
<td>11.87</td>
<td>0.04</td>
<td>15.8</td>
<td>-1.9</td>
</tr>
</tbody>
</table>

Figure 4.5: Overlay of transfer and output characteristics of measured data and the presented model. Transfer characteristics are shown in linear mode (a) with \(V_{DS} = 0.1\) V, and saturation mode (b) with \(V_{DS} = 10\) V. (c) Output characteristics with \(V_{GS} = 2-10\) V in steps of 2 V. In all plots data is represented by points and the fit is a solid line.
4.4 Analysis of Fabricated Devices

4.4.1 Double Gate with Staggered Bottom Gate

The family of curves of double-gate with staggered bottom gate devices with lengths of 6 microns can be seen in Fig. 4.6. Parameters extracted using the method presented in Sec. 4.3 can be seen in Table 4.2. As can be seen, wafer three has roughly half as much current drive as the other treatments and wafer four has a higher degree of channel-length modulation. This can be seen as a greater upwards slope in the saturation region as opposed to an approximately zero slope. Also, for all wafers it can be seen from the tabulated values of $V_c$ that the strength of drain-impressed deionization increases as the channel length decreases, with it being stronger on the glass substrates.

Table 4.2: Parameters extracted from double-gate with staggered bottom gate of each treatment with length of 6 microns and width of 24 microns. Parameters were extracted using the method described in Sec. 4.3.  

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$\alpha$</th>
<th>$\lambda$</th>
<th>$\mu$</th>
<th>$\theta$</th>
<th>$V_c$</th>
<th>$V_T$</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.8</td>
<td>0.016</td>
<td>13.3</td>
<td>0.04</td>
<td>17.3</td>
<td>-0.3</td>
<td>190</td>
</tr>
<tr>
<td>2</td>
<td>0.83</td>
<td>0.016</td>
<td>23.22</td>
<td>0.03</td>
<td>16.8</td>
<td>-1.3</td>
<td>201</td>
</tr>
<tr>
<td>3</td>
<td>0.85</td>
<td>0.016</td>
<td>14.07</td>
<td>0.06</td>
<td>11.2</td>
<td>0.6</td>
<td>332</td>
</tr>
<tr>
<td>4</td>
<td>0.8</td>
<td>0.024</td>
<td>14.3</td>
<td>0.05</td>
<td>11.5</td>
<td>-0.1</td>
<td>249</td>
</tr>
</tbody>
</table>

1Process differences on wafers as follows: W1-Si/No ALD, W2-Si/ALD, W3-Glass/No ALD, W4-Glass/ALD
4.4.2 Double Gate with Staggered Top Gate

The family of curves of double-gate with staggered top gate devices with lengths of 6 microns can be seen in Fig. 4.7. Parameters extracted using the method presented in Sec. 4.3 can be seen in Table 4.3. Much like with the characteristics in Table 3.3 and Fig. 3.8 the family of curves for the double-gate with a staggered top gate devices look almost identical, the only difference being a slighter higher maximum current for wafer three. At 6 micron length both treatments show the same degree of channel-length modulation and drain-impressed deionization.
Table 4.3: Parameters extracted from double-gate with staggered top gate of each treatment with length of 6 microns and width of 24 microns. Parameters were extracted using the method described in Sec. 4.3.  

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$\alpha$</th>
<th>$\lambda$</th>
<th>$\mu$</th>
<th>$\theta$</th>
<th>$V_c$</th>
<th>$V_T$</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0.75</td>
<td>0.024</td>
<td>17.46</td>
<td>0.04</td>
<td>29.7</td>
<td>-0.3</td>
<td>298</td>
</tr>
<tr>
<td>4</td>
<td>0.78</td>
<td>0.026</td>
<td>16.01</td>
<td>0.04</td>
<td>28.4</td>
<td>-0.4</td>
<td>296</td>
</tr>
</tbody>
</table>

Figure 4.7: Family of curves for double-gate with staggered top gate with $W/L=24/6$ for each treatment.

4.4.3 Staggered Top Gate

The family of curves of staggered top gate devices with lengths of 6 microns can be seen in Fig. 4.8. Parameters extracted using the method presented in Sec. 4.3 and can be seen in Table 4.4. As with the respective double configuration these devices show almost identical family characteristics. For both treatments the degree of channel-length modulation is exactly the same. Also, it can be seen that the maximum current of the ALD barrier treatment is slightly less than that of the other treatment, which could be explained by the higher degree of drain-impressed deionization. Most interesting to note is that for this electrode configuration both treatments have nearly identical alpha terms, mobility, and theta terms. These similarities could suggest that

---

$^2$Process differences on wafers as follows: W3-Glass/No ALD, W4-Glass/ALD
the addition of an ALD capping layer has no effect on the electrical characteristics of a staggered top gate electrode configuration.

**Table 4.4:** Parameters extracted from staggered top gate of each treatment with length of 6 microns and width of 24 microns. Parameters were extracted using the method described in Sec. 4.3.³

<table>
<thead>
<tr>
<th>Wafer</th>
<th>α</th>
<th>λ</th>
<th>µ</th>
<th>θ</th>
<th>Vc</th>
<th>VT</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0.82</td>
<td>0.026</td>
<td>9.78</td>
<td>0.05</td>
<td>15.3</td>
<td>0</td>
<td>438</td>
</tr>
<tr>
<td>4</td>
<td>0.81</td>
<td>0.026</td>
<td>10.14</td>
<td>0.05</td>
<td>13.2</td>
<td>0.4</td>
<td>575</td>
</tr>
</tbody>
</table>

**Figure 4.8:** Family of curves for staggered bottom gate with W/L=24/6 for each treatment.

### 4.4.4 Coplanar Top Gate

The family of curves of double-gate with staggered top gate devices with lengths of 6 microns can be seen in Fig. 4.9. Parameters extracted using the method presented in Sec. 4.3 and can be seen in Table 4.5. Of all the wafer treatments, the treatment on wafer three seems to be the worst. The degree of channel-length modulation is so strong that the device exhibits a punchthrough-like effect at all current levels. This

³Process differences on wafers as follows: W3-Glass/No ALD, W4-Glass/ALD
effect can also start to be observed on the wafer four treatment. Also of note is that
the degree of drain-induced deionization is a lot higher on the wafer three treatment,
as seen by a low $V_c$ value. This coupled with possible stress in the film stack due to
warping of the glass wafer during process steps involving a heated chuck could explain
the low current drive of wafers 3 and 4.

Table 4.5: Parameters extracted from coplanar top gate of each treatment with length of
6 microns and width of 24 microns. Parameters were extracted using the method described
in Sec. 4.3.  

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$\alpha$</th>
<th>$\lambda$</th>
<th>$\mu$</th>
<th>$\theta$</th>
<th>$V_c$</th>
<th>$V_T$</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.75</td>
<td>0.014</td>
<td>3.85</td>
<td>0.01</td>
<td>14.3</td>
<td>-0.5</td>
<td>342</td>
</tr>
<tr>
<td>2</td>
<td>0.77</td>
<td>0.017</td>
<td>9.76</td>
<td>0.02</td>
<td>8.2</td>
<td>0.5</td>
<td>223</td>
</tr>
<tr>
<td>3</td>
<td>0.71</td>
<td>0.062</td>
<td>1.12</td>
<td>0</td>
<td>4.5</td>
<td>-2.2</td>
<td>384</td>
</tr>
<tr>
<td>4</td>
<td>0.71</td>
<td>0.032</td>
<td>2.83</td>
<td>0</td>
<td>29.7</td>
<td>-1.5</td>
<td>251</td>
</tr>
</tbody>
</table>

Figure 4.9: Family of curves for coplanar bottom gate with $W/L=24/6$ for each treatment.

---

4Process differences on wafers as follows: W1-Si/No ALD, W2-Si/ALD, W3-Glass/No ALD, W4-Glass/ALD
4.5 Summary

IGZO TFT transfer characteristics typically exhibit a concave upward trend as the gate bias is increased. Thus, traditional parameter extraction methods used for silicon devices, such as extracting $V_{GS}$ at the maximum transconductance for $V_T$ do not work. In order to account for this a SPICE Level-2 model for parameter extraction was developed and has been successfully demonstrated. This model attempts to fit a large family of curves by performing iterative calculations of $V_T$, $\mu_0$, $\theta'$, $\alpha$, $\lambda$, and $V_c$ to arrive at a solution. This method shows reliable performance with normalized root mean squared error on the order of 1-2%. For all device electrode configurations the glass substrates have a higher degree of channel length modulation and drain impressed deionization. This is believed to be the result of films depositing differently on the glass or stress in the film stack due to glass warping during process steps utilizing a heated chuck. Much like the transfer characteristics there is evidence in the family of curves to support double gate with a staggered top gate as the superior electrode configuration. The family of curves also supports coplanar top gate as the most inferior electrode configuration. As previously mentioned this is the result of topology issues and as such was expected.
5.1 Summary of Work

IGZO has been shown to be a strong contender for future display applications due to its electrical characteristics being superior to a-Si:H, specifically higher electron mobility and lower operating voltage. Issues performing parameter extraction on IGZO TFTs make a true quantitative comparison with published work impossible. Traditional methods developed for silicon are not applicable and can drastically overestimate $V_T$ and, consequently, mobility. This issue was solved by developing a parameter extraction method based on a SPICE level-2 model. This uses a free channel charge model that accounts for the filling of band-tail states and a mechanism known as drain-impressed deionization. This mechanism causes the distribution of occupation of band-tail states to become significantly two dimensional as $V_{DS}$ is increased. This model was then modified to account for channel length process bias and short-channel effects such as channel-length modulation. Using a Terada-Muta analysis, the $\Delta L$ of fabricated IGZO TFTs was approximately 3 $\mu$m, which corresponds well with an observed lift-off lithography bias. In practice this model provides a good fit to the data averaging between 1% and 2% normalized root mean squared error.

Using a new photo-mask that enabled fabrication of all TFT electrode configurations in a test chip, a process integration study was performed. The effects of an ALD
capping layer on device electrical performance and the compatibility of the process outlined in 3.2 were determined. All possible device configurations were fabricated on glass and oxidized silicon substrates and transfer characteristics for each configuration were extracted and compared. During testing an interesting phenomenon was observed; the staggered bottom gate devices displayed a degraded subthreshold slope and a one volt separation between the low and high drain characteristics. As such, it is believed that the devices experienced an overoxidizing anneal. However, since staggered bottom gate devices fabricated with the same process flow previously exhibited remarkable electrical characteristics this result was puzzling. The current hypothesis for this behavior is that the devices were not allowed to sit long enough in room ambient before passivation TEOS was deposited. It is hypothesized that after sputter the IGZO film contains interstitial oxygen that over time is released into room ambient. As such, if the devices are passivated too soon the interstitial oxygen is not allowed to escape, thus causing a supersaturation of oxygen to exist in the film during the anneal. Resulting from this effect an electrical comparison of bottom gate TFTs between each process difference was not able to be collected as all processed wafers appear to be compromised. All other gate electrode configurations, however, manage to compensate for this effect and regain control over the IGZO back channel.

Compared to other device configurations both double-gate configurations show an improved subthreshold slope, a right shifted $V_T$, and an improvement in mobility. It was also observed that an ALD capping layer has little to no effect on the electrical performance of double-gate configurations. The staggered top gate configuration was superior to the coplanar top gate which suffered from low current drive, poor subthreshold slope, and degraded mobility. The single gate configurations showed a discernible difference between devices with and without an ALD capping layer. This, however, may be a consequence of the devices being over-oxidized.
CHAPTER 5. CONCLUSIONS

After initial device characteristics extracted, each configuration on the glass substrates was subjected to positive and negative bias stresses for one hour. For the double-gate configurations no discernible shift is observed under both positive and negative bias stress when an ALD capping layer is present in the device structure. On the other hand, the double-gate devices without an ALD capping layer showed significant right shifting under positive bias stress and little to no shifting under negative bias stress. This may show that an ALD capping layer is useful for the suppression of bias stress instabilities; however, this may be a consequence of over-oxidation and as such more future research is required. In the single gate configurations more lateral shifting is observed under positive bias stress and similarly exhibit little to no shifting under negative bias stress.

The combined results indicate that the double-gate with a staggered top gate configuration is superior for transfer characteristics and bias stress susceptibility. These results are promising and future work will include larger sampling and more aggressive bias stress testing. The results also show that there is a moderate difference to fabricating on a glass substrate. All differences between the oxidized silicon and glass substrates are suspected to be the result of stress in the film stack due to warping of the glass during any process step involving a heated chuck.

5.2 Future Work

Additional work will be performed to understand the mechanism behind IGZO aging before passivation deposition. All device configurations will then be fabricated on a single glass or oxidized silicon substrate. These results of this experiment will then be used to develop a consistent TCAD model which considers each TFT configuration. Using TCAD, a device model that accurately models double gate on-state electrostatics will be derived. More aggressive bias stress testing will be performed to determine how resistant these configurations are to positive and negative bias stress.
Bibliography


**Acronyms**

**ALD** Atomic layer deposition  
**AM-LCD** Active-matrix liquid-crystal display  
**TGC** Coplanar Top Gate  
**DGBS** Double Gate with Staggered Bottom Gate  
**DGTS** Double Gate with Staggered Top Gate  
**asi** Hydrogenated amorphous silicon  
**IDC** Interdigitated capacitor  
**IGZO** Indium gallium zinc oxide  
**LCD** Liquid crystal display  
**LED** Light-emitting diode  
**OLED** Organic light-emitting diode  
**PECVD** Plasma-enhanced chemical vapor deposition  
**TGS** Staggered Top Gate  
**TEOS** Tetraethyl orthosilicate  
**DGBS** Double Gate with Staggered Bottom Gate  
**TFT** Thin-film transistor
Appendix A: Parameter Extraction Matlab Code

function [ vt , mu, theta, alpha, vc ] = model_fit_extraction(...
width, length, vgs, vds, idslin, idsfam )

% Iterative model fit until Vgs−Vt is > 0

% Puts Vgs in x1 and Idslin in y1
x1=vgs; x2=x1; y1=idslin;

% Initial curve fit and extract fit parameters
[ffit, gof] = createFit(x2, y1, width, length);
extractlin = coeffvalues(ffit);
vt = extractlin(3); mu = extractlin(1); theta = extractlin(2);

% Extract vt, mu, theta from linear data
logic=min(x2) − vt>0;

while logic==0
    % Round all entries in x1 to the nearest 1E−1
    x1=roundn(x1,-1);

    % Find the index of the closest Vgs to Vt
    indx=find(x1==2*roundn(vt/2,-1));

    % Null all entries in x2 and y1 prior to indx
    x2(1:indx)=[] ;
    y1(1:indx)=[] ;

    % Determine initial vt, u0, and theta from reduced linear fit
[ffit, gof] = createFit(x2, y1, width, length);

% Extract Values from Curve Fit
extractlin = coeffvalues(ffit);
vt = extractlin(3); mu = extractlin(1); theta = extractlin(2);
APPENDIX A. PARAMETER EXTRACTION MATLAB CODE

```
logic=min(x2) - vt>0;
end  
%

% Loop Increment
inc = 1;
while inc<=1
  % Recreate Values
  vd=vds; vg=vgs; id=idsfam;
  % Remove all values less than vt since nonsense
  % Round all entries in vg to the nearest 1E-1
  vg=roundn(vg,-1);
  % Find the index of the closest Vgs to Vt
  indx1=find(vg==2*roundn(vt/2,-1));
  % Null all entries in vg and id prior to indx1
  vg(1:indx1)=[];
  id(:,1:indx1)=[];
  % Turn Data Into Column Vectors
  [vd, vg, id] = prepareSurfaceData(vd, vg, transpose(id));
  % Null Start Point
  start = [];
  % Use extracted vt, mu, and theta as start points and find actual values
  % Initial curve fit and extract fit parameters
  [ffit2, gof2] = createFamily(vd, vg, id, width, length, mu, vt, theta, start);
```
extractlin = coeffvalues(ffit2);
alpha = extractlin(1); vc = extractlin(2);

% Puts Vgs in x1 and Idslin in y1
x1=vgs; x2=x1; y1=idslin;

% Extract vt, mu, theta from linear data
logic=min(x2) - vt>0;

while logic==0
    % Round all entries in x1 to the nearest 1E-1
    x1=roundn(x1,-1);

    % Find the index of the closest Vgs to Vt
    indx=find(x1==2*roundn(vt/2,-1));

    % Null all entries in x2 and y1 prior to indx
    x2(1:indx) = [];
    y1(1:indx) = [];

    % Re-evaluate curve fit and extract new parameters with full linear % fit
    [ffit, gof] = createFitFull(x2, y1, width, length, alpha, vc);

    extractlin = coeffvalues(ffit);
    vt = extractlin(3); mu = extractlin(1); theta = extractlin(2);
    logic=min(x2) - vt>0;
end %end while

% Recreate Values
vd=vds; vg=vgs; id=idsfam;
APPENDIX A. PARAMETER EXTRACTION MATLAB CODE

```matlab
% Remove all values less than vt since nonsense
% Round all entries in vg to the nearest 1E-1
vg = roundn(vg, -1);

% Find the index of the closest Vgs to Vt
indx1 = find(vg == 2 * roundn(vt / 2, -1));

% Null all entries in vg and id prior to indx1
vg(1:indx1) = [];
id(:, 1:indx1) = [];

% Turn Data Into Column Vectors
[vd, vg, id] = prepareSurfaceData(vd, vg, transpose(id));

% Start Points
start = [alpha, mu, theta, vc, vt];

% Use extracted vt, mu, and theta as start points and find actual values
% Initial curve fit and extract fit parameters
[ffit2, goffinal] = createFamily(vd, vg, id, width, length, mu, vt, theta, start);
extractlin = coeffvalues(ffit2);
alpha = extractlin(1); mm = extractlin(2); theta = extractlin(3);
vc = extractlin(4); vt = extractlin(5);

% Increment Loop Monitor
inc = inc + 1;
end %end while loop

end %end function
```
function [ f f i t , gof , vt , mu, theta , alpha , vc , lambda ] = 
short_channel_fit( ... 
 width, length, vgs, vds, ids, vt, mu, theta, alpha, vc)

indx = 1; lambda= 0.05;
while indx<=1
    % Recreate Values
    vd=vds; vg=vgs; id=ids;

    % Remove all values less than vt since nonsense
    % Round all entries in vg to the nearest 1E-1
    vg=roundn(vg,−1);

    % Find the index of the closest Vgs to Vt
    indx1=find(vg==2*roundn(vt/2,−1));

    % Null all entries in vg and id prior to indx1
    vg(1:indx1)=[];
    id (:,1:indx1)=[];

    % Turn Data Into Column Vectors
    [vg, vd, id] = prepareSurfaceData(vg, vd, id);

    % Start Points
    start = [alpha, lambda, mu, theta, vc];

    % Use extracted vt, mu, and theta as start points and find actual values
    % Initial curve fit and extract fit parameters
    [ffit, gof] = createFamilyShort(vd, vg, id, width, length, vt, start);
    extractlin = coeffvalues(ffit);
    alpha = extractlin(1); lambda = extractlin(2); mu = extractlin(3);
\texttt{theta = extractlin(4); vc = extractlin(5);}

\texttt{
\% Increment Loop Monitor
indx=indx+1;
end;
}

\texttt{end}
## Appendix B: Process Recipes

**Table B.1: CVC 601 Sputter Recipes.**

<table>
<thead>
<tr>
<th>Material</th>
<th>Power (W)</th>
<th>Gas</th>
<th>Flow Rate (sccm)</th>
<th>Pressure (mTorr)</th>
<th>Deposition Rate (Å min⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>1000</td>
<td>Ar</td>
<td>20</td>
<td>5</td>
<td>500</td>
</tr>
<tr>
<td>Mo</td>
<td>1000</td>
<td>Ar</td>
<td>20</td>
<td>2.8</td>
<td>150</td>
</tr>
<tr>
<td>Ti</td>
<td>1000</td>
<td>Ar</td>
<td>20</td>
<td>6</td>
<td>322</td>
</tr>
<tr>
<td>TiNₓ</td>
<td>500</td>
<td>Ar/N₂</td>
<td>20/22</td>
<td>4.8/1.2</td>
<td>31</td>
</tr>
</tbody>
</table>
## Appendix C: Combined Device Process Flow

<table>
<thead>
<tr>
<th>#</th>
<th>Step</th>
<th>Process Parameters</th>
<th>Process Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Create Lot Notebook</td>
<td>Obtained a Cleanroom notebook a previous notebook can be used</td>
<td>Tape into the notebook: Process Flow (this document) and lot split info</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Update and insert the file located in morbo</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Important Lot Processing Information Sheet</td>
</tr>
<tr>
<td>2</td>
<td>Scribe</td>
<td>Tool: Diamond Tips Scribe</td>
<td>Also make sure all wafers are scribed correctly.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Scribe monitor wafers with the lot number and M1 M3 M4. (these can be found in the monitor wafer box)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>&quot;Print out wafer box label and tape it on 6&quot; or 4&quot; polypropylene box&quot;</td>
</tr>
<tr>
<td>3</td>
<td>RCA Clean</td>
<td>Tool: RCA Bench</td>
<td></td>
</tr>
<tr>
<td>4a</td>
<td>Thick oxide growth</td>
<td>Tool: Bruce furnace</td>
<td>Grow oxide on all silicon wafers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tube: Tube 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Recipe: 350</td>
<td></td>
</tr>
<tr>
<td>4b</td>
<td>TEOS Oxide (glass wafers only)</td>
<td>Tool: P5000</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Chamber: A</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Thickness: 1 kA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Time:</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Mo Sputter</td>
<td>Tool: CVC 601</td>
<td>Want a base pressure of 1.5E-6 before sputtering Mo</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Target: 2 - Molybdenum</td>
<td>Change the platen according to wafer size Include glass slide for thickness measurement and monitor wafers for etch test/stress etc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Ar Flow: 20sccm</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pressure: 2.7mTorr</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power: 1000W</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Thickness: 50nm</td>
<td></td>
</tr>
</tbody>
</table>
### APPENDIX C. COMBINED DEVICE PROCESS FLOW

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Presputter:</td>
<td>300 sec (use shutter)</td>
</tr>
<tr>
<td></td>
<td>Dep. Time:</td>
<td>200 seconds</td>
</tr>
<tr>
<td>6</td>
<td>Measure Mo thickness</td>
<td>Tool: Tencor P2</td>
</tr>
<tr>
<td></td>
<td>Recipe:</td>
<td>Ger</td>
</tr>
<tr>
<td>7</td>
<td>Measure Mo Rs</td>
<td>Tool: CDE Resmap</td>
</tr>
<tr>
<td></td>
<td>&quot;Recipe: 6” Rs 61 points&quot;</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Measure Bow</td>
<td>Tool: Tencor P2</td>
</tr>
<tr>
<td></td>
<td>Recipe: 6_INCH_STRESS</td>
<td>Take Vertical and Horizontal measurements SAVE SCAN and COPY them to Lot Folder on morbo.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Save Files as L<strong>D*H or L</strong>D*V</td>
</tr>
<tr>
<td>9</td>
<td>Gate Litho</td>
<td>SVG (program 1) or manual dispenser SSI (nodispense recipe)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HMDS prime 140C bake HPR 504 100C bake</td>
</tr>
<tr>
<td>10</td>
<td>Gate Exposure</td>
<td>Tool: GCA Lithography</td>
</tr>
<tr>
<td></td>
<td>&quot;Verify stepper is in INTEGRATE &amp; 6” Mode&quot;</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Tool: SVG Program 1 or SSI - Develop.rcp</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mask: Hirsch IGZO 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Job: IGZODG.6in</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pass: P2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time: 2.8 sec (integrate mode)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Focus: 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Alignment Marks: N</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Inspection</td>
<td>Tool: Leica Microscope</td>
</tr>
<tr>
<td></td>
<td>Take Pictures of devices on all wafers and transfer to morbo.</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Gate Etch</td>
<td>Tool: Wet Bench - Manual</td>
</tr>
<tr>
<td></td>
<td>Pour the etchant back into bottle after use</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Chemistry: Mo etchant</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Time: Until all moly is removed (about 30 seconds)</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Inspection</td>
<td>Tool: Leica Microscope</td>
</tr>
<tr>
<td></td>
<td>Take Pictures of devices on all wafers and transfer to morbo.</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Resist Strip</td>
<td>Tool: Wet Bench</td>
</tr>
<tr>
<td></td>
<td>Solvent: PRS2000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Temp: 90C</td>
<td></td>
</tr>
</tbody>
</table>
# APPENDIX C. COMBINED DEVICE PROCESS FLOW

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
</table>
| 15   | TEOS        | Time: 5 min (each bath)  
                   Tool: P5000  
                   Chamber: A  
                   Recipe: LS1000A  
                   Thickness: 1000Å  
                   Time: 12 sec for 1 kÅ  
                   5 sec for 500 Å |
| 16   | Densify TEOS | Tool: BruceTube 5  
                   Temperature: 600C  
                   Time: 2 hours  
                   Ramp Down: Standard (not long)  
                   Recipe: 535 |
| 17   | Optional Barrier Layer | Tool: Ultratech ALD  
                   Material: Al$_2$O$_3$  
                   Thickness: 10-15nm  
                   Use 100-150 cycles, about 10 cycles per nanometer |
| 18   | S/D Lift-off Litho | Use SVG for HMDS prime ONLY  
                   SCS spinner for LOR coat (LOR 5Å 35sec @ 2k rpm)  
                   1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime  
                   HMDS prime LOR 5Å 150C bake HPR 504 100C bake |
| 19   | S/D Lift-off exposure | Tool: GCA Lithography  
                   Tool: SVG Program 1 or SSI  
                   "Verify stepper is in INTEGRATE & 6”” Mode”  
                   Mask: Hirsch IGZO 1  
                   Job: IGZODG.6in  
                   Pass: P4  
                   Time: 2.8 sec (integrate mode)  
                   Focus: 0  
                   Alignment Marks: N |
| 20   | S/D metal deposition | Tool: CVC 601  
                   Cover H1 |
### APPENDIX C. COMBINED DEVICE PROCESS FLOW

**Target:** Ti  
**Ar Flow:** 50 sccm  
**Pressure:** 6 mTorr  
**Power:** 1000 W  
**Thickness:** 50 nm  
**Presputter:** 300 sec (use shutter)  
**Dep. Time:** 300 seconds  
**Tool:** CVC 601

**Target:** Ti (TiN)  
**Ar Flow:** 20 sccm  
**Pressure:** 4.8 mTorr  
**N2 Flow:** 21 sccm  
**Power:** 500 W  
**Thickness:** 20 nm  
**Presputter:** 300 sec (use shutter)  
**Dep. Time:** 385 seconds + 15 sec with shutter closed

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Equipment</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>Inspection</td>
<td>Tool: Leica Microscope</td>
<td>Take Pictures of devices on all wafers and transfer to morbo.</td>
</tr>
<tr>
<td>22</td>
<td>Metal lift-off</td>
<td>Tool: Ultrasonic Bench</td>
<td>Don’t do tape liftoff on glass wafers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Perform tape liftoff then use ZnO dedicated petridish</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PG Remover</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>about 45 min per wafer</td>
</tr>
<tr>
<td>23</td>
<td>Inspection</td>
<td>Tool: Leica Microscope</td>
<td>Take Pictures of devices on all wafers and transfer to morbo.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Equipment</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>”6” wafers:</td>
<td></td>
<td>Send to Corning for IGZO”</td>
</tr>
<tr>
<td>25</td>
<td>MESA Litho</td>
<td>SVG (program 1) or manual dispense SSI (nodispense recipe)</td>
<td>HMDS prime 140C bake HPR 504 100C bake</td>
</tr>
<tr>
<td>26</td>
<td>MESA Exposure</td>
<td>Tool: GCA Lithography</td>
<td>Adjust alignment as necessary</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tool: SVG Program 1 or</td>
<td></td>
</tr>
</tbody>
</table>
SSI - Develop.rcp

"Verify stepper is in INTEGRATE & 6”” Mode"

Mask: Hirsch IGZO 1
Job: IGZODG.6in
Pass: P1
Time: 2.8 sec (integrate mode)
Focus: 0
Alignment Marks: N

27 Inspection Tool: Leica Microscope
Take Pictures of devices on all wafers and transfer to morbo.

28 IGZO Etch Wetbench
Etchant: DI + HCl 6:1 by volume etch-rate increases with HCl proportion. Use IGZO monitor wafer for etch-time.
Also look for visual end-point
Time: Depends on thickness
Use ZnO dedicated petridishes
This could be a very fast etch!!!

29 Inspection Tool: Leica Microscope
Take Pictures of devices on all wafers and transfer to morbo.

30 Resist Strip Use acetone + IPA on wet chemical bench
First strip off resist using acetone and then before rinsing in DI water rinse with IPA. Don’t do DI water rinse right after acetone
Use ZnO dedicated petridishes or
Tool: Wet Bench
Solvent: PRS2000
Temp: 90C
Time: 5 min (each bath)

31 Inspection Tool: Leica Microscope
Take Pictures of devices on all wafers and transfer to morbo.

32 S/D Lift-off Litho Use SVG for HMDS prime ONLY
HMDS prime LOR 5A 150C bake
HPR 504 100C bake
SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm)
1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime

33 S/D Lift-off exposure
Tool: GCA Lithography Adjust alignment as necessary
Tool: SVG Program 1 or SSI "Verify stepper is in INTEGRATE & 6” Mode"
Mask: Hirsch IGZO 1
Job: IGZODG.6in No post develop bake
Pass: P4
Time: 2.8 sec (integrate mode)
Focus: 0
Alignment Marks: N

34 S/D metal deposition
Tool: CVC 601 Cover H2
Target: 2 - Molybdenum
Ar Flow: 20sccm
Pressure: 2.6mTorr
Power: 1000W
Thickness: 50nm
Presputter: 300 sec (use shutter)
Dep. Time: 200 seconds
Tool: CVC 601
Target: 1 Al/Si
Ar Flow: 20 sccm
Pressure: 5mTorr
Power: 1000 W
Thickness: 250nm
Presputter: 300 sec (use shutter)
Dep. Time: 300 seconds

35 Inspection Tool: Leica Microscope Take Pictures of devices on all SPC wafers and transfer to morbo.

36 Metal lift-off Tool: Ultrasonic Bench Don’t do tape liftoff on glass wafers
APPENDIX C. COMBINED DEVICE PROCESS FLOW

Perform tape liftoff then use ZnO dedicated petridish
PG Remover
about 45 min per wafer

37 Inspection Tool: Leica Microscope
Take Pictures of devices on all SPC wafers and transfer to morbo.

38 Passivation/ TG Dielectric Tool: P5000 SMFL low stress 1kA TEOS recipe
Chamber: A Use bare Si monitor wafers for deposition rate

TEOS Recipe: LS1000A
Thickness: 1000A
Time: 12 sec for 1 A
  5 sec for 500 A

39 Passivation / TG Dielectric anneal Tool: BruceTube 7
Temperature: 400C O2
Time: 8 hours
Ramp Down: 2 hour O2
Recipe: 522

40 Optional Barrier Layer Tool: Ultratech ALD
Use 100-150 cycles, about 10 cycles per nanometer
Material: Al2O3
Thickness: 10-15nm

41 G/S/D contact litho SVG (program 1) or manual dispense SSI (nodispense recipe)
HMDS prime 140C bake HPR 504
100C bake

42 G/S/D contact exposure Tool: GCA Lithography
Adjust alignment as necessary

Tool: SVG Program 1 or SSI
"Verify stepper is in INTEGRATE & 6”” Mode”

Mask: Hirsch IGZO 3
Job: IGZODG.6in
No post develop bake
Pass: P4
Time: 2.8 sec (integrate mode)
Focus: 0
## APPENDIX C. COMBINED DEVICE PROCESS FLOW

<table>
<thead>
<tr>
<th>Step</th>
<th>Process Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>43</td>
<td>Inspection</td>
</tr>
<tr>
<td></td>
<td>Tool: Leica Microscope</td>
</tr>
<tr>
<td>44</td>
<td>G/S/D contact etch</td>
</tr>
<tr>
<td></td>
<td>HF MOS grade 10:1 or PAD etch</td>
</tr>
<tr>
<td></td>
<td>Find etch rate first from monitor wafers</td>
</tr>
<tr>
<td>45</td>
<td>Inspection</td>
</tr>
<tr>
<td></td>
<td>Tool: Leica Microscope</td>
</tr>
<tr>
<td>46</td>
<td>Resist Strip</td>
</tr>
<tr>
<td></td>
<td>Tool: Wet Bench</td>
</tr>
<tr>
<td></td>
<td>Solvent: PRS2000</td>
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<tr>
<td></td>
<td>Temp: 90C</td>
</tr>
<tr>
<td></td>
<td>Time: 5 min (each bath)</td>
</tr>
<tr>
<td>47</td>
<td>TG Metal deposition</td>
</tr>
<tr>
<td></td>
<td>Tool: Al Flash Evaporator</td>
</tr>
<tr>
<td></td>
<td>Thickness: 250 nm</td>
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<tr>
<td>48</td>
<td>TG Litho</td>
</tr>
<tr>
<td></td>
<td>SVG (program 1) or manual dispense SSI (nodispense recipe)</td>
</tr>
<tr>
<td>49</td>
<td>TG Exposure</td>
</tr>
<tr>
<td></td>
<td>Tool: GCA Lithography</td>
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<tr>
<td></td>
<td>Tool: SVG Program 1 or SSI</td>
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<tr>
<td></td>
<td>Mask Hirsch IGZO 2</td>
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<tr>
<td></td>
<td>Job: IGZODG.6in</td>
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<tr>
<td></td>
<td>Pass: P2</td>
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<tr>
<td></td>
<td>Time: 2.8 sec (integrate mode)</td>
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<td></td>
<td>Focus: 0</td>
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<tr>
<td></td>
<td>Alignment Marks: N</td>
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<tr>
<td>50</td>
<td>Inspection</td>
</tr>
<tr>
<td></td>
<td>Tool: Leica Microscope</td>
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<tr>
<td>51</td>
<td>Top Gate Etch</td>
</tr>
<tr>
<td></td>
<td>Tool: Al Etch Wet Bench</td>
</tr>
<tr>
<td></td>
<td>Chemistry: Al etchant</td>
</tr>
<tr>
<td></td>
<td>Time: Until all Al is removed</td>
</tr>
<tr>
<td>52</td>
<td>Resist Strip</td>
</tr>
<tr>
<td></td>
<td>Tool: Wet Bench</td>
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</tbody>
</table>
Solvent: PRS2000
Temp: 90C
Time: 5 min (each bath)

<table>
<thead>
<tr>
<th>No.</th>
<th>Stage</th>
<th>Tool:</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>53</td>
<td>Inspection</td>
<td>Leica Microscope</td>
<td>Take Pictures of devices on all SPC wafers and transfer to morbo.</td>
</tr>
<tr>
<td>54</td>
<td>Final Testing</td>
<td></td>
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