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Wireless Interconnects for Intra-chip & Inter-chip Transmission

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Wireless Interconnects for Intra-chip & Inter-chip Transmission

By

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requirements of the Degree of

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Abstract

With the emergence of Internet of Things and information revolution, the demand of high performance computing systems is increasing. The copper interconnects inside the computing chips have evolved into a sophisticated network of interconnects known as Network on Chip (NoC) comprising of routers, switches, repeaters, just like computer networks. When network on chip is implemented on a large scale like in Multicore Multichip (MCMC) systems for High Performance Computing (HPC) systems, length of interconnects increases and so are the problems like power dissipation, interconnect delays, clock synchronization and electrical noise. In this thesis, wireless interconnects are chosen as the substitute for wired copper interconnects. Wireless interconnects offer easy integration with CMOS fabrication and chip packaging. Using wireless interconnects working at unlicensed mm-wave band (57-64GHz), high data rate of Gbps can be achieved.

This thesis presents study of transmission between zigzag antennas as wireless interconnects for Multichip multicores (MCMC) systems and 3D IC. For MCMC systems, a four-chips 16-cores model is analyzed with only four wireless interconnects in three configurations with different antenna orientations and locations. Return loss and transmission coefficients are simulated in ANSYS HFSS. Moreover, wireless interconnects are designed, fabricated and tested on a 6'' silicon wafer with resistivity of 55Ω-cm using a basic standard CMOS process. Wireless interconnect are designed to work at 30GHz using ANSYS HFSS. The fabricated antennas are resonating around 20GHz with a return loss of less than -10dB. The transmission coefficients between antenna pair within a 20mm x 20mm silicon die is found to be varying between -45dB to -55dB.

Furthermore, wireless interconnect approach is extended for 3D IC. Wireless interconnects are implemented as zigzag antenna. This thesis extends the work of analyzing the wireless interconnects in 3D IC with different configurations of antenna orientations and coolants. The return loss and transmission coefficients are simulated using ANSYS HFSS.

Publications from the Present Work

1. M. S. Shamim, N. Mansoor, R. S. Narde, V. Kothandapani, A. Ganguly, and J. Venkataraman, "A Wireless Interconnection Framework for Seamless Inter and Intra-Chip Communication in Multichip Systems," *IEEE Trans. Comput.*, pp. 1–14, 2016.
2. R. S. Narde, J. Venkataraman and A. Ganguly, "Feasibility study of Transmission between Wireless Interconnects in Multichip Multicore systems," Proceedings IEEE International Symposium on Antenna and Propagation and USNC-URSI Radio Science Meeting, San Diego, 2017 (paper accepted).

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List of Abbreviations

AMC	Artificial Magnetic Conductor
ANT	Antenna
AoC	Antenna-on-Chip
BCB	Benzo-cyclo-Butene
BEOL	Back End of Line
BOE	Buffered Oxide Etch
CMOS	Complementary Metal-Oxide-Semiconductor
CPW	Co-planar Waveguide
EBG	Electromagnetic Band-Gap
FCC	Federal Communications Commission
FEOL	Front End of Line
GND	Ground
GSG	Ground-Signal-Ground
HFSS	High Frequency Structure Simulator
HPC	High Performance Computing
IC	Integrated Circuit
IoE	Internet of Everything
IoT	Internet of Things
ITRS	International Technology Roadmap for Semiconductors
MCMC	Multichip Multicores
MIMO	Multiple Input Multiple Output
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor

NoC	Network on Chip
PCB	Printed Circuit Board
PEC	Perfect Electric Boundary
PNA	Programmable Network Analyzer
RFIC	Radio Frequency Integrated Circuit
RIT	Rochester Institute of Technology
SMFL	Semiconductor and Microelectronics Fabrication Laboratory
SOI	Silicon On Insulator
TSV	Through Silicon Via
UWB	Ultra-Wide Band
WLAN	Wireless Local Area Network
WNoC	Wireless Network on Chip

1. Introduction

1.1. Moore's Laws & Dennard's Scaling

In 1965, Gordon Moore, one of the founder of Intel, reported prediction that the number of components in a chip will be doubled every two years [1]. This statement is known as Moore's law. Over the years, the size of MOSFETs has become smaller and smaller, so as to keep up with the trend of doubling number of transistors in a chip. Now, it has become so small that it is reaching atomic limit [2], [3]. This means that the Moore's law is on the verge of collapse. Researchers are implementing a 3D IC arrangement, which is discussed in later section, to keep up the Moore's trend of doubling the number of components every 2 years.

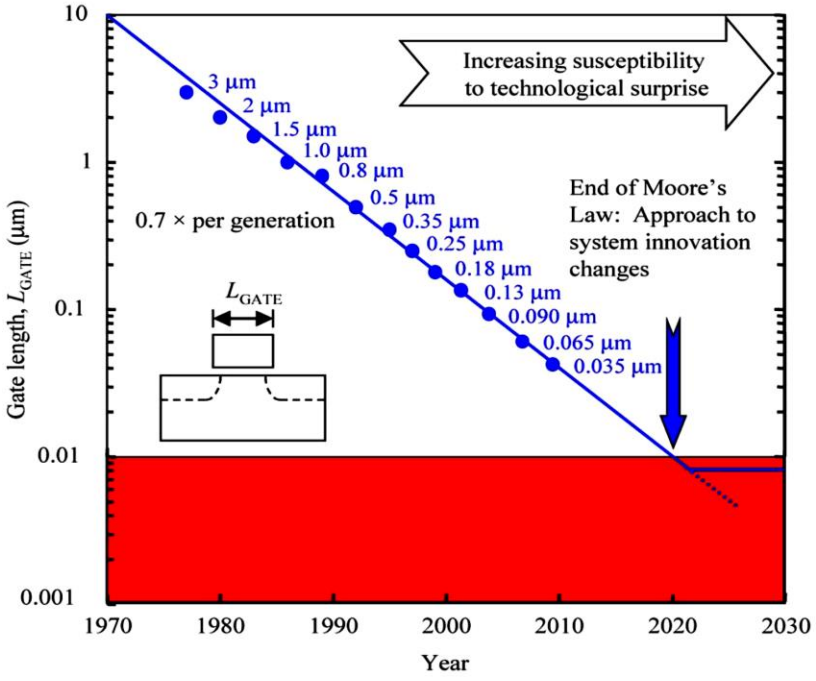


Figure 1-1: Reduction of gate length of transistor [3].

Talking about decades old trends, there was one more which failed in 2004 [2]. It was known as Dennard's scaling theory. Robert Dennard and his team at IBM in 1974 published a

paper [4] stating a relationship between the parameters of MOSFET. The parameter includes the dimension, voltage, current, power, operating frequency. Dennard's paper emerged an industry standard for MOSFET scaling for nearly three decades [5]. It provided a way to increase the operating frequency and at the same time reducing the size of transistors. Till 2004, the Dennard's scaling worked good. It showed a way to engineers to increase the operating frequency of transistor till 3 to 4 GHz. That was it, and it collapsed due to unbearable heat density, and limits to switching voltage. The collapse of Dennard's scaling forced the semiconductor industry to move from single core to multicore systems in order to keep up with the Moore's trend [2].

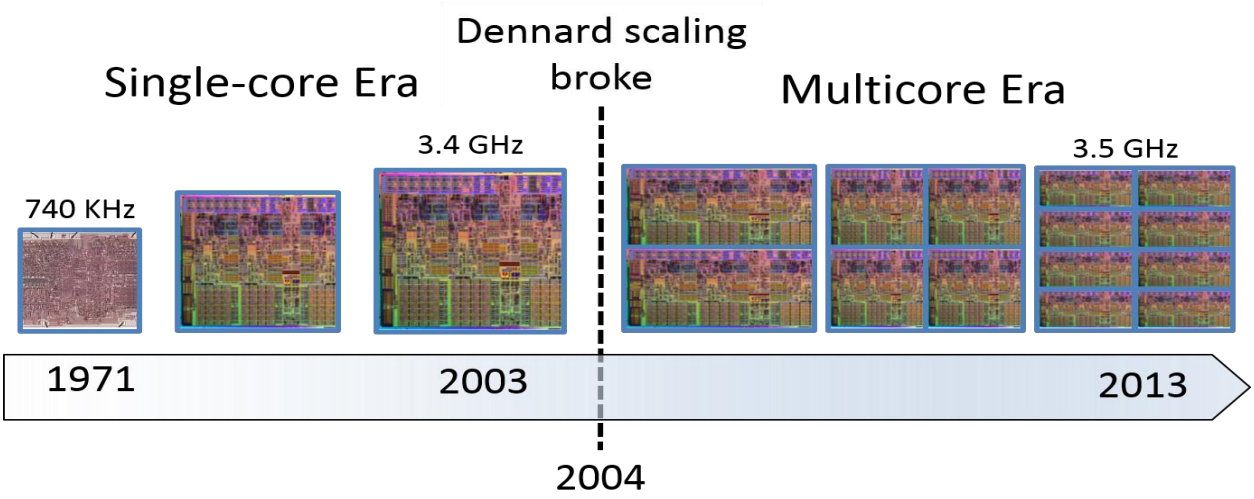


Figure 1-2: Chronological progress towards multicore systems.

Multicore processors work on the concept of distributed or parallel processing. A process is distributed in between multiple computing units or cores. The concept of multicore systems & parallel processing are alternatives to overcome the collapse of Dennard's scaling, however, it is limited by the communication between cores [2]. Since, the cores require to communicate or exchange data with other cores for processing data in parallel, it is a must to have a high speed data exchange link between cores.

1.2. Multicore systems

Since, the collapse of Dennard's scaling the performance of computing systems are improved not by increasing the operating frequency, but by dividing a processor into multiple independent processing units known as cores. In 2004, Intel was the first to move towards multicore systems in a processor [2]. The layout (Figure 1-3) of the processor shows eight similar blocks of independent cores on a single silicon die.

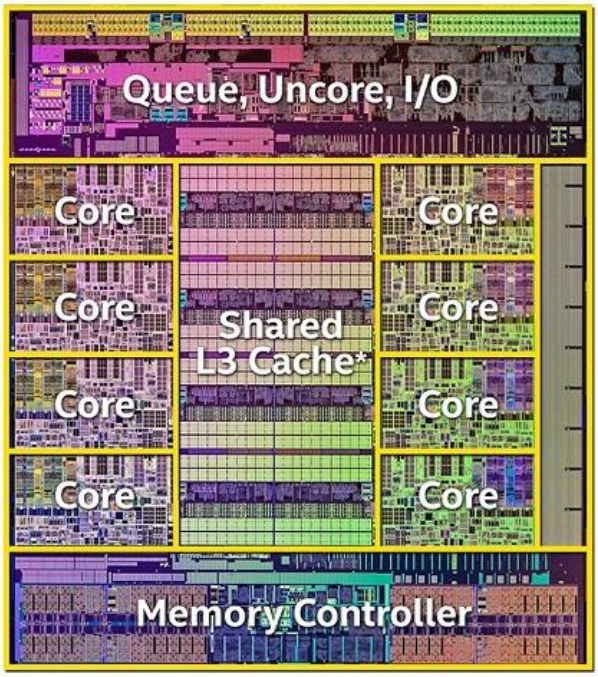


Figure 1-3: Eight cores on Intel Core i7-5960X Extreme Edition processor [6].

Multicores systems can be fabricated in two ways: on a Single silicon wafer, or on multiple silicon wafers. Fabricating multiple cores on a single standard sized silicon wafer has a problem. If any core in the middle of the wafer gets defective it cannot be used. The whole wafer becomes defective. This results in lower yield, moreover the single wafer design is expensive to maintain. If there is any problem, then technician should have to replace the whole wafer.

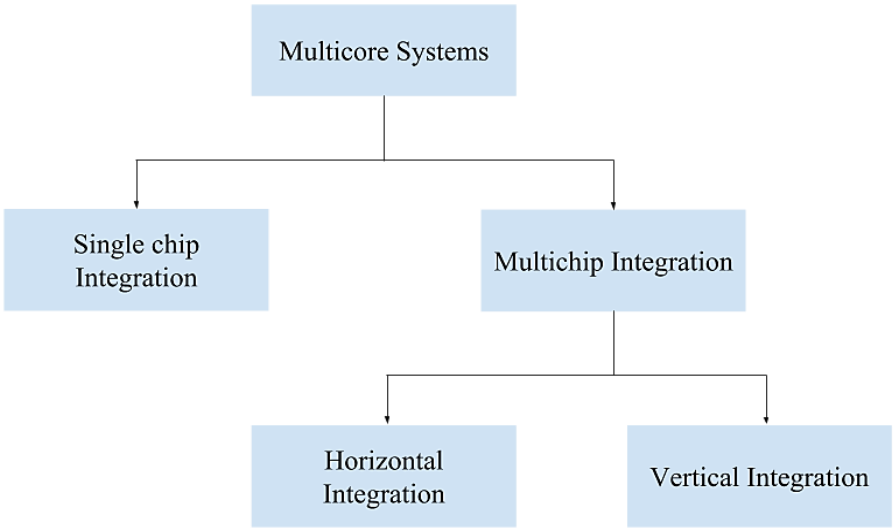


Figure 1-4: Multicore systems.

On the other hand, fabricating multiple cores of a processor on multiple silicon wafers has relatively high yields, and more flexible placing chips on Printed circuit board (PCB). Therefore, the multichip multicore (MCMC) design is popular among processor architects. Furthermore, multichip multicore design can be divided in two types depending on integration of multiple chips: Horizontal integration and Vertical integration. The horizontally integrated multicore systems are commonly called Multichip Multicore (MCMC) system. Of late, there has been great interest seen in designing vertical integrated multicore systems, also known as 3D IC, which are discussed in later section.

1.2.1. Multichip Multicore systems

It is abbreviated as MCMC systems. It has multiple cores distributed in multiple chips on a interposer or PCB horizontally. This type of systems is mostly used in High Performance Computing (HPC) centers like datacenters, weather forecasting centers, etc. An example of MCMC system is shown in Figure 1-5. It can be seen that system is divided into 4 processors or

sockets. Furthermore, a socket is divided into multiple cores. Each core has a separate computing unit along with its cache memory. Each core in a socket is connected with wired copper interconnects. Each socket is connected using metal interconnects. Generally, HPC systems house more than 10 such processors working in parallel.

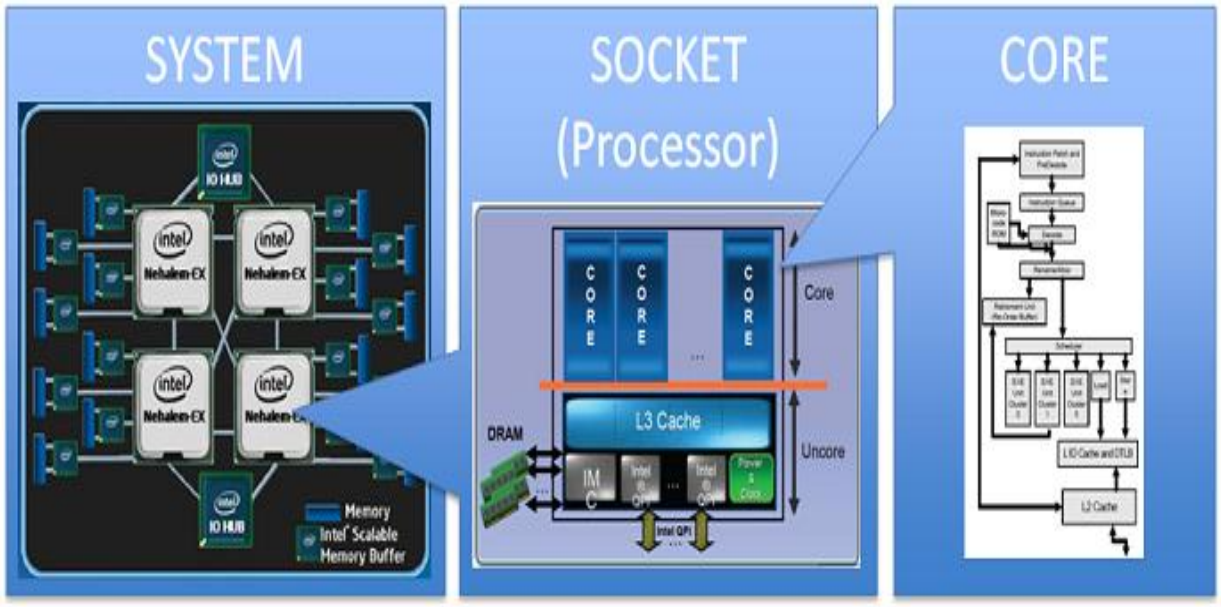


Figure 1-5: Horizontal placed Multichip Multicore systems [7].

As number of sockets increase, the system demands more space to distribute the chips horizontally. This in turn requires longer metal interconnects for connections which results in delay and ohmic losses. To maintain dissipating signal requires additional circuitry such as repeaters. One emerging solution to this problem is to integrate cores vertically.

1.2.2. Vertical Integration or 3D IC

As mentioned in ITRS [8] that in big cities when the real estate on ground is fully used, people started building in "vertical dimension". Similar strategy is adopted by engineers in 3D IC. Recently flash memory manufacturers have demonstrated 3D memory units [9]. In the coming decade, 3D IC will become industry standard for computing units.

In a 3D IC, active silicon layers are placed one over other. In this way, a new dimension of increasing the performance of processor is devised. This 3D configuration, however, complicates the communication interfaces. A new type of metal interconnect is used which transfers signals between cores through the bulk silicon layer, therefore known as Through-Silicon Via or TSV or 3D via. A 3D IC is shown in Figure 1-6 with three active silicon layers as Tier 1,2 and 3. TSV can also be seen in the Figure 1-6 which are connected silicon layers.

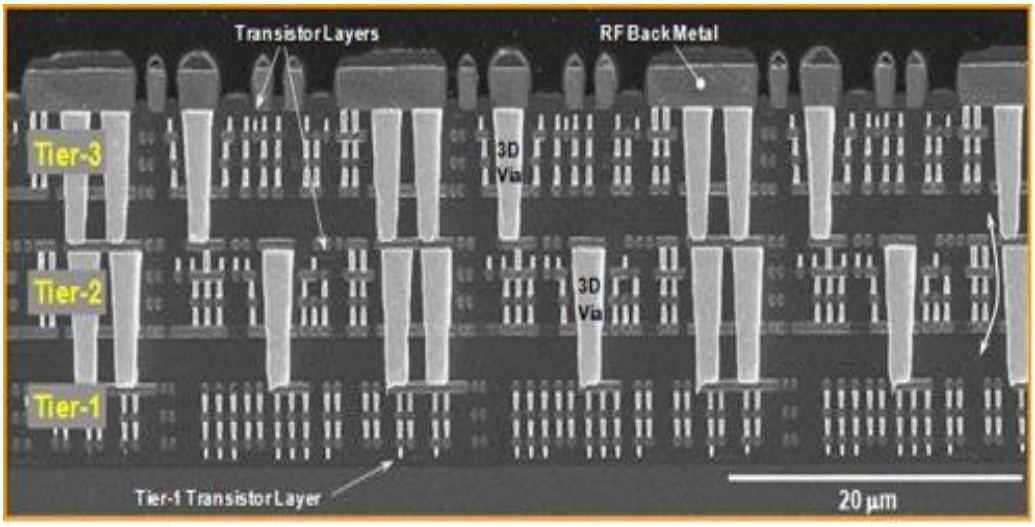
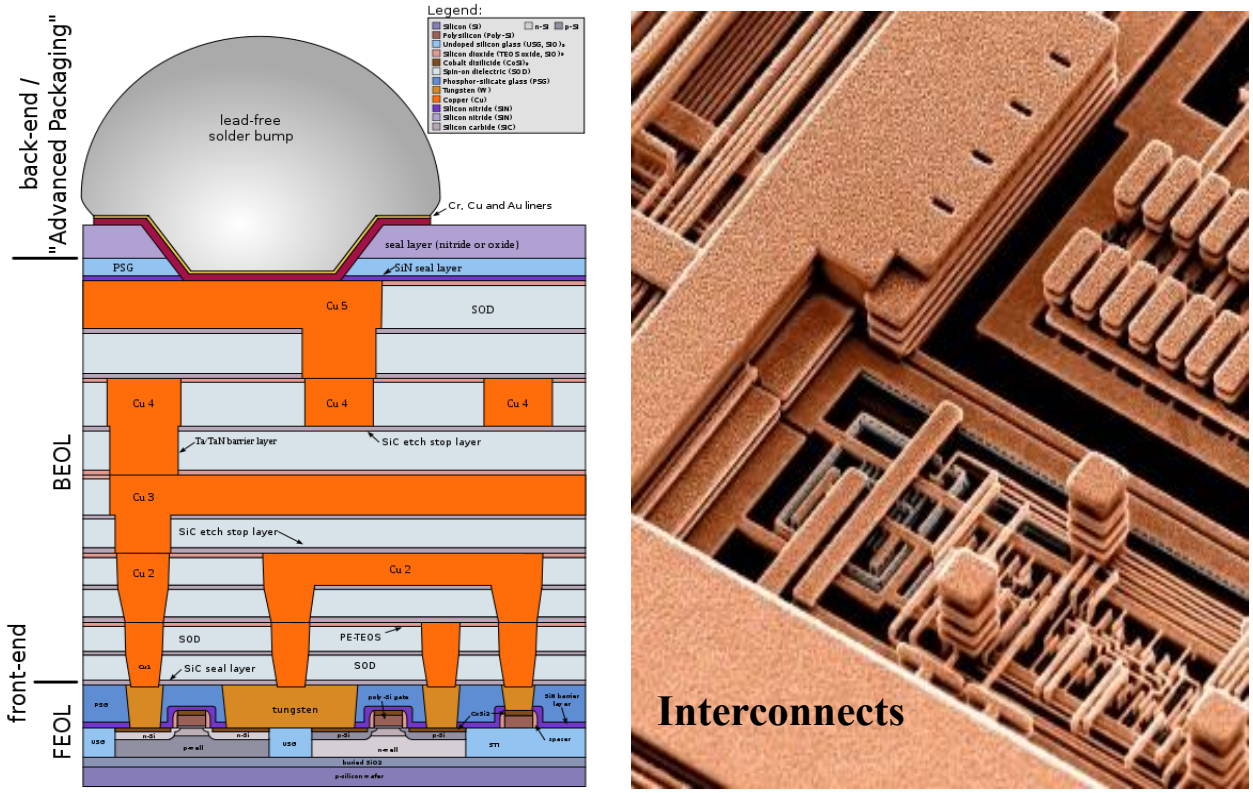


Figure 1-6: Vertically placed Multichip Multicores systems [10].

1.3. Network on Chip

The digital circuitry, mostly MOSFET, are fabricated on silicon wafer using variety of standard process technologies. This design is called a Front End of Line (FEOL). The front end layer is nothing but two dimensional placements of MOSFET on a silicon wafer. The front end does not include connections between different MOSFETs or other devices. A metal wire or interconnect is fabricated to support the transfer of power, signal and data. Metal used to fabricate interconnects are Copper. Metal interconnect are designed in Back End of Line (BEOL) which is on top of the MOSFET layer or FEOL. FEOL and BEOL are shown in Figure 1-7. These Metal

interconnect does not only provide connections between MOSFET in FEOL, but also connects to the outer package pins using a solder bump. The lead solder bump can be seen in Figure 1-7(a).



(a) (b)

Figure 1-7: Wired interconnects. (a) chip cross-section view [11]; (b) 3D view [12].

Till the start of 21st century, each device on chip were connected with separate interconnects. This point-to-point communication made interconnect design bulky and cumbersome to fabricate. Designing interconnects quickly became toil because connection should be made between millions, if not billions, of transistors in different layers. Moreover, the scaling of interconnects with smaller technology node was problematic [13] due to increasing power consumption [14], delay, electro-mitigation, electrical noise and clock synchronization [15]. A researcher from Intel noted in 1995 that the efficient implementation of high performance computing systems depends on the metal interconnects [13]. Considering limitations of metal

interconnects, a new interconnect system was proposed in 2002 which implemented networks of interconnects based on computer networking [15]. Switches, routers, hubs and other networking devices were designed on chip to support the Network-on-chips (NoC). Moreover, different networking algorithms like mesh, bus, et al. based on large computer networks were implemented to improve the interconnect performance. It is really a smart way to overcome interconnect problems in a computer chip. It is still used in today's commercial computing systems.

As the transistors become smaller and smaller with technology nodes, the interconnects become thinner and thinner, consequently more resistive which causes heat dissipation. It has been studied that the metal interconnects alone consume 30-60% of the dynamic power of the chip [2]. Long copper interconnects in multi-hop networks for data transfer results in high latency and power loss [16]. To make the signal go long distances, repeaters or buffers are introduced which further increases the delay between the interconnects. Furthermore, it is noted that in a chip, the repeaters take more space than the computing devices [2].

To cope with power consumption by metal interconnects, designers have created multi-width multi-layer interconnects. In process technology of 22nm, number of interconnect layers can go up to 16 of different width [2]. Still, interconnects consume significant amount of power and takes up considerable space in a sub-micron world. Therefore, it is required to research new techniques for improving current infrastructure of interconnects in high performance multicore systems. Researchers have proposed Wireless Network on Chip (WNoC), which is discussed in later section, in order to curb above mentioned drawbacks of Wired networks.

1.4. International Technology Roadmap for Semiconductors (ITRS) 2015

ITRS [8] is a set of guidelines consist of future developments and predictions about semiconductor devices written by the experts from semiconductor industries across Europe, Japan, Korea, Taiwan, and USA. The main focus of the ITRS 2.0 is Internet of Everything (IoE), or otherwise known as Internet of Things (IoT). "IoE is nothing more than a distributed computer system" [8] with memories located remotely. This leads to improvement in technologies related to IoT which includes datacenters, communications, et al.

According to ITRS predictions, the demand for data processing is going to increase tremendously by 2029. It is predicted that number of cores on one socket of datacenter will increase 30 times. Moreover, the memory storage will increase to 4000 times. The predicted augmentation of computing systems will result to another projection of power consumption by future data giants by 2.5 times increment. A table from the ITRS summary is shown in Table 1. According to [2] in 2011, the datacenters in USA consumed 2.2% of its total power generated. Current consumption of power is already substantial. It will be difficult to cope up with increase in power consumption.

In this way, a new efficient and robust communication technology is needed to take care of the future demands. Moreover, it has been stated in ITRS that the wired interconnects inside a chip and communication interfaces between chips are bulky, increases latency when interconnects are long, and increases operating temperature due to heat generated. Therefore, research for wireless interconnects/antennas for semiconductor circuits have been motivated.

Table 1: Predictions provided by ITRS 2015 [8].

Categories	Year	2015	2017	2019	2021	2023	2025	2027	2029
Power	Energy source (B = battery; H = energy harvesting)	B	B	B + H	B + H	B + H	B + H	B + H	B + H
	Lowest VDD Used By Components (V)	0.8	0.75	0.7	0.65	0.65	0.55	0.45	0.45
	Deep suspend current of MCU (nA)	100	72	52	38	27	20	14	10
	Conversion efficiency of DC-to-DC Conversion (%)	80%	82%	86%	88%	89%	91%	93%	95%
	Spatial Power Density of DC Converter (W/mm^2)	1	1.17	1.36	1.59	1.85	2.16	2.52	2.94
	Peak Current Consumed by Connectivity Interface (mA)	50	19.28	7.44	2.87	1.11	0.43	0.16	0.06
	Transmission Power per bit (µW/bit)	2.48	0.972	0.381	0.149	0.058	0.023	0.009	0.004
Form factor	Module footprint (mm2)	500	500	280	179	115	73	47	30
Performance	MCU Number of Cores	1	1	1	1	1	1	1	1
	MCU Current / Operation frequency (mA/MHz)	30	21.7	15.7	11.3	8.9	7.7	6.7	5.8
	Max MCU Frequency (MHz)	200	235	277	306	316	327	338	350
	MCU Flash Size (KB)	1024	1024	2048	4096	4096	8192	8192	8192
	MCU Dhrystone MIPS (DMIPS)	200	242	293	354	429	519	628	759
Peripheral	Number of Sensors Integrated to System	4	8	10	12	12	13	13	13
	Max Sensor Power (µW)	2850	1397	1009	729	617	522	442	374

1.5. Wireless Network on chip

When the traditional NoC grows too large into a multi-hop link between two distant locations, the limitations of metal interconnect becomes significant [17]. So, the traditional NoC limits the on chip communication system design. As discussed in [13], the performance of computing systems is limited by the metal interconnects. Wireless Network on Chip (WNoC) can help to cope with the barriers in NoC. It has already been demonstrated using modelling and simulations in [17], [18], [19] and [20] that WNoC improves the throughput and decrease the energy consumption. Moreover, the routing algorithm used by the Wireless network on chip can reduce the latency of communication.

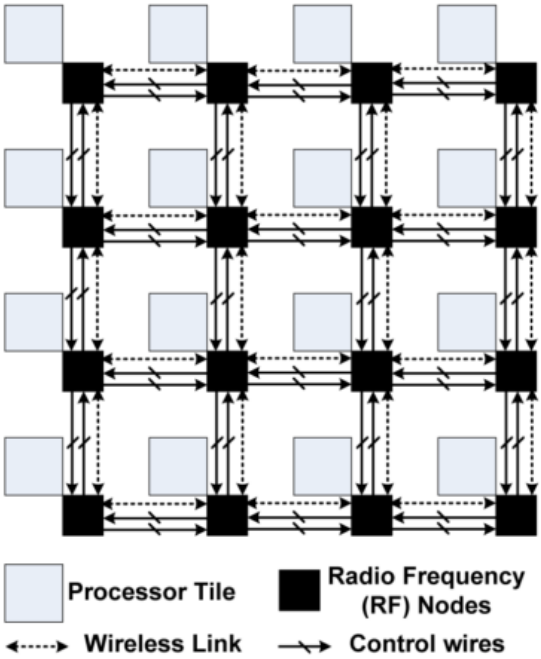


Figure 1-8: Block diagram representation of 2D mesh WNoC [17].

As shown in previous sections, collapsing Moore's law and predictions by ITRS 2015 must be considered in order to keep up with increasing demand for optimum and faster processing. Photonics is another technology with advantages of low latency, high bandwidth which may overcome the limitations of wired metal interconnects. However, Photonics integrated circuits has to overcome the technological challenges of size reduction of optical components, and manufacturing challenges to be viable for mass production. Currently the cost of fabricating is high, and size of interconnects is large for commercial purpose. Silicon Photonics is currently at an early stage where silicon electronics was in 1970 [21], [22].

According to Shannon–Hartley theorem, high speed data communications requires large bandwidth. The unlicensed bandwidth of present high speed communication system is limited according to band of 2.4 GHz or 5 GHz. Therefore, Federal Communications Commission (FCC) has allocated an unlicensed 57-64GHz band [23] with greater than 100MHz band channels in USA.

This millimeter wave frequency band is commonly known as 60 GHz frequency band, since it is centered around 60 GHz. The allocation made possible the realization of ultrahigh speed communication systems. Moreover, the range of frequency helps design an antenna of very small size (of micrometer dimensions) which is feasible for fabricating antenna on chip. In this way, small wireless interconnects for WNoC can be implemented on semiconductor devices.

One more advantage of Wireless is obviously it is wireless. No wired interconnect is required to transfer data from one chip to another. The fact that different data transfer protocols are used at different interfaces, so data is converted into specific blocks corresponding to interfaces which increase the delay and complexity. But with direct wireless links, complexity and delay will reduce. This will increase the performance, and save chip space of CMOS devices.

Since, here, the transmission of 60 GHz band is used for short distance with a maximum of 10 meters. Moreover, the 60 GHz band cannot even penetrate concrete walls. It has a high attenuation rate in atmosphere. All above mentioned reasons is going to decrease the chances of Spoofing (unauthorized access using wireless protocols), thereby increasing security. Another advantage is the fabrication process of antenna on chip (AoC) is compatible with existing CMOS technology. The antennas are easily fabricated using standard process technology used by the semiconductor industry today.

Since the beginning of wireless communication, it has touched the life of everyone. Most of the communication systems of the world depends on wireless technology. This means that the wireless technology has become mature and stable. There has been many research already done. This is advantageous for wireless researchers. Many wireless technologies like MIMO systems,

beam steering, etc. are yet to be implemented on chip. This creates opportunity for researchers to investigate the ways to connect chips wirelessly.

1.6. Silicon

It is the most dominated substrate for designing microelectronics circuitry due to its unique properties. Some of the properties are described below.

Figure 1-9: Silicon wafers in a wafer boat [24].

1. **Abundantly available:** One of the simplest reason to use silicon for semiconductor industry is because silicon is available to us as silica (sand) in abundance. Silicon makes up more than 25% of the earth's crust. There are standard metallurgical processes devised, over the years, to obtain metallurgical-grade silicon from sand (silica). Using Czochralski process, metallurgical-grade silicon is converted into electronics-grade silicon. To get ultra-pure silicon crystals, Float zone method is implemented following the Czochralski process.
2. **High quality native-oxide formation:** Silicon forms a native oxide (SiO_2) by reacting with water (H_2O) or dry oxygen (O_2), though, at high temperatures from 900°C to 1100°C.

This property outshines silicon in the list as SiO_2 acts as high quality electrical insulator. The dielectric strength of thin layer (≈1μm) SiO_2 on silicon varies from 5-8 MV/cm. Therefore, SiO_2 is used as insulation in fabrication process. It can also be used to mask a part of wafer while treating another part. One more significance is the silicon-dioxide over silicon can be selectively etched using a Buffered Oxide Etch (BOE) solution, means the underneath silicon is not etched.

3. **Doping can easily change the conductivity:** The different conductivity is required depending on different applications, so a good microelectronics material should be able to change its electrical properties without much hassle. Silicon can be doped with impurity like Boron, Phosphorous, Arsenic to change the conductivity of the wafer. Boron impurity acts as acceptor impurity and used to make hole enriched or p-type silicon wafer. Phosphorous and Arsenic act as donor impurity which makes electron enriched or n-type silicon wafer.
4. **Chemically resist** – Due to crystalline structure of silicon, it is chemically inert. The durability of silicon microelectronics is more than other semiconductor materials can offer.

As seen above, silicon is most appropriate material for semiconductor industry. However, when it comes to microwave or millimeter wave applications, silicon is a hostile material. Following are some of the reasons:

1. **High dielectric constant** – Silicon has a high dielectric constant (ε_r) of 11.7 [24]. This extreme property of silicon makes it a tough material to implement a high frequency circuit or antenna. Because of high dielectric constant, most of the radiation of antennas goes into silicon. Therefore, changing the radiation pattern significantly.

2. **Lossy due to high conductivity –** Electronics grade silicon is doped, so it is conductive (generally ρ of Si wafers varies from 5mΩ-cm-30Ω-cm [25], so σ varies from 0.03S/cm to 200S/cm), therefore acts as a lossy medium. *Note:* High and ultra-high resistivity silicon [24] can be used for RFIC working at GHz and THz. High resistivity Si wafers are expensive because requires additional process of filtration of impurity (Float Zone process).

1.7. Review of Antenna on chip as Wireless Interconnects

The research on Antenna on Chip (AoC) is going on for more than two decades now. One of the earliest implementation was planar microstrip antenna array [26] in 1986. It was implemented with a 95GHz oscillator circuit on a very high resistivity substrate (ρ=10000Ω-cm). Later in 2000, AoC was implemented with an aim to demonstrate the idea of wireless clock distribution in digital integrated circuits [27].

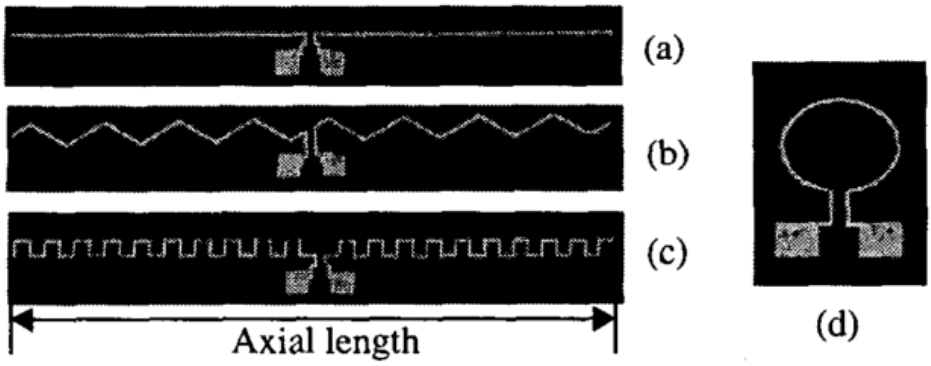


Figure 1-10: Antenna on chip [27] (a) Dipole (b) Zigzag (c) Meander (d) Loop. Axial length=2mm.

Another modified form of zigzag antenna shown in Figure 1-10 (b) is provided in [28]. Figure 1-11 shows the design of dipole antenna and substrate cross-section. This antenna showed promising results for being an omnidirectional antenna at 15 GHz.

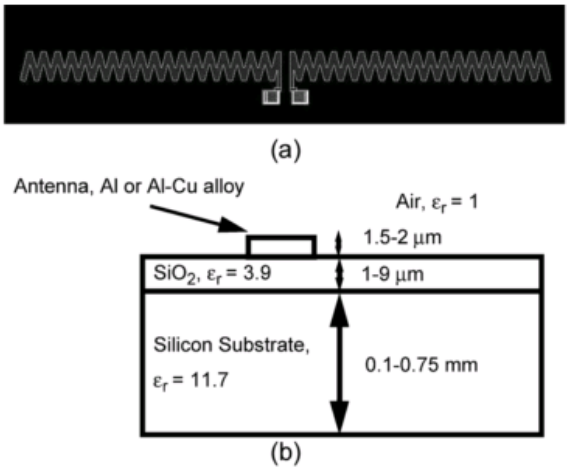


Figure 1-11: (a) Zigzag antenna on silicon wafer [28], (b) Cross-section of silicon wafer.

Above shown dipole antenna is modified into a monopole [29] with long sleeves for ground shown in Figure 1-12. This antenna was tested at frequency centered around 6 GHz. Despite little change in radiation pattern of monopole, its performance is similar to the dipole. Moreover, monopole antenna takes less space than dipole antenna shown above.

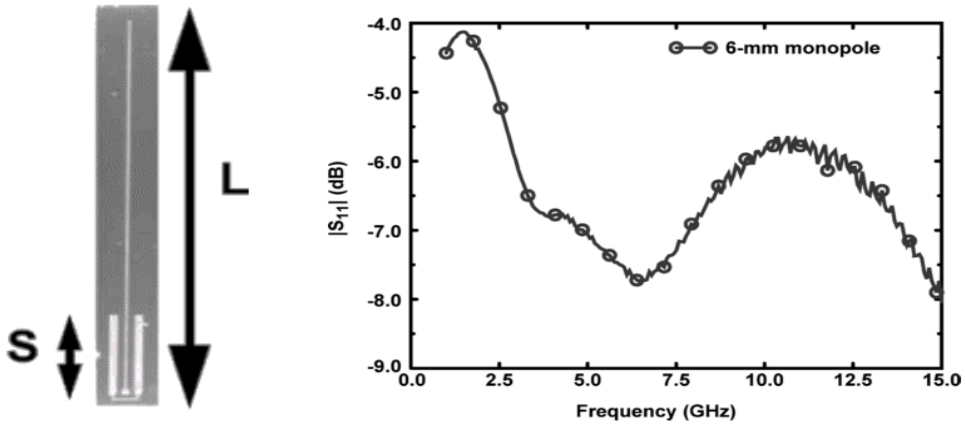


Figure 1-12: Monopole antenna with its return loss [29]. L=6mm and S=0.6mm.

All aforementioned antennas do not include feed, but excited by GSG probes. A zigzag antenna with co-planar waveguide (CPW) feed was designed in [30]. It is shown in Figure 1-13. The reason for choosing CPW feed is low loss at high frequencies. Moreover, the CPW feed can

be easily fabricated on a single layer without a bottom ground plane, unlike microstrip feed. The zigzag antenna is optimized and simulated to work at 60GHz. It was simulated in ANSYS HFSS[31].

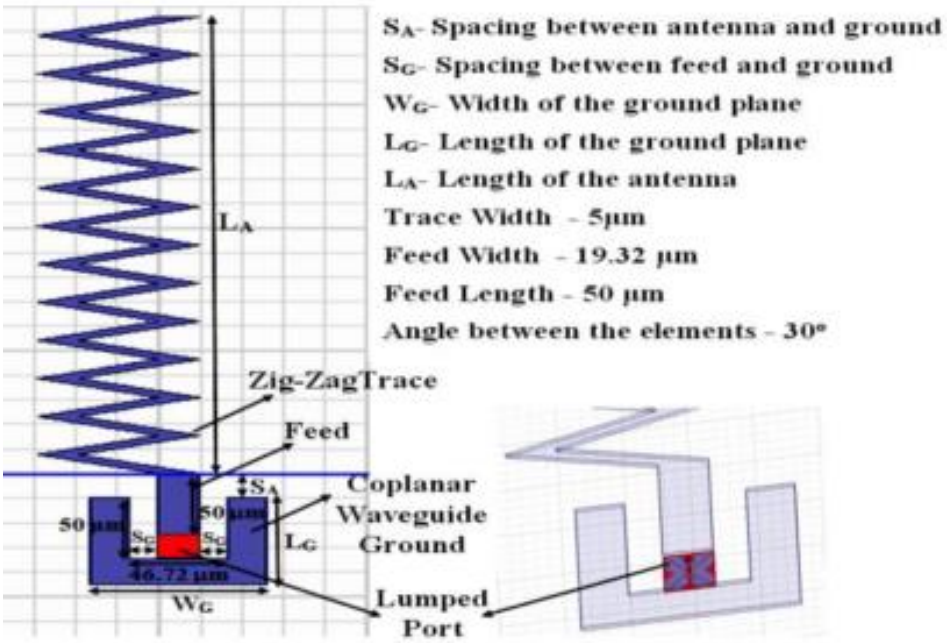


Figure 1-13: CPW-fed zigzag antenna [30].

A loop antenna is also designed on silicon wafer using CMOS technology in [32]. The antenna is shown in Figure 1-14. The antenna is simulated to work at 60GHz. The loop antenna uses multiple-layer fabrication. One half was fabricated at the top layer of BEOL of chip, and another half at the bottom of BEOL of chip. It is fed by Ground-Signal-Ground (GSG) probe.

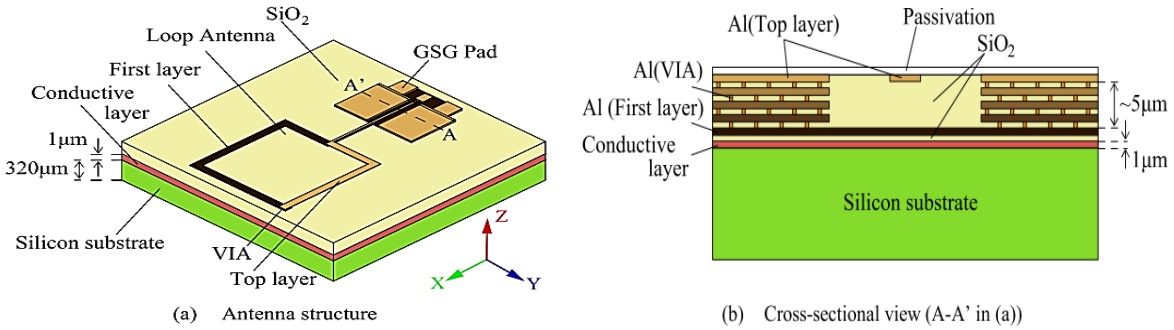


Figure 1-14: Loop Antenna designed on silicon [32].

In [33], it is shown that the rectangular loop antenna has low profile, easy to fabricate, and dual band characteristic. It is designed for WLAN applications with an omnidirectional pattern. A CPW-fed loop antenna based on [33] is proposed in later chapter to take advantage of dual band or it can be modified for a UWB antenna which is required for 60GHz frequency band.

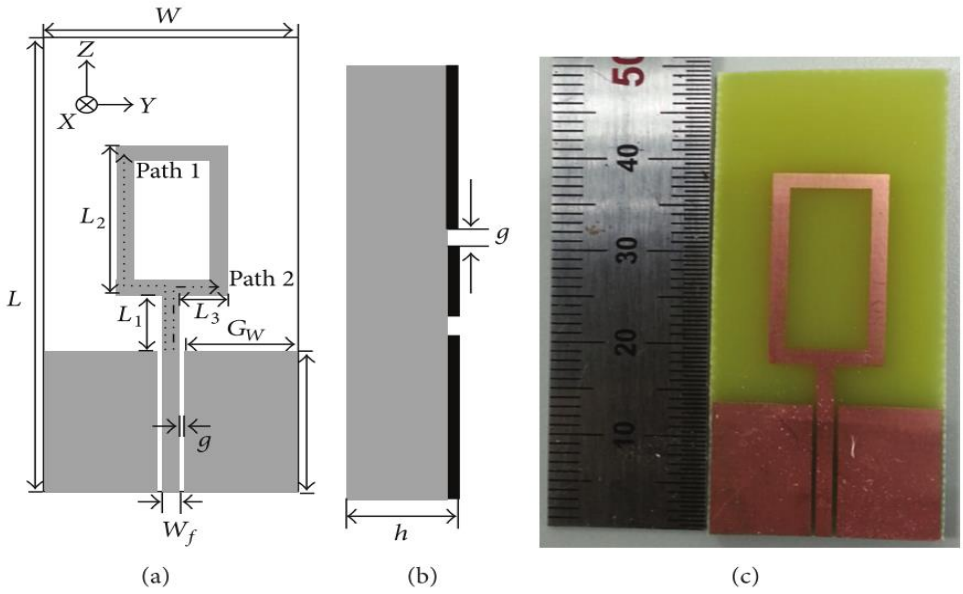


Figure 1-15: Loop antenna designed with CPW feed for dual band operation (2.4/5.8GHz) [33].

Moreover, directional antennas such as log-periodic antenna [34]; Yagi antenna [37], [38], [37]; dielectric resonator [38] have been fabricated on chip. It is to be noted that the AoC technology has low radiation efficiency [41] , [42]. However, performance of on-chip antennas

can be increased by using different techniques like air cavity, micromachining, et al. and using substrates like Silicon on Insulator (SoI), SiGe, GaAs; and different process technology like BiCMOS-9MW, layer of Benzo-cyclo-Butene (BCB) polymer, etc. Performance Evaluation of various antennas on chip can be found in publications [39], [40], [41] and [42]. In this work, only monopole zigzag antenna is implemented for WNoC in MCMC systems and 3D IC.

To solve the problem of wired network on chip, wireless network on chip is implemented. One of the main component of WNoC is antenna on chip known as wireless interconnect. The earliest implementation of wireless interconnects (or AoC) for WNoC is implemented in [43] using capacitive and inductive coupling.

Wireless network on chip implemented in [18] using log periodic antennas which are directional antennas. Another implementation of Carbon nanotubes directional antenna for WNoC is shown in [44]. A simulation-based study on Wireless Network on chip performed using zigzag antenna is in [19], which is extended in chapter 3. Fabrication of zigzag antennas are performed in chapter 5.

For WNoC in 3D IC, meander dipole antenna of length 2.4mm are simulated as wireless interconnects [45]. This analysis is performed in X-band (8-12GHz) region. Another simulation study of wireless interconnects using zigzag antennas at 60GHz is shown in [30]. The study uses a setup of multiple-tier 3D IC with micro-fluidic coolant channels for thermal management. In this thesis, work of [30] is extended by using two different antenna orientation and two different coolants. The extended work is shown in chapter 5.

1.8. Major Contributions

Due to increasing demand of high performance computing and IoT, it is required to come up with a new and efficient way of decreasing the delays and power consumptions. So Wireless Network on chip is proposed. One of the main part of it is wireless interconnects. In this work, study of transmission between wireless interconnect is performed. The simulations are performed in ANSYS Electronics suite (HFSS) [31].

a) Planar antennas as wireless interconnect is analyzed on silicon with and without ground plane with respect to distortions in the radiation pattern.
b) Transmission study of wireless interconnect in multichip multicore system using the zigzag antenna as the radiator.
c) Zigzag antennas have been fabricated on silicon for 30GHz at RIT's Semiconductor Microsystems Fabrication Laboratory (SMFL). Using the Cascade probe station and Agilent PNA., the return loss and the transmission between on-chip antennas have been measured.
d) A 3D IC with cooling channels has been analyzed for two different wireless interconnects configurations and two different coolants to study the feasibility of transmission between the silicon active layers.

1.9. Organization of Present Work

The thesis presents work related to wireless interconnect. It does not consist of details on Wireless Network on chip networking algorithms. The thesis is divided into chapters which are briefly introduced below.

- **Analysis of Planar Antenna on Silicon:** This chapter details characteristics of antennas such as linear monopole, zigzag antennas and circular loop antenna in different setups which include silicon with and without perfect electrical boundary (PEC).
- **Wireless Interconnects for MCMC systems:** This chapter collects all different models simulated for zigzag antennas as wireless interconnects in MCMC systems. The positions of wireless interconnects are varied to analyze the transmission coefficients between wireless interconnects.
- **Fabrication of Wireless Interconnects on silicon:** This chapter discusses the design procedure and results of zigzag antennas which are fabricated on silicon wafer at Semiconductor & Microelectronics Fabrication Lab at Rochester Institute of Technology, Rochester, NY.
- **Wireless Interconnects for 3D IC:** This chapter collects HFSS [31] simulation results performed using zigzag antennas in a 3D IC structure. To cope up with the heat generated in 3D IC microchannels are designed. Analysis of antennas with two different configurations and two different coolants is performed. At last, a comparison between transmission coefficients of antennas is provided.

2. Analysis of Planar antennas in various Si environments

To understand the antennas on chip, it is important to simulate single antennas on different arrangement of silicon. The aim of the chapter is to provide results and observations of antennas behavior when placed on a Si wafer. The results provided in the report are current density, return loss and radiation pattern. The radiation pattern of the antenna is plotted. Furthermore, the comparison of radiation pattern for antennas in different environments is performed. This section presents results of simulations performed in following setups:

- In Free space.
- On 5mmx5mm Si wafer without Ground plane.
- On 5mmx5mm Si wafer with Ground plane.

All configuration has one antenna at a time. Three different Al antennas structures such as Linear monopole, Zig-Zag monopole and Circular Loop antennas are simulated with Co-planar waveguide(CPW) feed. The antenna is designed using ANSYS Electronics Desktop(HFSS)[31] to resonant at 60GHz. The CPW feed is fed using a lumped port in simulation software. For simulating a frequency sweep like from 0.25GHz to 80GHz, interpolating sweep is used rather than fast sweep. Fast sweep is used for small frequency interval and less mesh elements. For more details, on frequency sweep please refer to ANSYS Help. As per instructions from ANSYS Help, it is required to place the radiation boundary at least $\lambda/4$ distance from the radiating sources.

Simulation results like current density, return loss, radiation pattern are discussed. We will start with the simplest antennas of three, the Linear monopole antenna, and the simplest environment, free space.

2.1. Antennas in Free space

To design and verify the antenna structures and results, first antennas are designed in free space. This is only a hypothetical setup since the antennas are planar, they require a support substrate to work. Free space setup is simulated only to compare with the results of other configuration.

2.1.1. Linear monopole antenna

A planar linear monopole antenna is designed with large ground to operate at 60GHz. The length of the monopole is $\lambda_0/4$; at 60GHz $\lambda_0/4$=1250µm. It is fed by a Co-planar waveguide (CPW). The CPW is excited by using a lumped port in ANSYS HFSS.

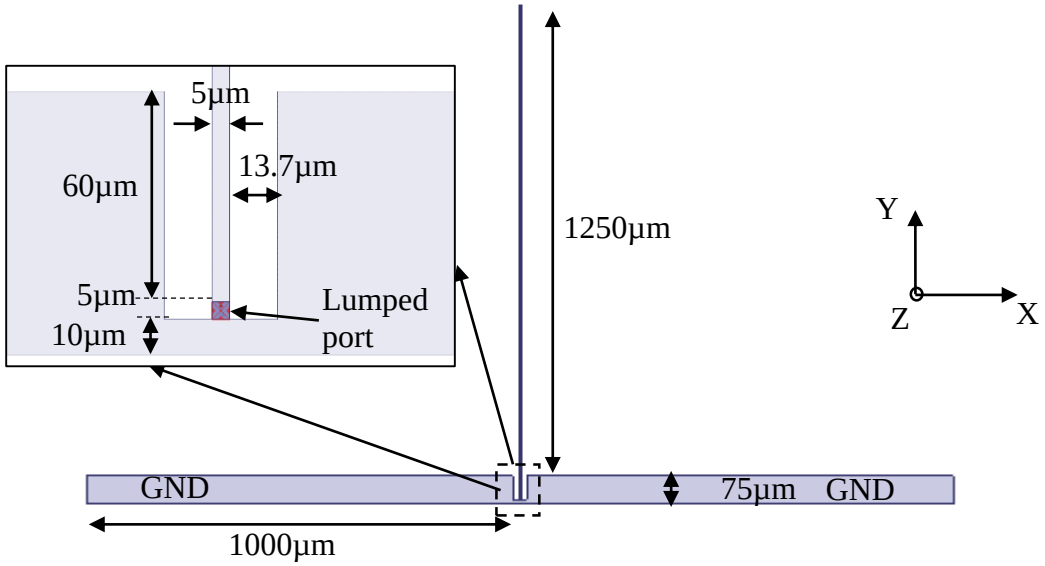


Figure 2-1: Linear monopole antenna.

The return loss is shown in Figure 2-2. It shows that the antenna is resonating with a return loss of -12dB at 60GHz.

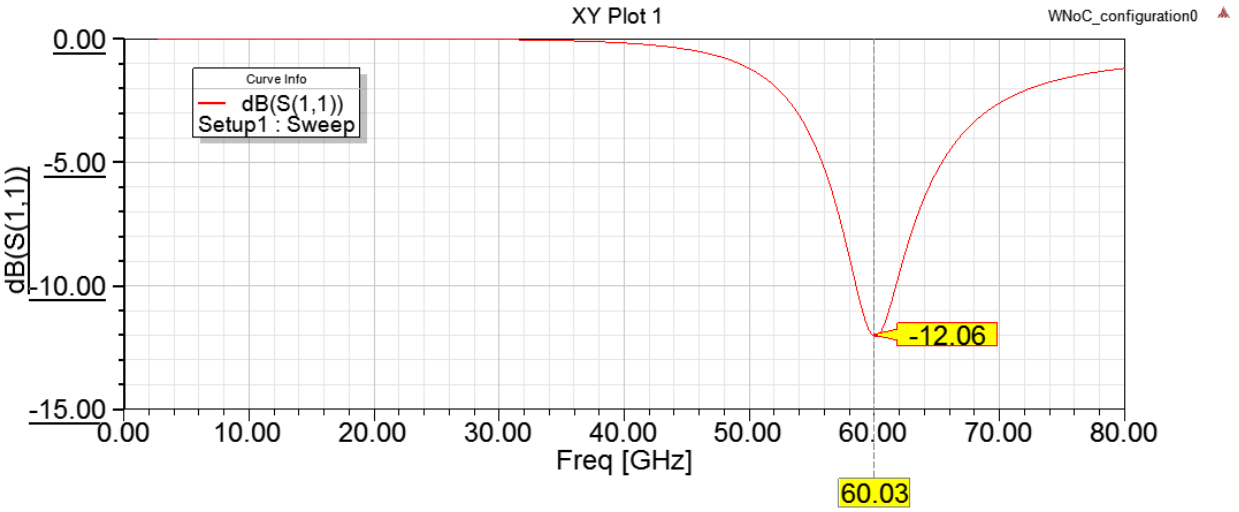


Figure 2-2: Return loss of linear monopole antenna in free space.

Current density in Figure 2-3 is showing that the current is flowing through the monopole, moreover the current distribution is as expected for monopole that is quarter wavelength. Moreover, the radiation pattern is shown in azimuthal plane i.e. the plane of the antenna. The radiation pattern in azimuthal plane is similar to the monopole wire antenna in free space.

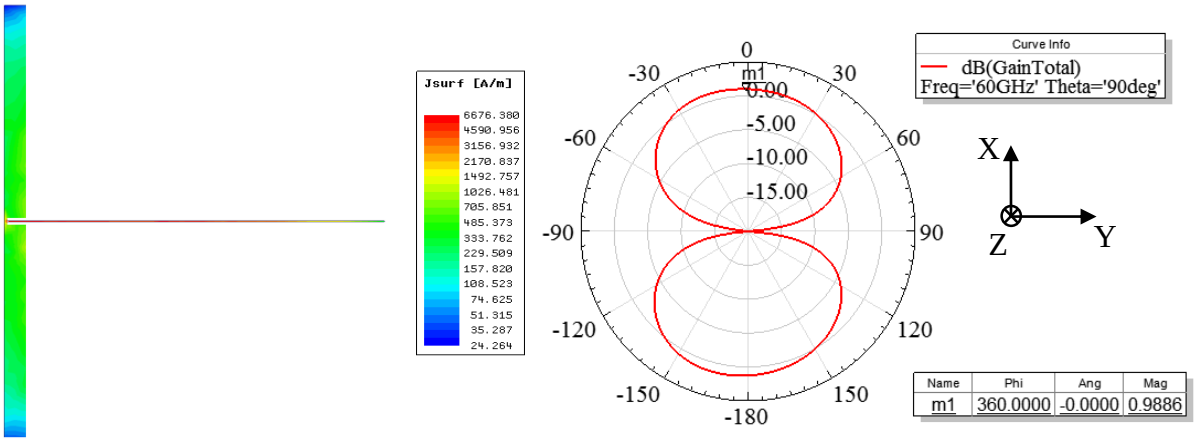


Figure 2-3: Current density and radiation pattern in θ=90° planes (Azimuthal).

Next, radiation pattern in elevation plane is shown in Figure 2-4. It can be seen that the radiation pattern is like donut shape just like a monopole wire antenna. However, the gain is 0.98dBi which is less than a monopole antenna in free space.

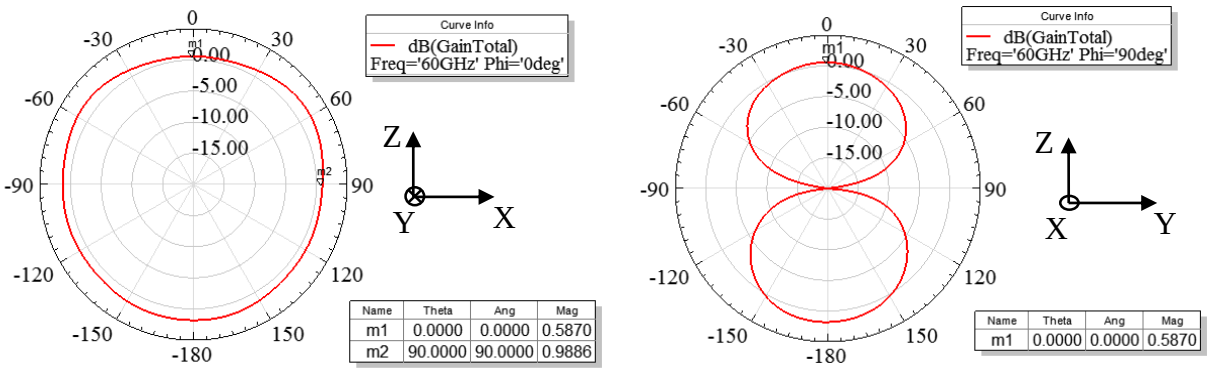


Figure 2-4: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.1.2. Linear Antenna with smaller GND

The required antenna for fabricating on chip should be low-profile, easy to fabricate, therefore the size of ground plane of CPW feed is reduced just like monopole antenna with long sleeves shown in [29]. After reducing the bottom CPW feed's GND of Linear monopole of previous section, the resonant frequency increases a lot. To make the monopole resonant on 60GHz, it is required to increase the length of monopole. The new length of monopole which is resonating at 60GHz is 1680µm.

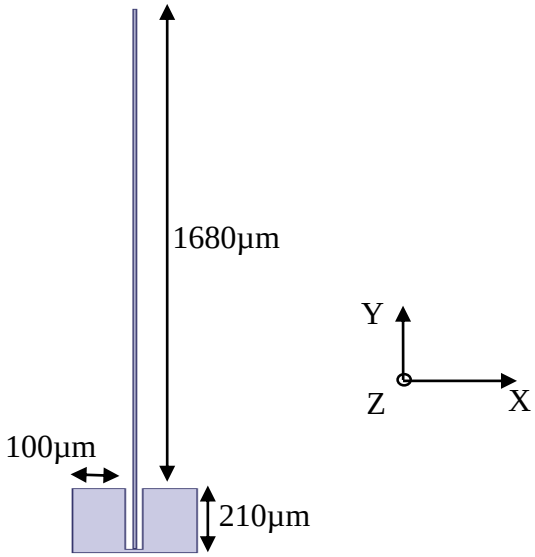


Figure 2-5: Linear monopole with small CPW ground in free space.

Return loss plot is shown in Figure 2-6. It can be seen that at 60GHz the antenna is resonating at 60GHz with a return loss of -11.85dB.

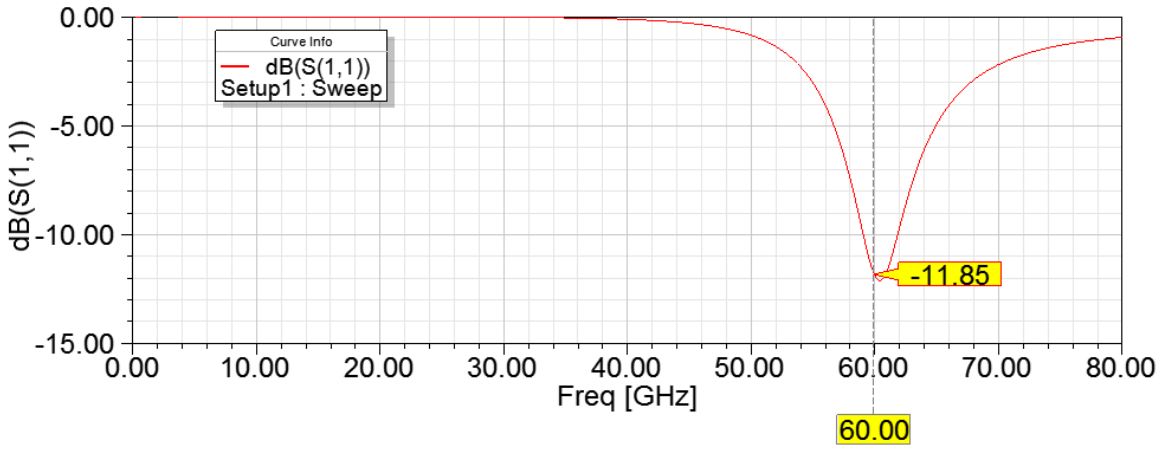


Figure 2-6: Return loss of antenna. At 60GHz, return loss = -11.85dB.

The current density and radiation pattern(azimuthal plane) plot are shown in Figure 2-7. The current distribution of the antenna shows that the antenna is quarter-wave long. The radiation pattern in azimuthal plane shows that the antenna still has overall donut shape with little abnormality.

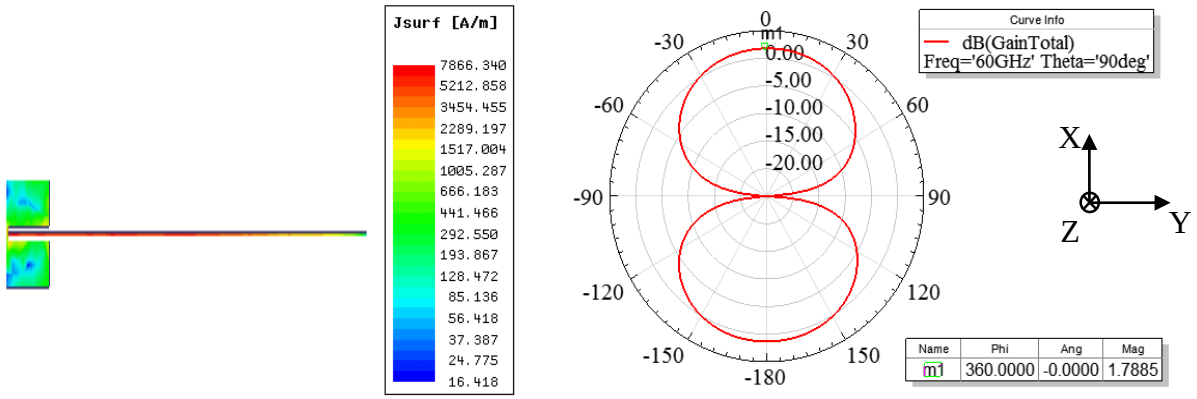


Figure 2-7: Current density and radiation pattern in θ=90° planes (Azimuthal).

The elevation plane radiation pattern is shown in Figure 2-8.

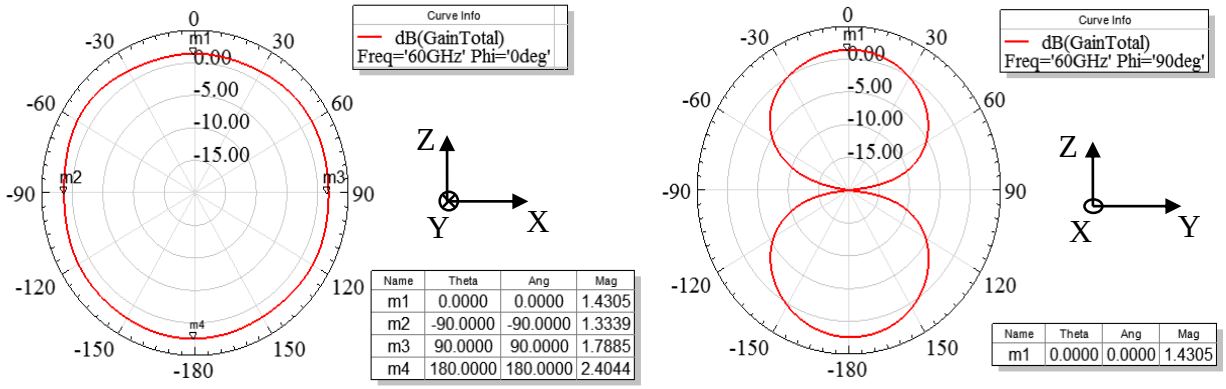


Figure 2-8: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.1.3. Zigzag monopole antenna

To save space in axial direction, low-profile zigzag antenna is designed which acts similar to linear monopole antenna [46]. The calculation of actual length of zigzag antenna is shown. It can be seen that the actual length of zigzag monopole antenna shown below is around $\lambda_0/4$ at 60GHz.

$$L_{actual} = \frac{L_{axial}}{\sin\left(\frac{\theta}{2}\right)} + 50\mu m = \frac{703\mu m}{\sin\left(\frac{30°}{2}\right)} + 50\mu m = 2766\mu m$$

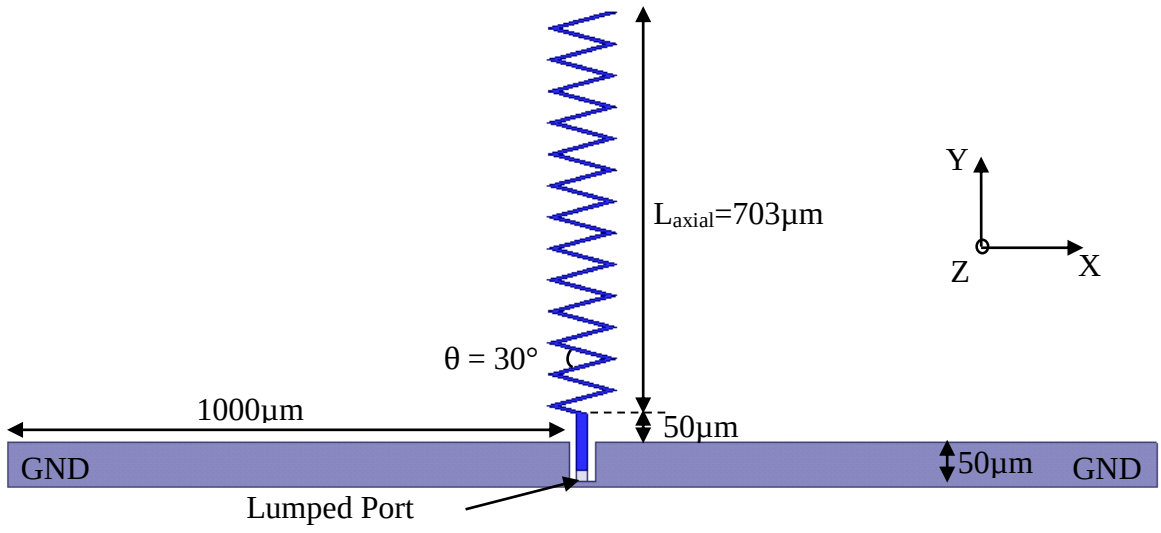


Figure 2-9: Zigzag monopole antenna in free space. Trace width=5μm, Trace thickness=1μm.

The antenna is resonating at 60GHz with a return loss of -10dB.

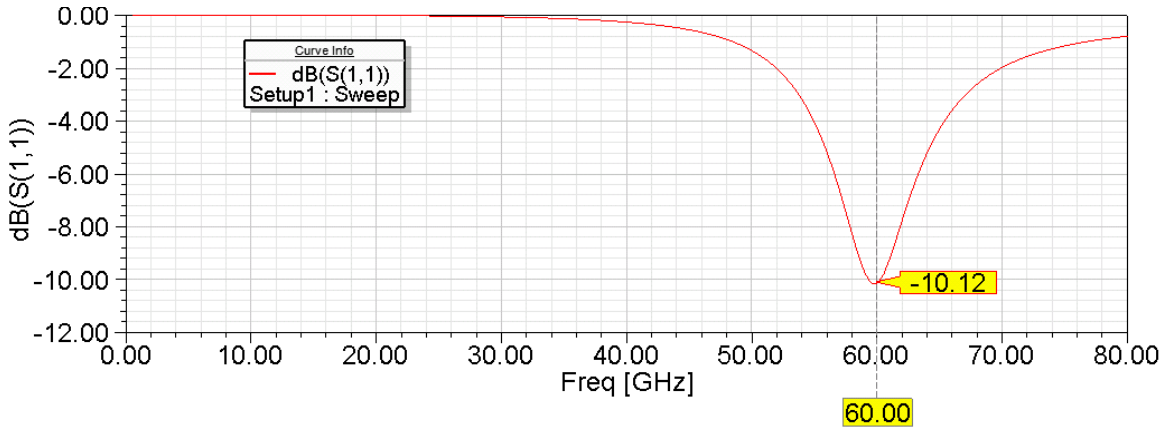


Figure 2-10: Return loss of zigzag monopole antenna.

The current distribution of zigzag monopole antenna is shown in Figure 2-11. It can be seen that the current density at the inner corners of the zigzag elements is very high reaching up to 42000A/m. It should be noted that high current density at the corners can increase ohmic losses, and may add up to heat dissipation or even cause Electromigration in fabricated antenna. The azimuthal plane radiation pattern shows that the shape of radiation pattern is donut shape with decreased gain relative to Linear monopole antenna in previous section.

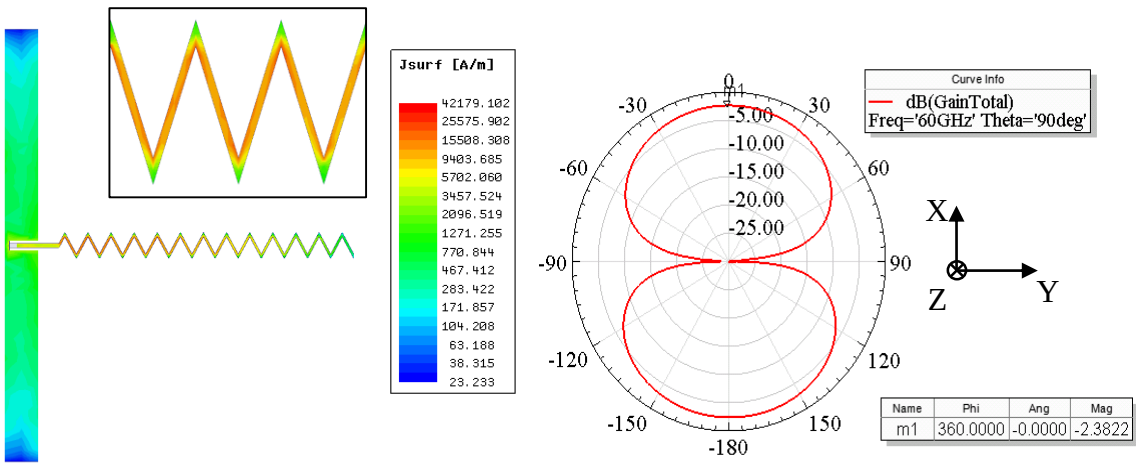


Figure 2-11: Current density and radiation pattern in θ=90° planes (Azimuthal).

The elevation plane radiation pattern is shown below. The pattern is donut shaped with gain -2.34 dBi which is negative relative to isotropic antenna.

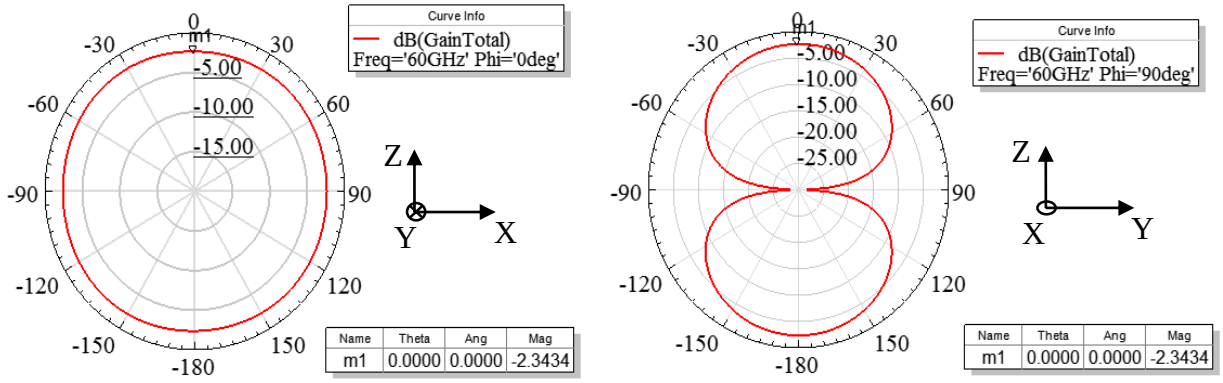


Figure 2-12: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.1.4. Zigzag monopole antenna with smaller GND

The Zigzag antenna with big ground is optimized to smaller ground. Like, linear monopole antenna the length of antenna is increased.

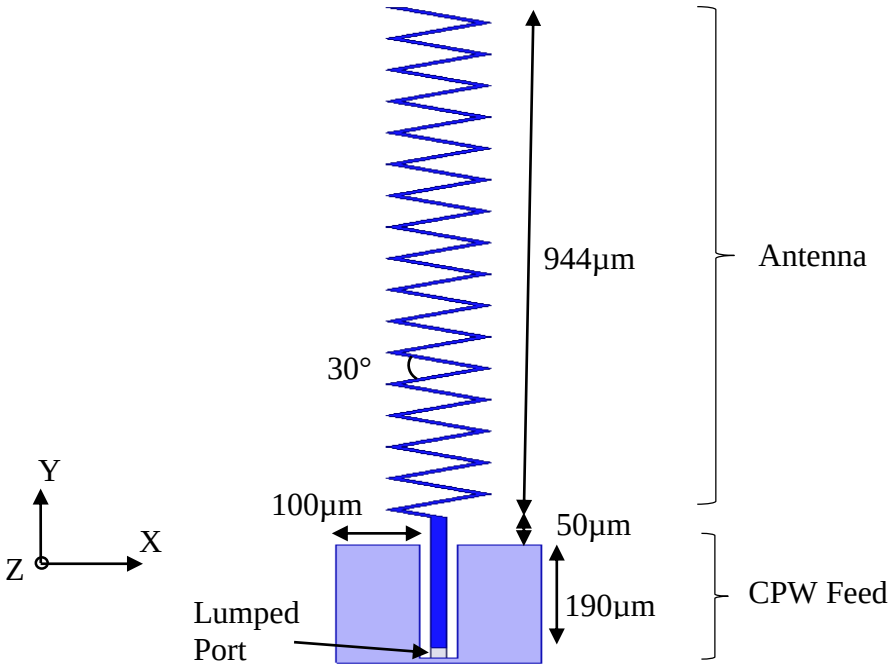


Figure 2-13: zigzag monopole antenna in free space. Trace width=5µm, Trace thickness=1µm.

The antenna is resonating at 60GHz with a return loss of -15.47dB.

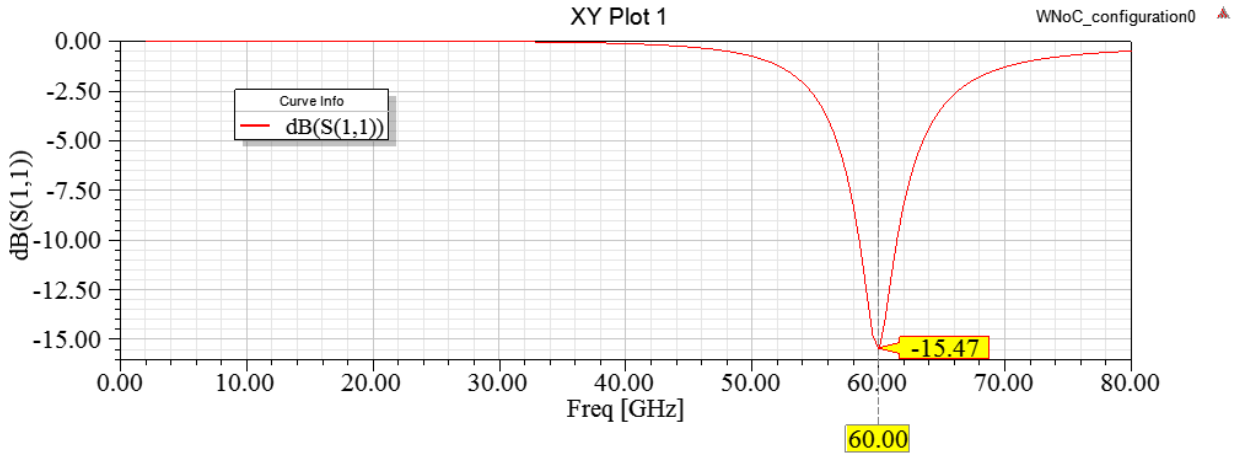


Figure 2-14: Return loss of antenna. At 60GHz, return loss = -15.47dB.

The current distribution is shown in Figure 2-15. The current density is high at the corners of zigzag elements. The azimuthal plane radiation pattern is shown below. The pattern is donut shaped as seen in other antennas with a gain of -1.2dBi

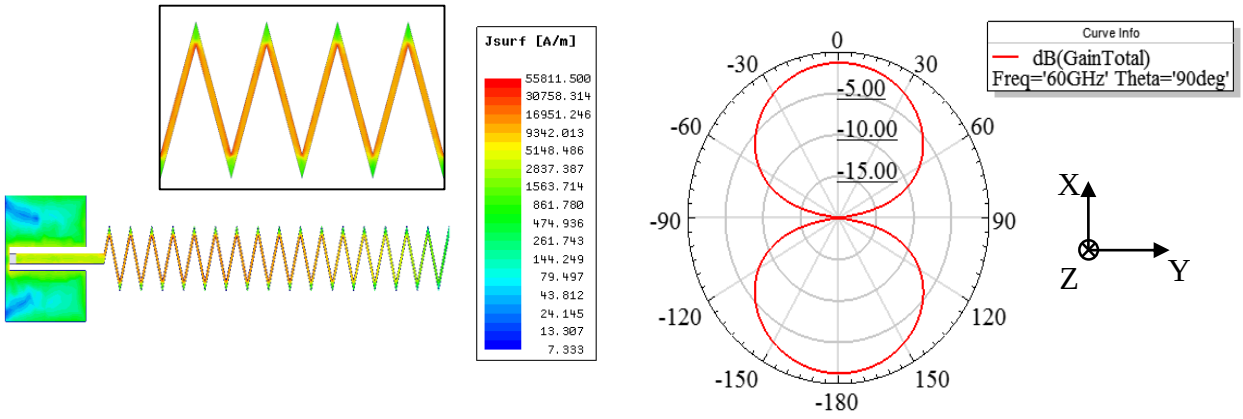


Figure 2-15: Current density and radiation pattern in θ=90° planes(Azimuthal)

The elevation plane radiation pattern is shown in Figure 2-16.

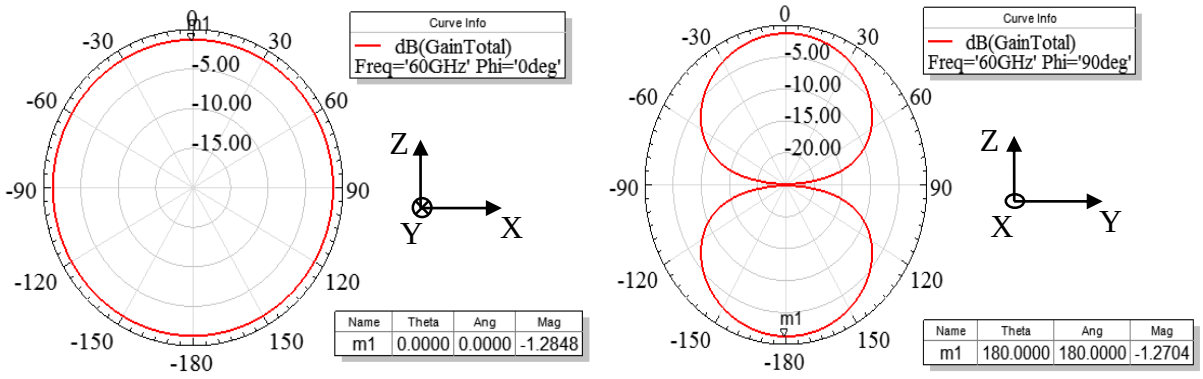


Figure 2-16: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.1.5. Circular loop antenna

A circular loop antenna is designed fed by a CPW feed based on [32] and [33]. Trace width is 5μm. Trace thickness is 1μm. The dimensions is shown below. For simulation in HFSS, the antenna trace is aluminum and GND is PEC material.

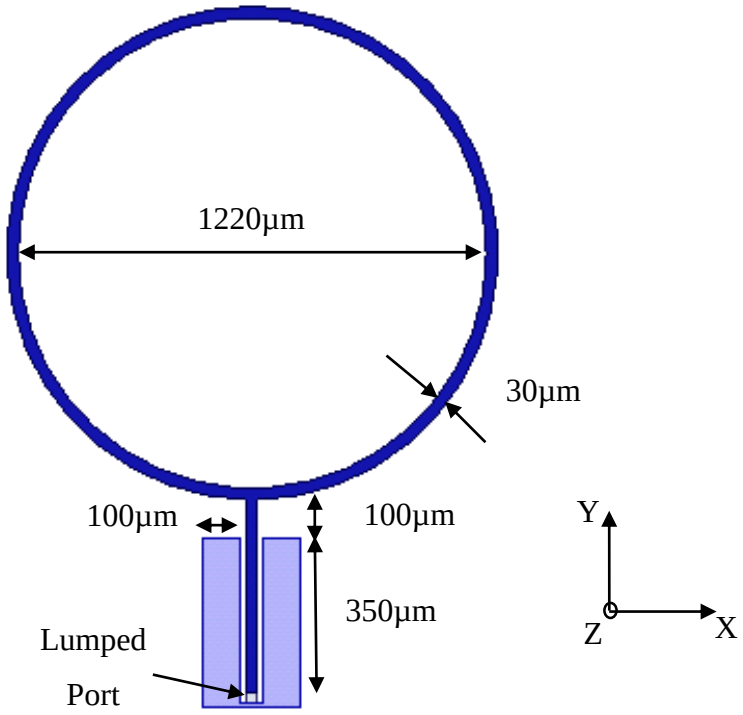


Figure 2-17: Circular loop antenna.

The return loss of the loop antenna is -18.72dB at 60GHz.

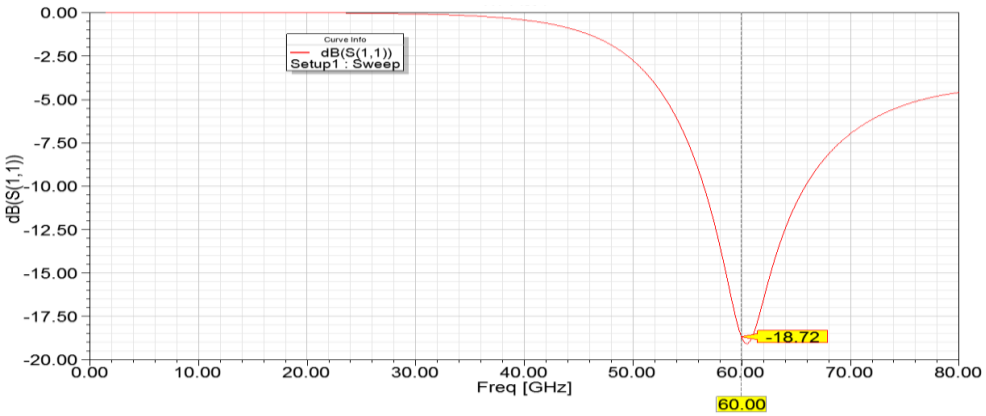


Figure 2-18: Return loss of antenna.

The current distribution of loop antenna is shown below. The maximum current density is approximately same as the linear monopole antenna. Moreover, the current density of antenna is 10 folds smaller than max current density of zigzag antenna. The azimuthal plane radiation pattern is similar to the previous antennas (linear and zigzag antennas). It is donut shaped with directive gain =0.93dBi in azimuthal plane.

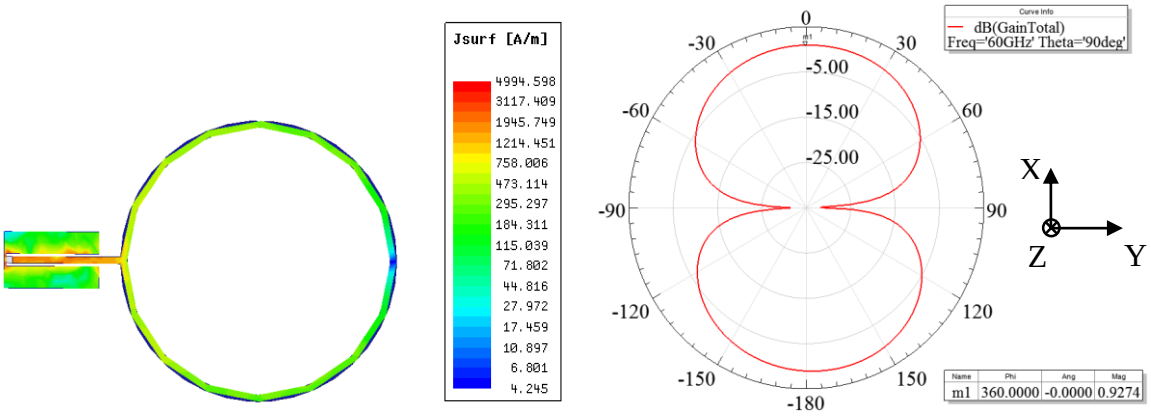


Figure 2-19: Current density and radiation pattern in θ=90° planes (Azimuthal).

The radiation pattern in elevation plane is shown in Figure 2-20. The radiation pattern in elevation plane has a directive gain of 2.47dBi, which shows that the antenna is radiating more towards Z-axis.

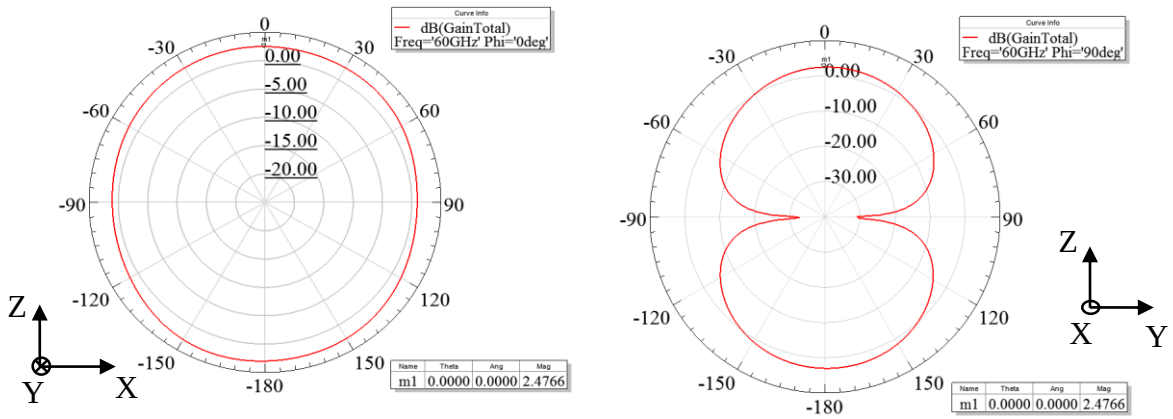


Figure 2-20: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.2. On 5mmx5mm Si wafer without Ground plane at the bottom

The setup (in text, referred as IC or chip) is shown in Figure 2-21. The silicon wafer thickness is taken as 663 µm, which is commonly used in semiconductor industry. The Silicon has dielectric constant ε_r = 11.7 and high resistivity (ρ = 1000Ω-cm). A silicon dioxide(ε_r = 3.4) layer of thickness 2µm is modelled on top of silicon wafer. A packaging layer with dielectric constat ε_r = 2.9 is covering silicon wafer with a thickness of 1mm. The setup has no PEC boundary at the bottom. Antenna is placed in the middle of silicon dioxide. The size of silicon wafer is 5mmx5mm.

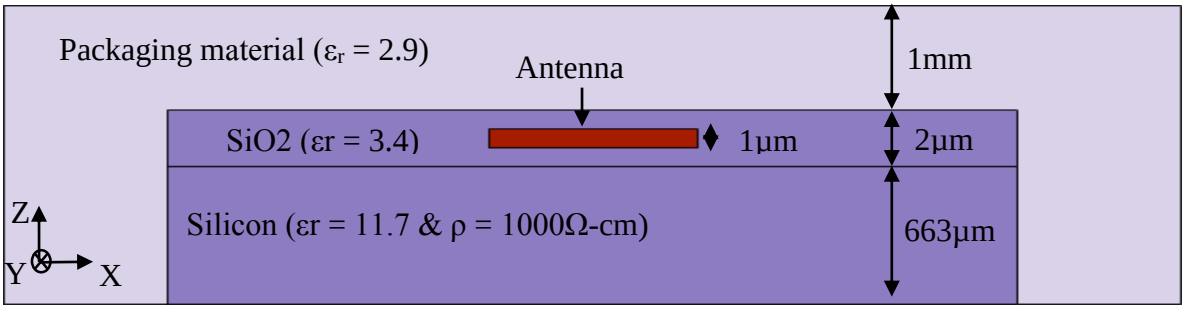


Figure 2-21: Cross section view of setup (Not to scale).

2.2.1. Linear Monopole Antenna

The monopole antenna is designed on Si chip inside the silica layer. It can be seen that the length of monopole antenna is reduced to nearly three times when compared to length of linear

monopole antenna simulated in free space in section 2.1.2. It is because of the change in wavelength at 60 GHz due to environment/material. It is complicated to find the effective dielectric constant because of various material like packaging material, silicon dioxide and packaging material. The simulation results of reduced length antenna on silicon show that the antenna is resonating at 60 GHz. Therefore, it is to be noted that silicon significantly influences on-chip antenna properties.

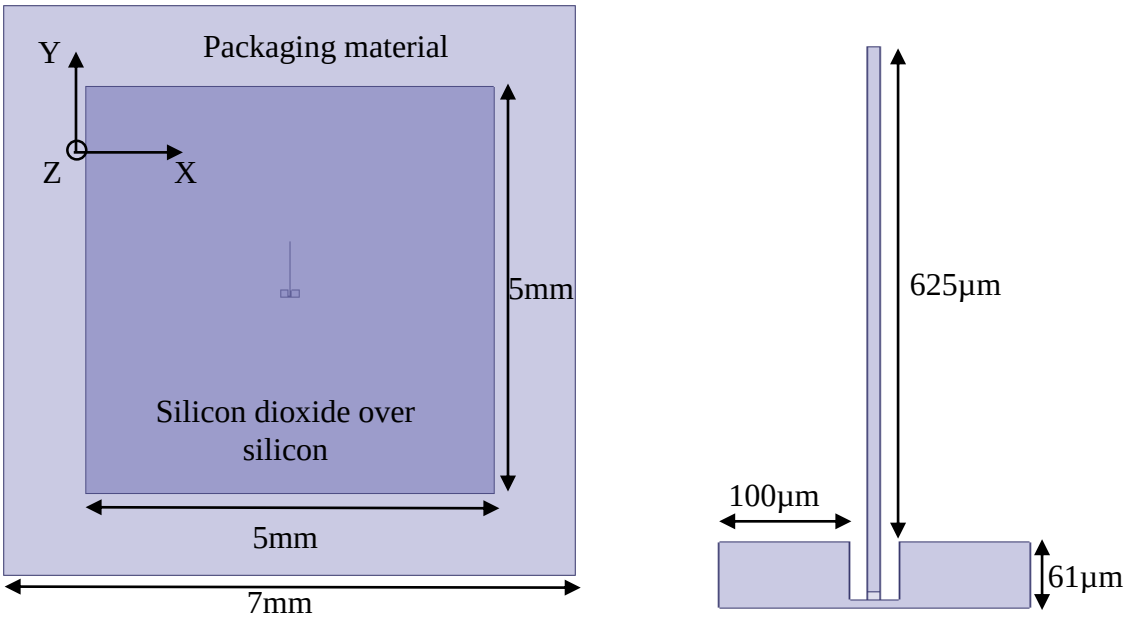


Figure 2-22: Linear monopole in silicon dioxide over silicon.

Simulation is performed in ANSYS HFSS [31]. It has been found that the antenna is resonating at 60GHz with a return loss -9.71dB.

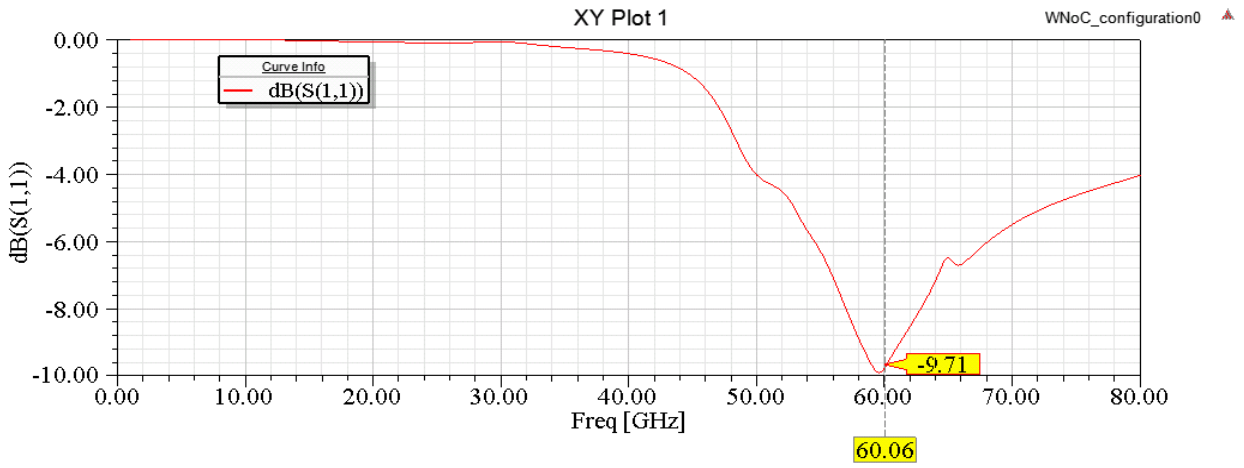


Figure 2-23: Return loss of linear monopole antenna.

The magnitude of current density of antenna is shown in Figure 2-24. The azimuthal radiation pattern can be seen below. It is noted that the radiation pattern is changed compared to previous pattern in free space shown in Figure 2-7 due to silicon high dielectric constant. It has become more omnidirectional in nature.

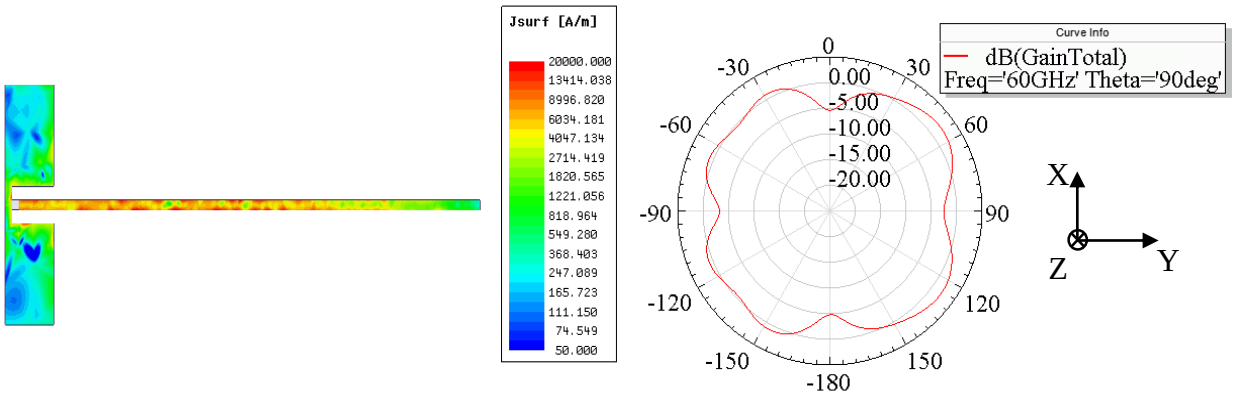


Figure 2-24: Current density and radiation pattern in θ=90° planes (Azimuthal).

The elevation plane radiation pattern is shown in Figure 2-25. The antenna seemed to radiate into the silicon and at certain direction like ϕ=90°& θ=60° (directive gain=-1dBi); ϕ=0°& θ=±60° (directive gain=-2.5dBi).

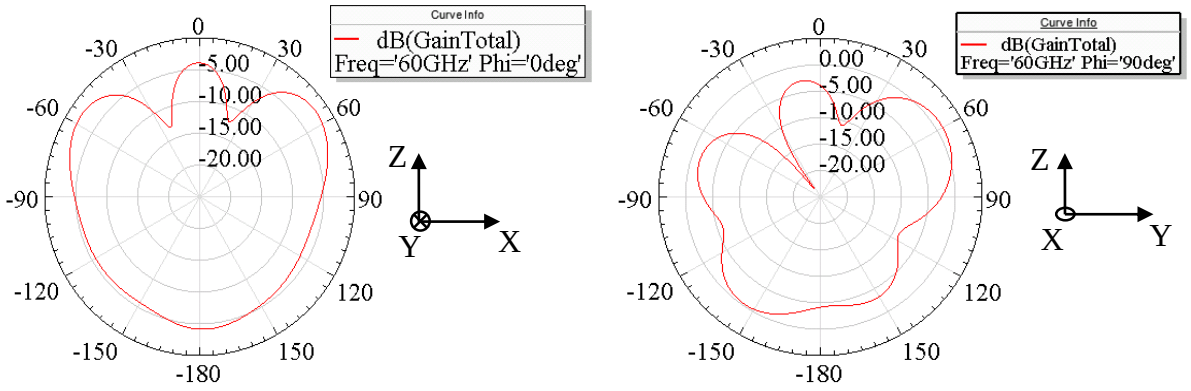


Figure 2-25: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.2.2. Zigzag antenna

Zigzag antenna is designed for silicon chip with a setup shown in Figure 2-21. The design of zigzag antenna is shown in figure below. The CPW-fed zigzag antenna is placed at the center of silicon wafer in the silicon dioxide layer. Like linear monopole antenna, length of zigzag antenna is reduced to significantly.

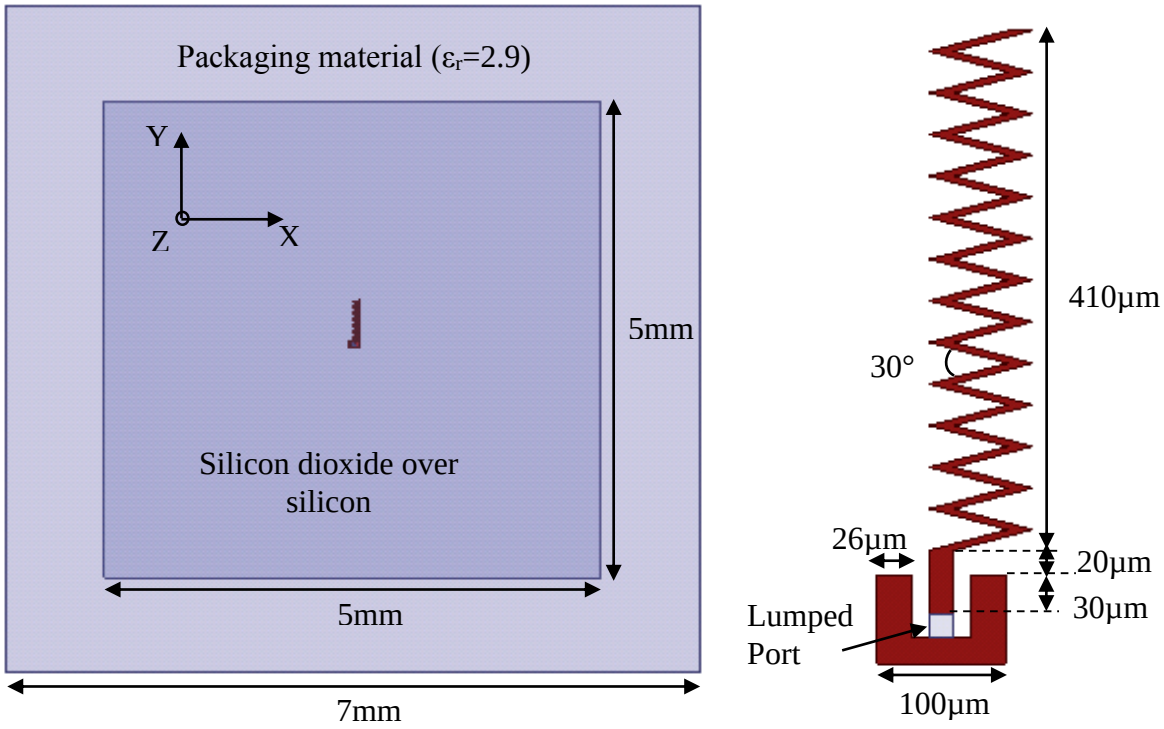


Figure 2-26: Linear monopole in silicon dioxide over silicon.

The zigzag antenna is resonating at 60GHz with a return loss of -25dB.

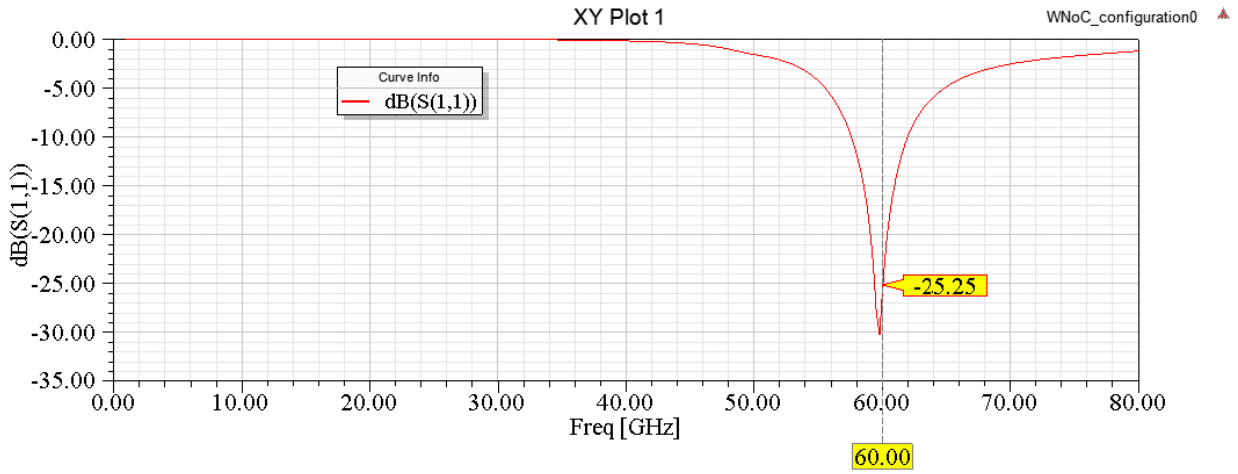


Figure 2-27: Return loss of zigzag antenna.

The current density and azimuthal radiation pattern is shown below. The maximum current density of zigzag antenna at the corners is high compared to linear monopole antenna in same setup which is discussed in previous section. It can be seen that the azimuthal radiation pattern has become nearly omnidirectional.

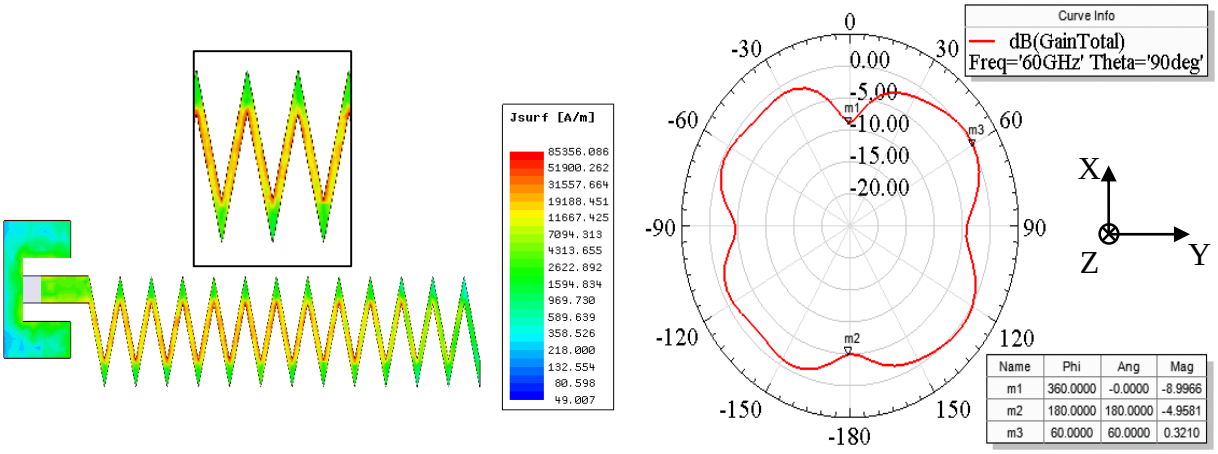
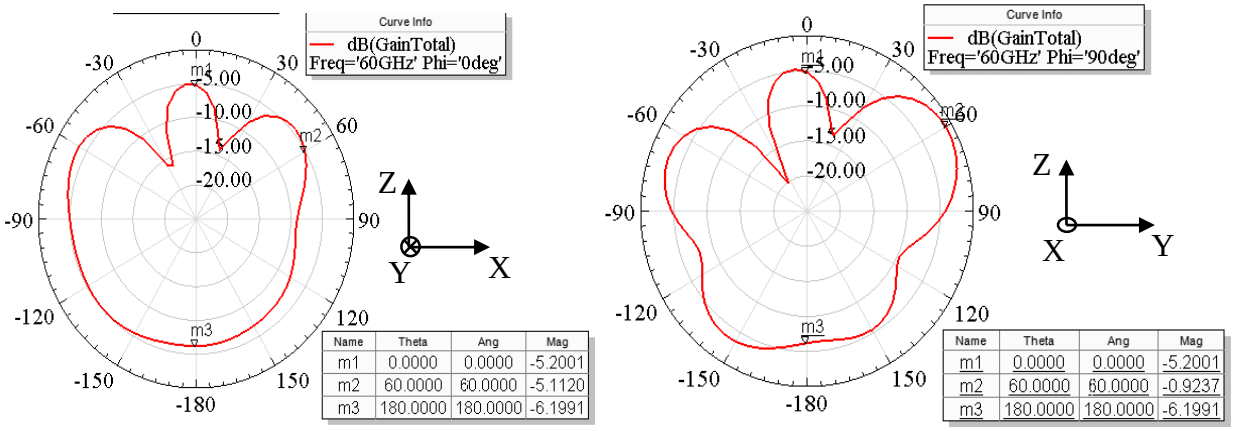


Figure 2-28: Current density and radiation pattern in θ=90° planes (Azimuthal).

Elevation plane radiation pattern is shown in Figure 2-29. Like linear monopole antenna discussed in section 2.2.1, it can be seen that the zigzag antenna is radiating more into the silicon, and at certain angles similar to linear antenna.



Name	Theta	Ang	Mag
m1	0.0000	0.0000	-5.2001
m2	60.0000	60.0000	-5.1120
m3	180.0000	180.0000	-6.1991

Name	Theta	Ang	Mag
m1	0.0000	0.0000	-5.2001
m2	60.0000	60.0000	-0.9237
m3	180.0000	180.0000	-6.1991

Figure 2-29: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.2.3. Circular loop antenna

Circular loop antenna analyzed in section 2.1.5 is optimized for silicon chip shown below.

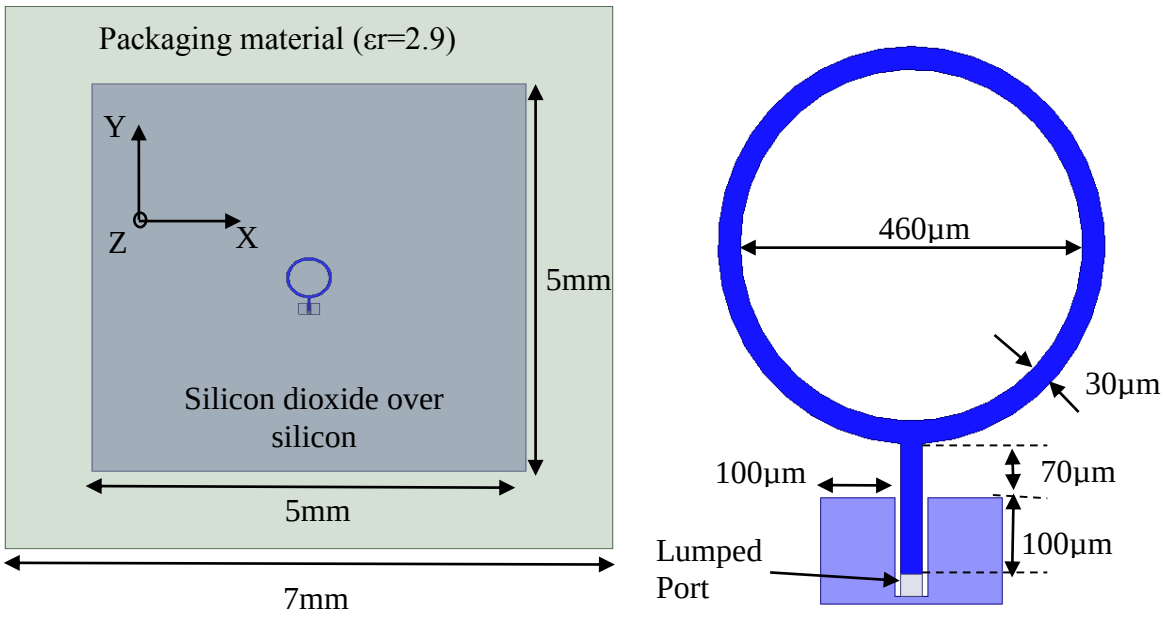


Figure 2-30: Circular loop antenna in silicon chip without ground.

The CPW feed gap is 7µm. The simulation is performed with the antenna placed at the center of the setup shown in .Figure 2-21. The antenna is resonating at 60GHz with a return loss of -23.79dB.

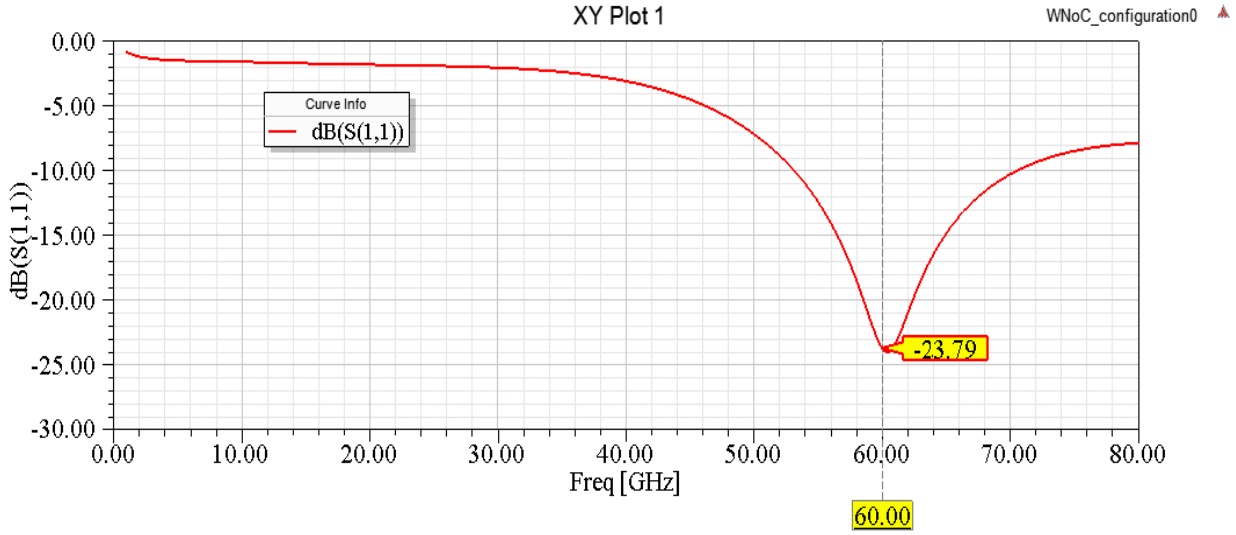


Figure 2-31: Return loss of circular loop antenna.

The current density of circular loop antenna is shown below. Moreover, azimuthal radiation pattern is shown. It should be noted that, like previous antennas, the radiation pattern of this antenna in azimuthal plane is nearly omnidirectional.

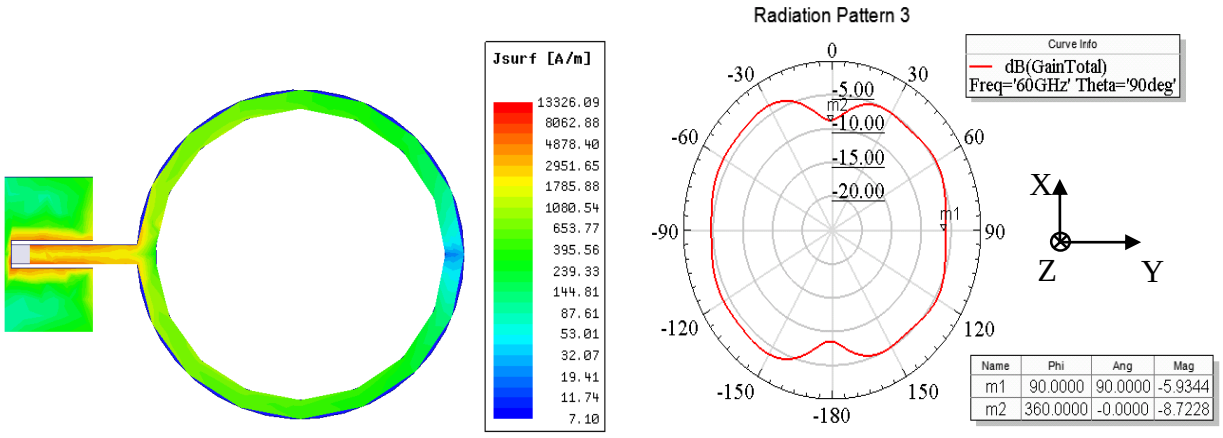


Figure 2-32: Current density and radiation pattern in θ=90° planes (Azimuthal).

The radiation pattern in elevation plane is shown below. Similar to previous antennas, the radiation of loop antenna is going into the silicon wafer.

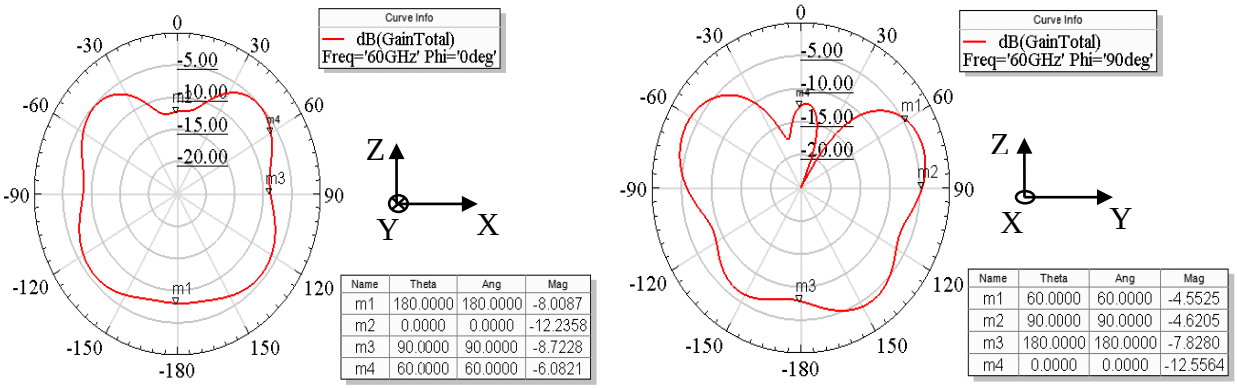
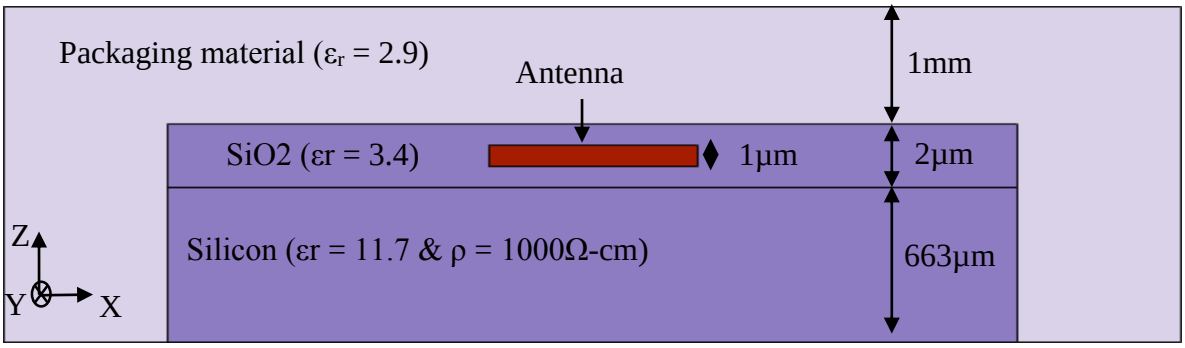


Figure 2-33: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.3. On 5mmx5mm Si wafer with Ground plane at the bottom

The silicon chip setup used in this section is same as the last section (shown in Figure 2-21), only change is the introduction of ground plane at the bottom of setup. The ground plane is used to see the effects of heat sink. No dimensions of layers are altered. The antenna is considered in between the silicon dioxide layer. It should be noted that *this section shows how the PEC layer at the bottom affects the antenna properties when compared with section 2.2.*



Ground at the bottom (PEC boundary)

Figure 2-34: Cross section view of setup (Not to scale).

2.3.1. Linear Antenna

The monopole antenna is now designed on Si wafer inside the silica layer. The size of the IC is 5mm x 5mm. The bottom of IC is considered as ground plane.

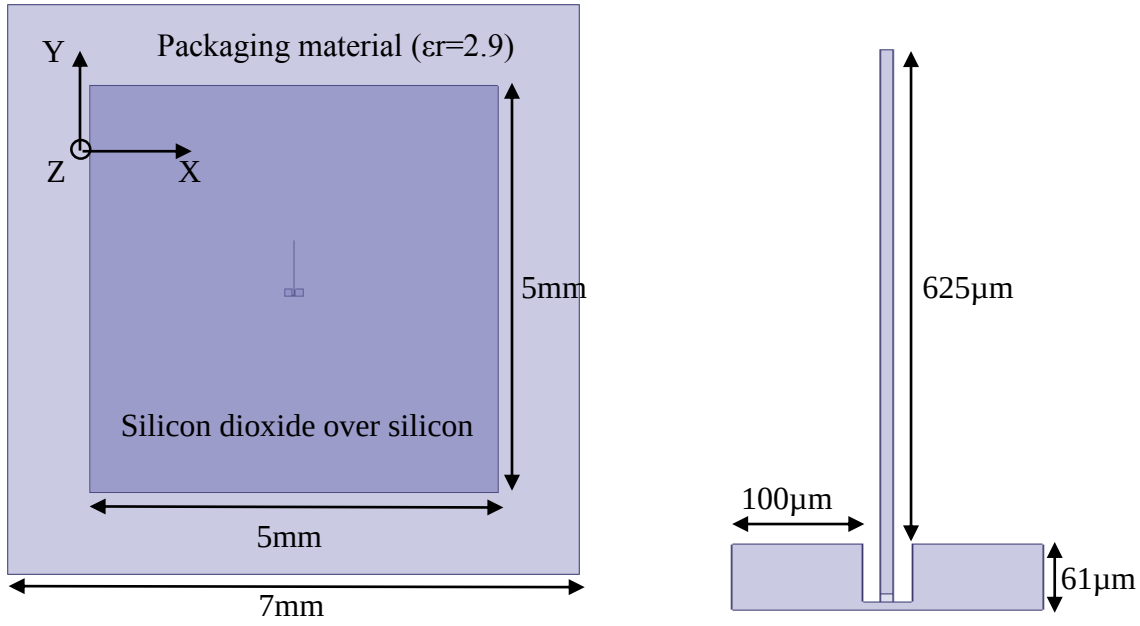


Figure 2-35: Linear monopole in silicon dioxide over silicon.

The antenna is resonating with a return loss of -20dB at 60GHz. However, the resonance is changed due to the presence of ground plane at the bottom of chip.

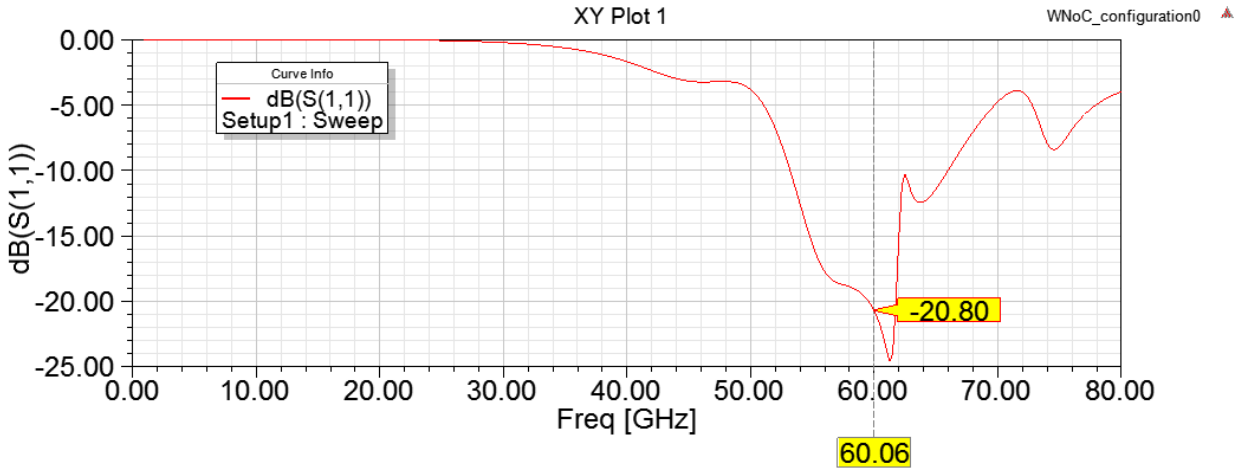


Figure 2-36: Return loss of antenna.

The current density and azimuthal radiation pattern of the antenna is shown below. The radiation pattern has changed from omnidirectional to a directional antenna. The antenna is radiating less towards its axis than towards its side.

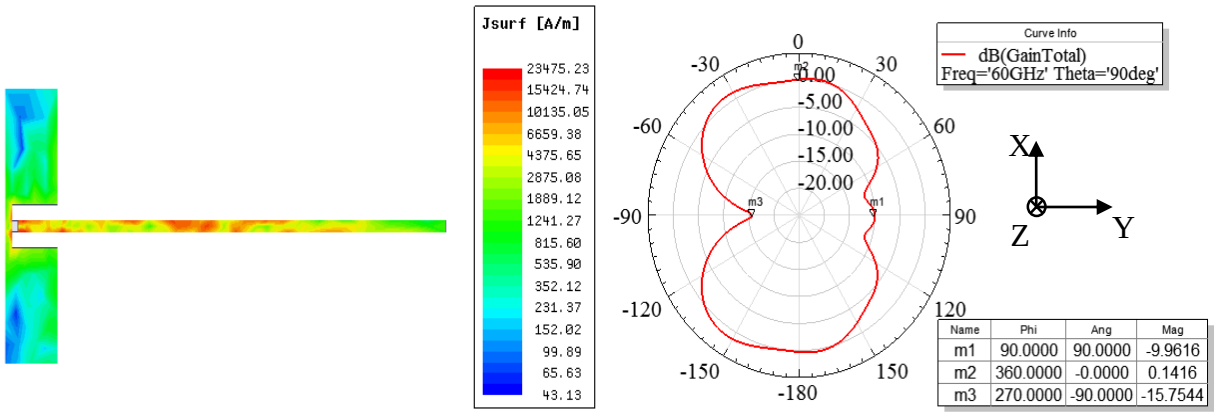


Figure 2-37: Current density and radiation pattern in θ=90° planes (Azimuthal).

Elevation plane radiation pattern is shown below. It can be seen that due to PEC boundary at the bottom of the chip, the most of the radiation of antenna is reflected towards positive z-direction.

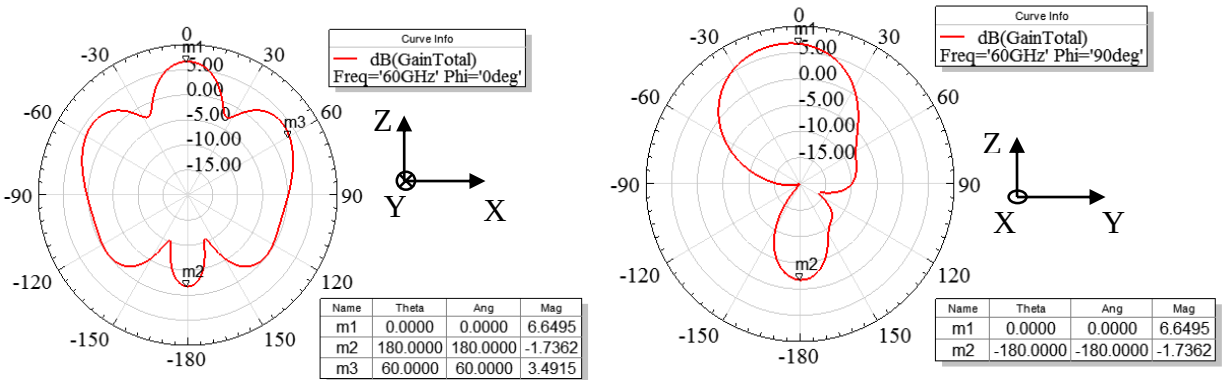


Figure 2-38: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

2.3.2. Zigzag antenna

Now, zigzag antenna is placed on top of a silicon chip with a cross section view shown in Figure 2-34. The zigzag antenna is placed at the center of the chip. The top view of setup is shown in Figure 2-39 along with the antenna dimensions.

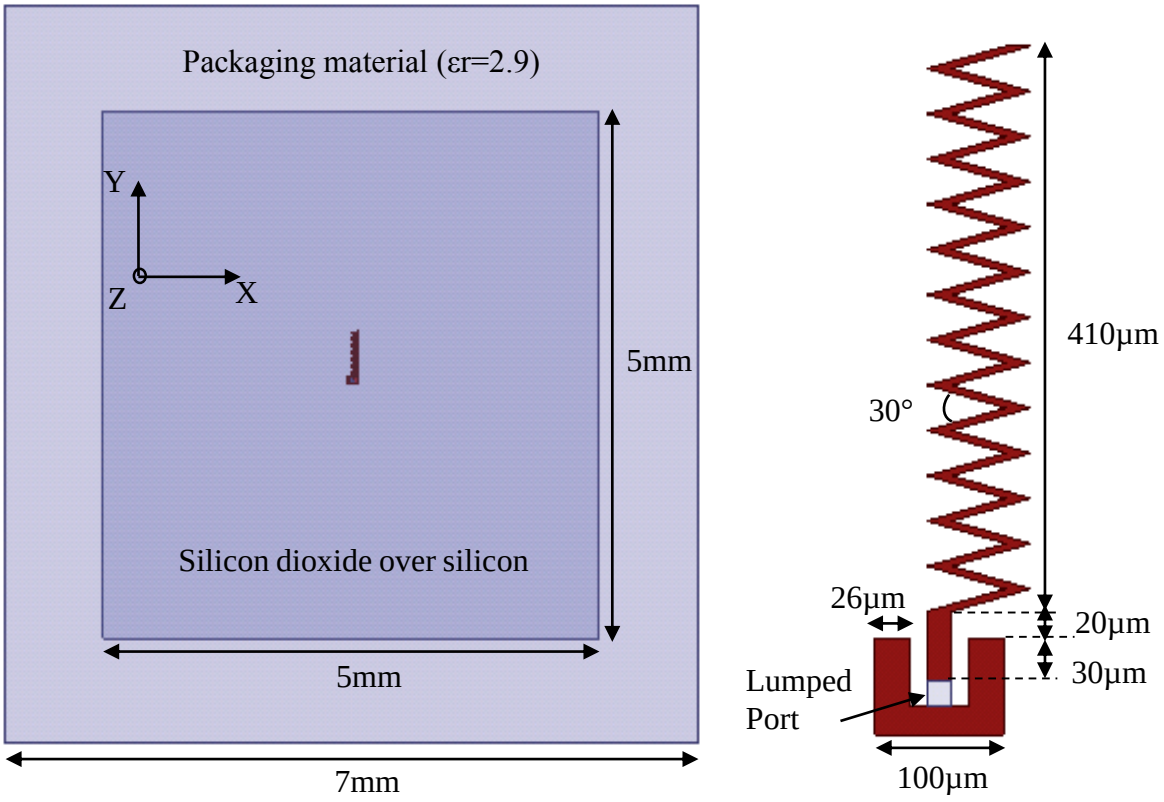


Figure 2-39: Zigzag monopole antenna in silicon dioxide over silicon.

Due to the introduction of PEC plane at the bottom, the resonance is shifted to frequency greater than 60GHz, though at 60GHz, the return loss (in) is -11dB which is good. The results are shown below. It can be optimized by increasing the length of CPW feed.

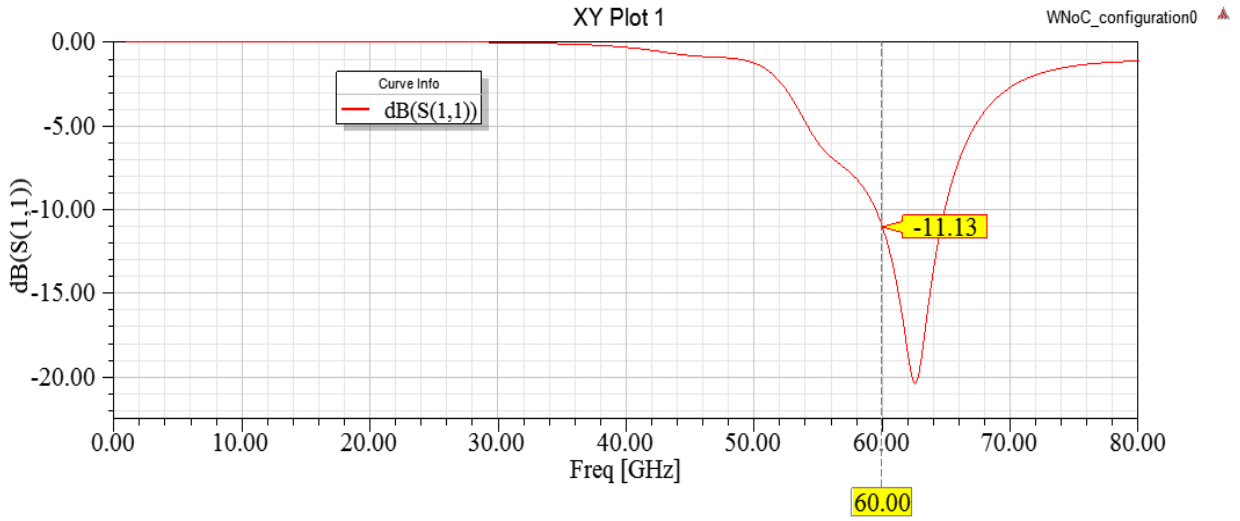


Figure 2-40: Return loss of zigzag monopole antenna in silicon dioxide over silicon

The current density and azimuthal radiation pattern is plotted below. Due to PEC boundary, it can be seen that the ground plane converts the omnidirectional pattern of zigzag antenna into directional pattern.

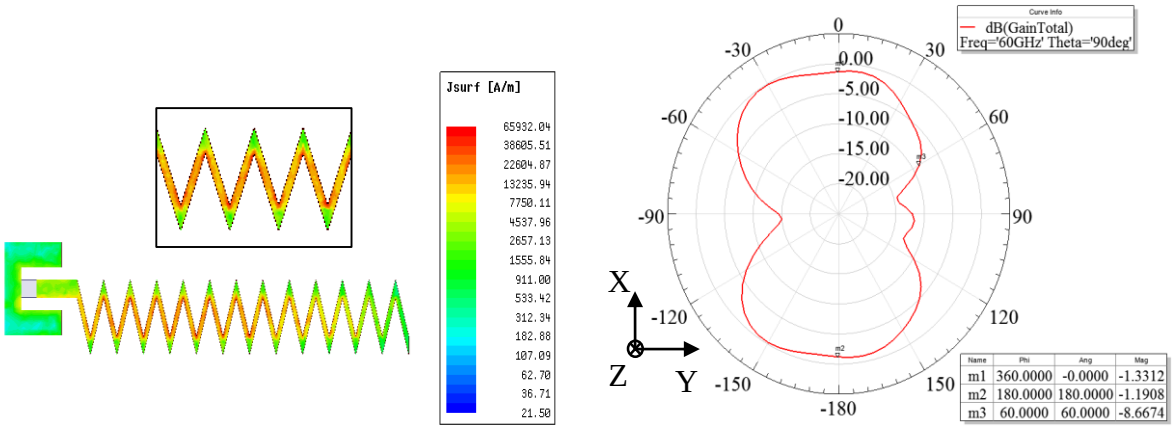


Figure 2-41: Current density and azimuthal radiation pattern of zigzag antenna.

Elevation plane radiation pattern is shown in Figure 2-42. The radiation is reflected towards positive z-direction.

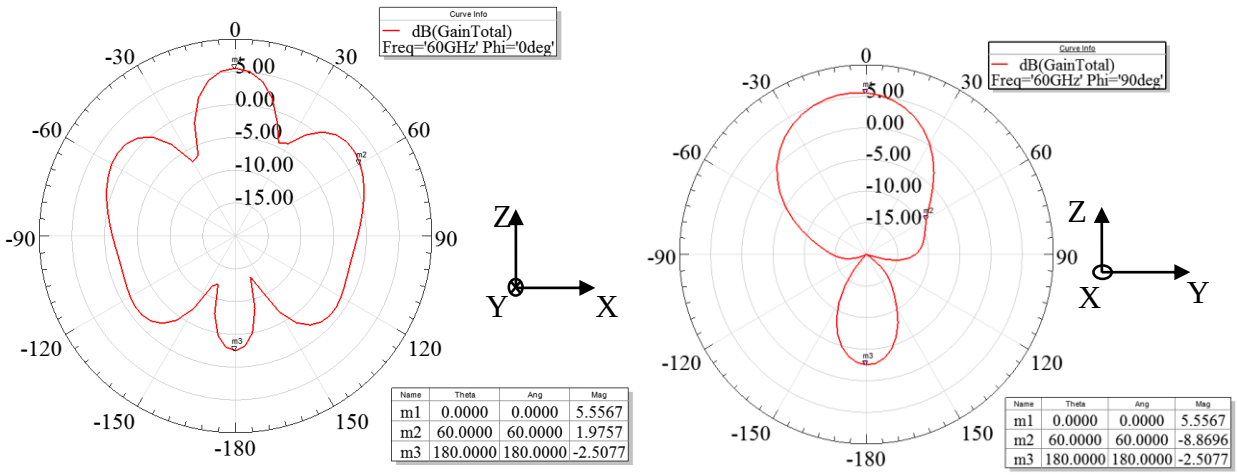


Figure 2-42: Elevation plane radiation pattern of zigzag antenna.

2.3.3. Circular loop antenna

Circular loop antenna is simulated on setup shown in Figure 2-34. Circular loop antenna has same design as simulated in previous section 2.2.3. The effect of ground plane at the bottom is analyzed.

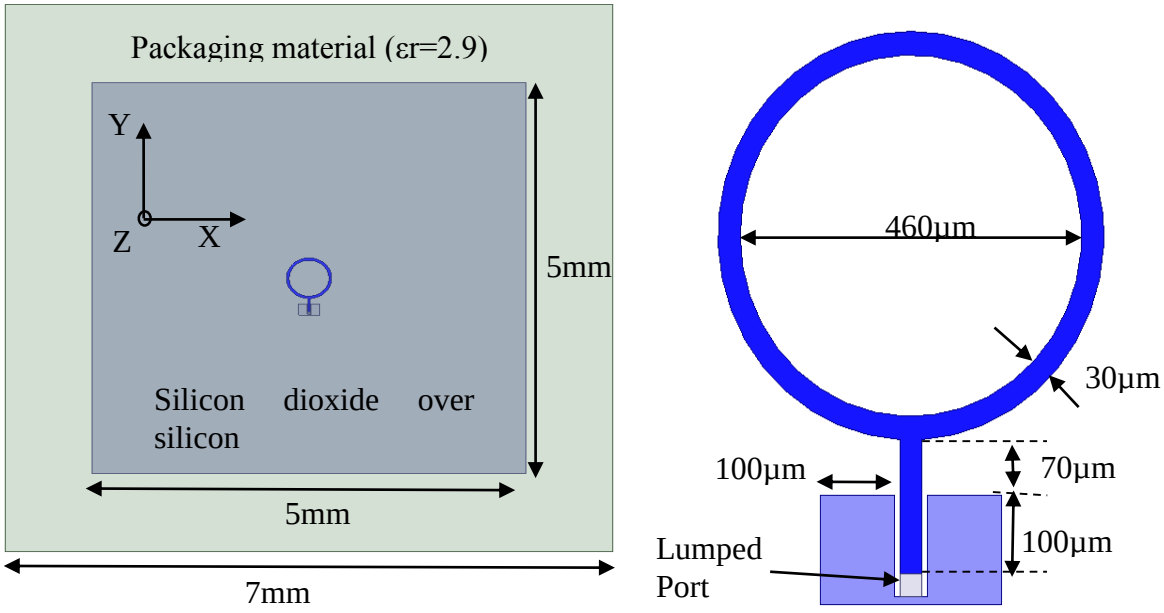


Figure 2-43: Loop antenna in silicon dioxide over silicon.

Due to the introduction of loop antenna, the return loss is shifted from 60GHz to 70GHz. Now, at 60GHz the return loss is -10.6dB.

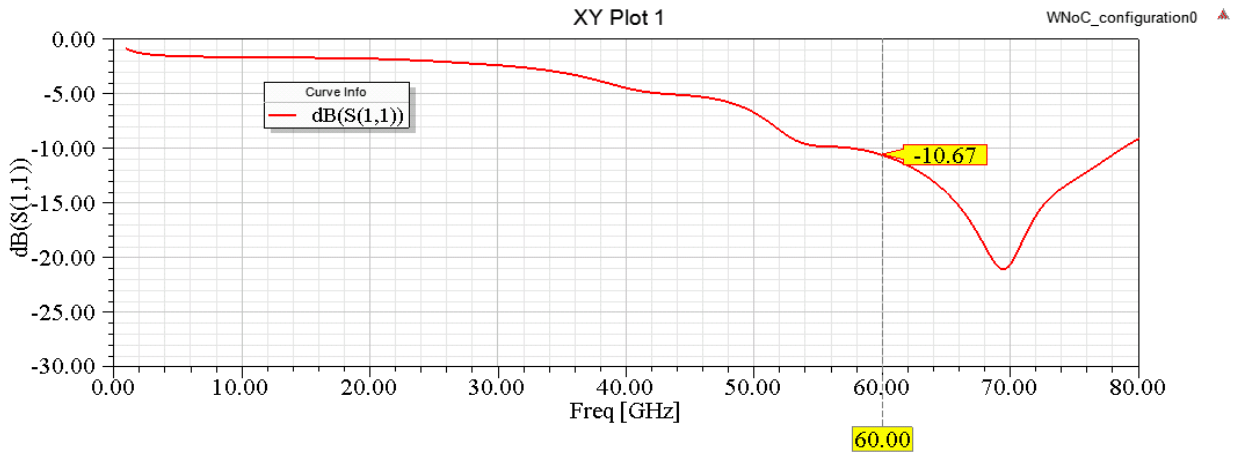


Figure 2-44: Return loss of antenna.

The current density and azimuthal plane radiation pattern is shown in Figure 2-45. The radiation pattern is changed to directional due to the ground plane at the bottom.

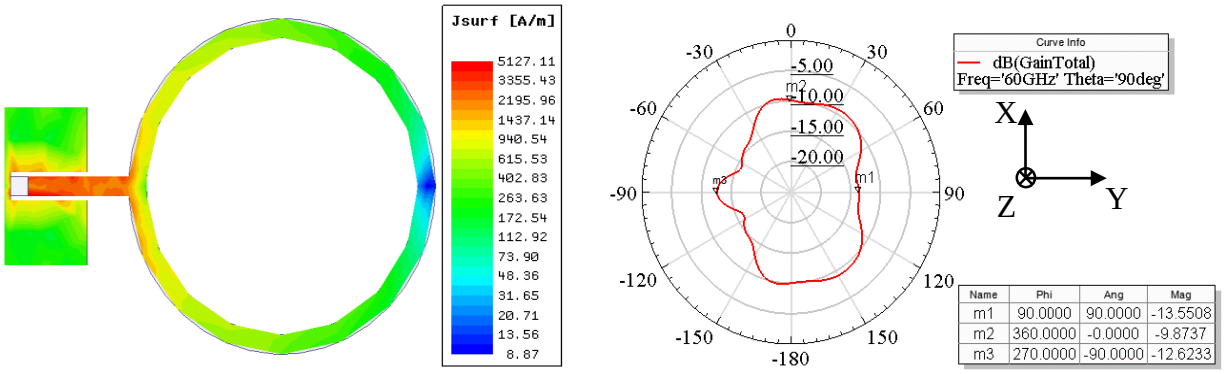


Figure 2-45: Current density and radiation pattern in θ=90° planes (Azimuthal).

The elevation plane radiation pattern is plotted in Figure 2-46. It is noted that the radiation of the antenna is reflected towards positive z-axis.

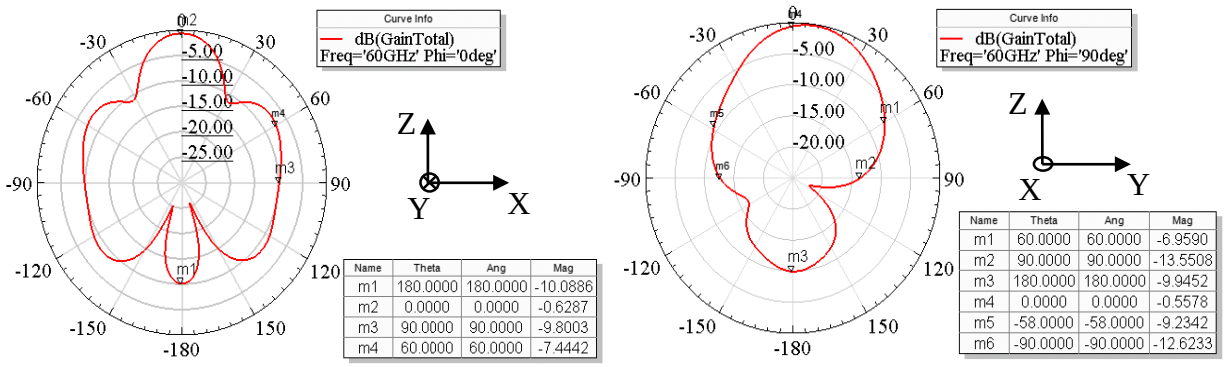


Figure 2-46: Radiation pattern in ϕ=0° and ϕ=90° planes (Elevation).

Zigzag antenna has high current density on the corners. It is nearly 10 times the current density when compared to linear monopole and loop antenna. The length of antenna on silicon chip reduced by 2-3 times when compared to the free space. It should be noted that the radiation pattern influence due to the size of silicon wafer.

It has been seen that the silicon changes the radiation pattern significantly. This has happened because of high permittivity of silicon. PEC boundary is also introduced as a metal surface of heat sink. The PEC boundary or ground plane reflects the radiation, also changes the phase of the radiation by 180°. Ground plane so near to radiating element changes the input impedance, so the resonance, and even the radiation pattern from omnidirectional in free space to directional in setup with PEC boundary. Moreover, PEC boundary so near to a radiating elements makes antenna design difficult.

3. Wireless Interconnects for Multichip-Multicore systems

Multichip multicores (MCMC) systems are used for high performance computing facility. MCMC systems have multicores distributed over a single chip and multiple chips are distributed on an interposer (substrate). Interposer is a substrate on which multiple chips are connected with each other using a network of metal interconnect. Interposer can be a bulk silicon, FR4 or other substrates. MCMC systems today employs Network on Chip (NoC) [15] using metal interconnects which limits the performance of the systems in that they consume nearly large amount of power transferring data [2]. Moreover, metal interconnects take more space than the computing devices, also special repeaters are required to keep the signal flowing in multi-hop networks [2]. Long interconnect also generate delays in signals. In this chapter, wireless interconnects/antennas, terms used interchangeably in chapter, are analyzed for MCMC system.

Four high resistivity silicon die ($\varepsilon r = 11.7$ & $\rho = 1000\Omega$-cm) of size 20mm x20mm is placed 10mm apart on top of FR4 ($\varepsilon r = 4.4$) interposer. All Silicon die has a thickness of 663µm. All four silicon die is further divided into four processing cores. SiO_2 of thickness 2µm is put on top of silicon die. The Si and oxide are covered with a packaging material ($\varepsilon r = 2.9$) of thickness 1mm as shown in Figure 3-1. The antennas are placed in between the SiO_2. The metal thickness is 1µm.

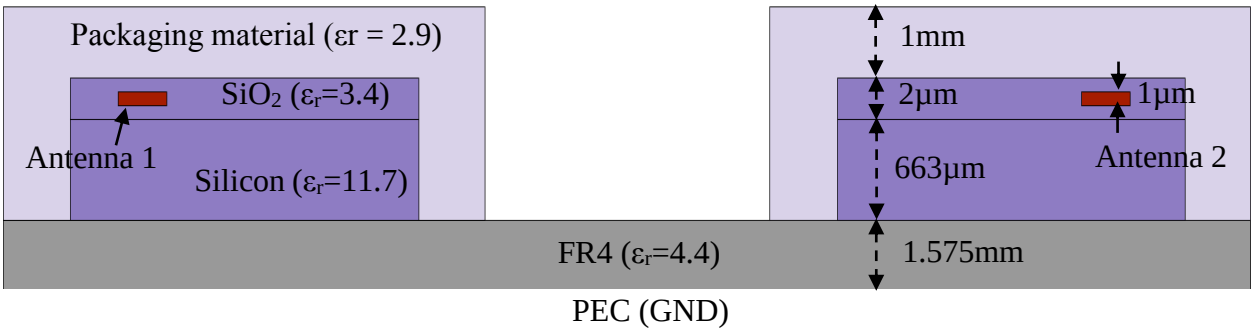
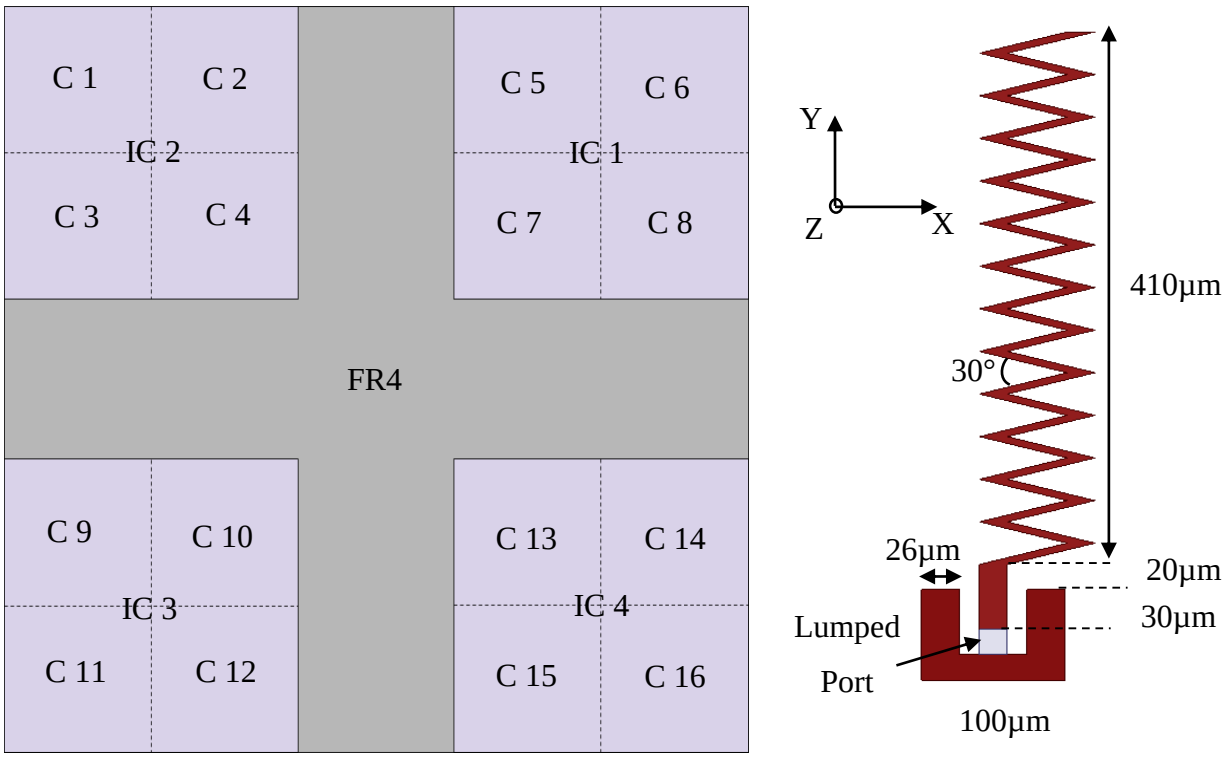


Figure 3-1: Cross-section of the model (Not to scale)

In this chapter, MCMC system is considered to have sixteen cores distributed in four chips (ICs). A top view of the MCMC system placed on FR4 is shown below in Figure 3-2 (a). Wireless interconnect is placed at the center of cores. CPW-fed zigzag antenna is implemented as wireless interconnect because of its small size and easy to fabricate design. The zigzag antenna is shown in Figure 3-2 (b). The antenna is used for all configurations as wireless interconnect.



(a) (b)

Figure 3-2: (a)MCMC system (Not to scale), C is core; (b) zigzag antenna with dimensions.

The chapter is divided into different sections having results of different configurations or antenna arrangement. The configuration #1 has four antennas situated at corner furthest cores. Configuration #2 considers four antennas with two antennas located on one chip for intrachip communication and other two antennas are located on different chips for interchip communication. Configuration #3 takes same antenna positions as in configuration #2, but changes the orientations.

3.1. Configuration 1

Four antennas are located at the four corner cores as wireless interconnects as shown in Figure 3-3. This case is for demonstrating the transmission coefficient for the farthest cores. The cross section view of the setup is shown in Figure 3-1. Wireless interconnect used is zigzag antennas as shown in Figure 3-2 (b). The interconnect is placed at the center of the core. Maximum distance is 59mm between antenna pair (ANT1, ANT2), and (ANT3, ANT4) as shown in the figure. Moreover, the distance between The distance between The orientation of all four wireless interconnect is shown in the inset in Figure 3-3.

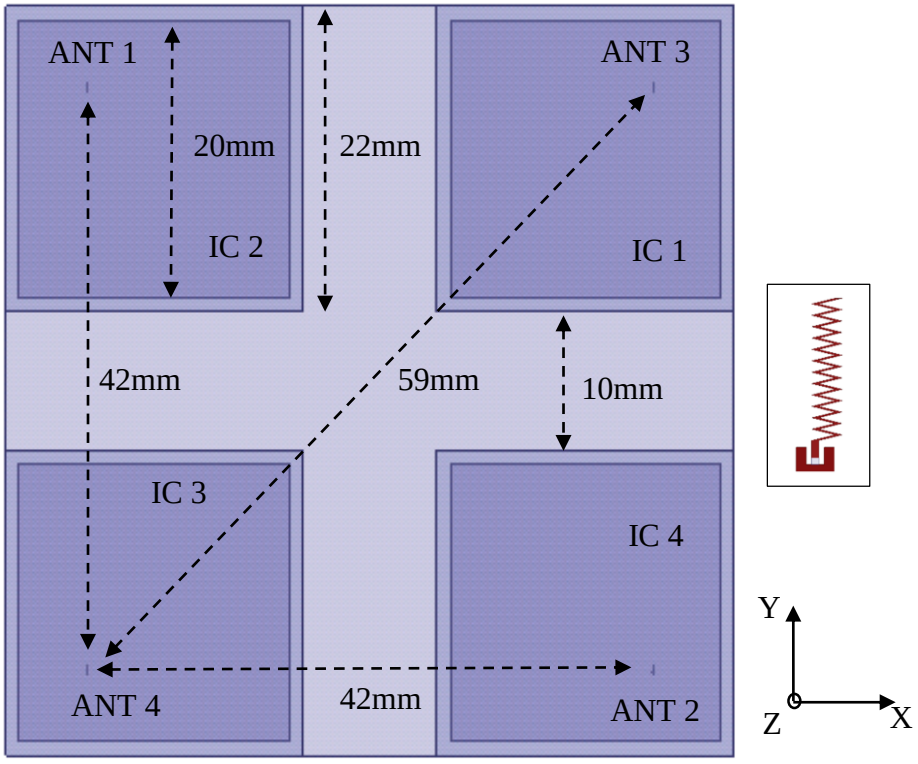


Figure 3-3: Top view of Configuration #1.

The return loss of all four antennas are shown in Figure 3-4. All four antennas are resonating at 60 GHz with return loss of less than -35dB.

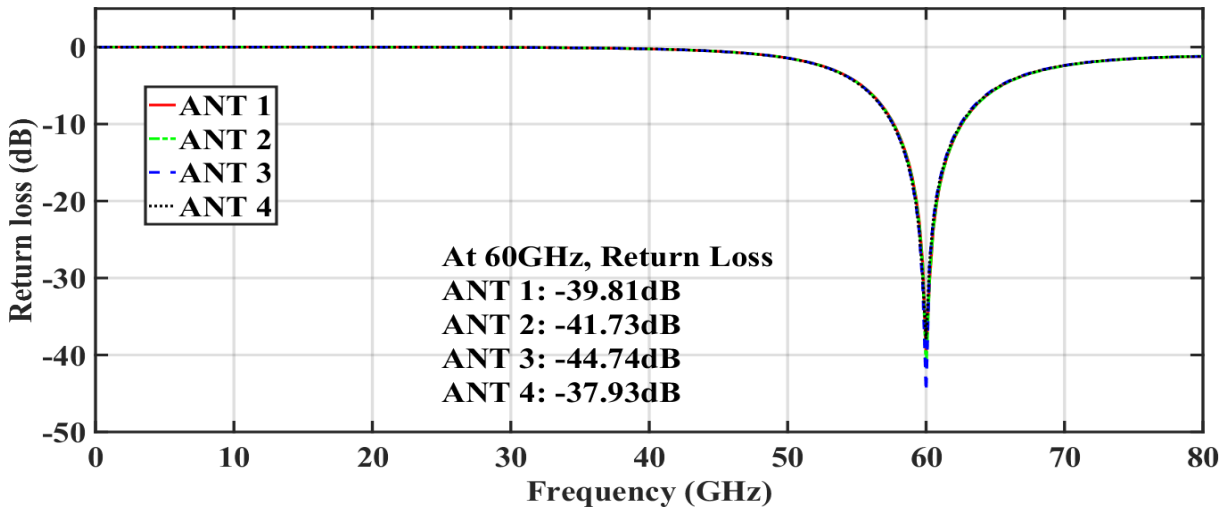


Figure 3-4: Return loss of four antennas.

The transmission coefficients between different antennas are shown in Figure 3-5. The transmission coefficient between farthest interconnects is -45dB for pair (ANT1, ANT2), and is -44.56dB for pair (ANT3, ANT4), which is about the same. These antenna pairs were expected to have the lowest transmission coefficients due to the fact that the path loss should have been the main factor causing the they are placed. Furthermore, it is noted that the pair (ANT1, ANT3) has lowest transmission coefficient of -50dB, which due to inconsistent radiation pattern of wireless interconnect on large silicon wafer.

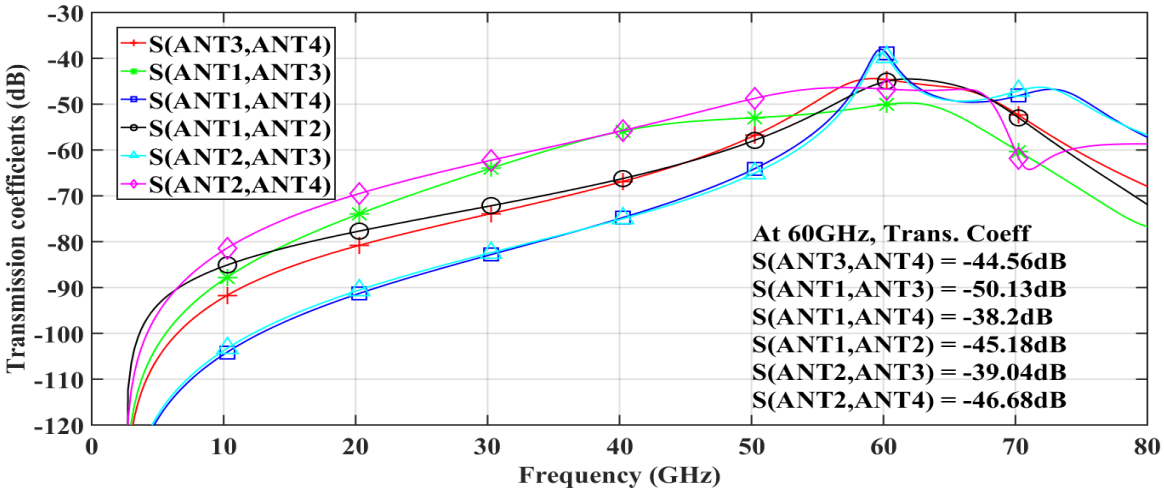


Figure 3-5: Transmission coefficients.

3.2. Configuration 2

Following two configurations are simulated. Both configuration has same four antennas placed at same positions. The only difference is the orientation of antennas. In configuration 2, all antennas are oriented towards top, however, in configuration 3 the orientation is 45° rotated. The rotation of orientation makes the radiations from antennas directly towards each other's main beam. The cross-section view of the setup is shown in Figure 3-1.

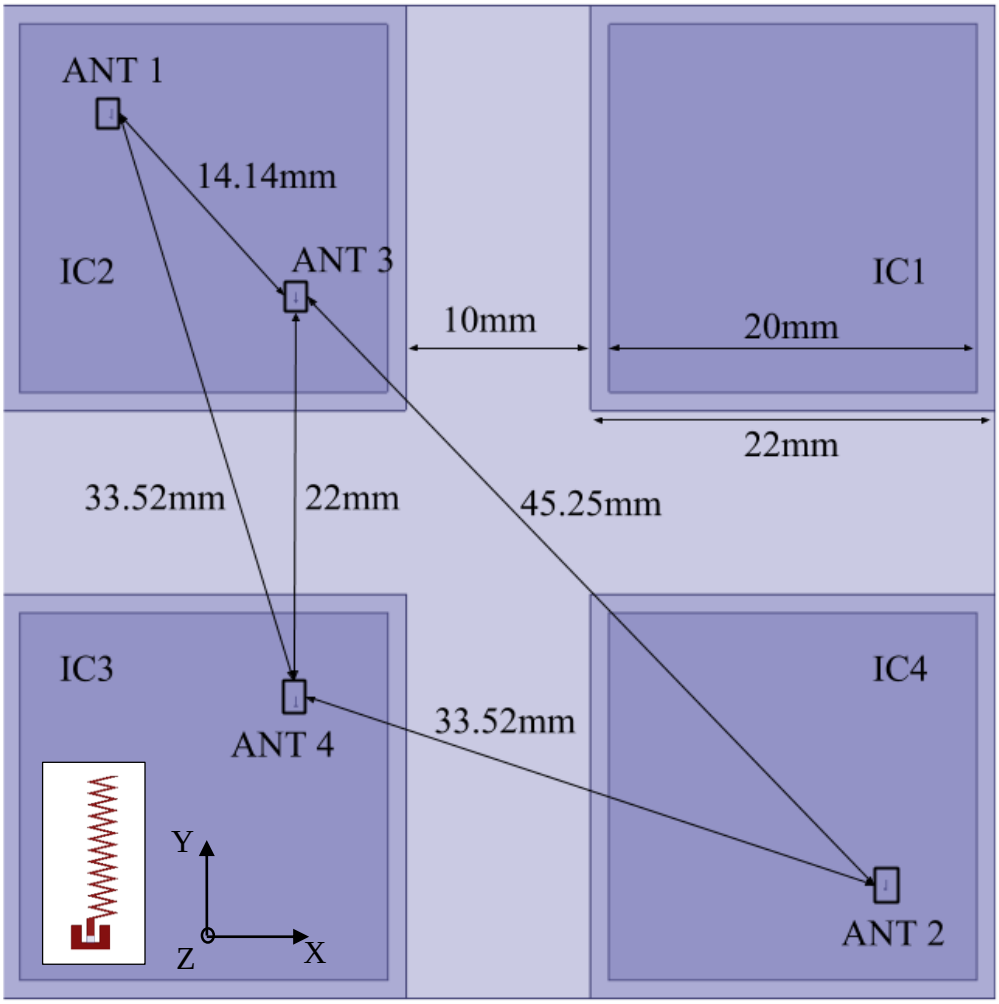


Figure 3-6: Top view of configuration 2. Orientation of antenna is shown in inset.

The return loss of antennas is shown in Figure 3-7. All the antennas are resonating at 60GHz with a return loss of less than -20dB.

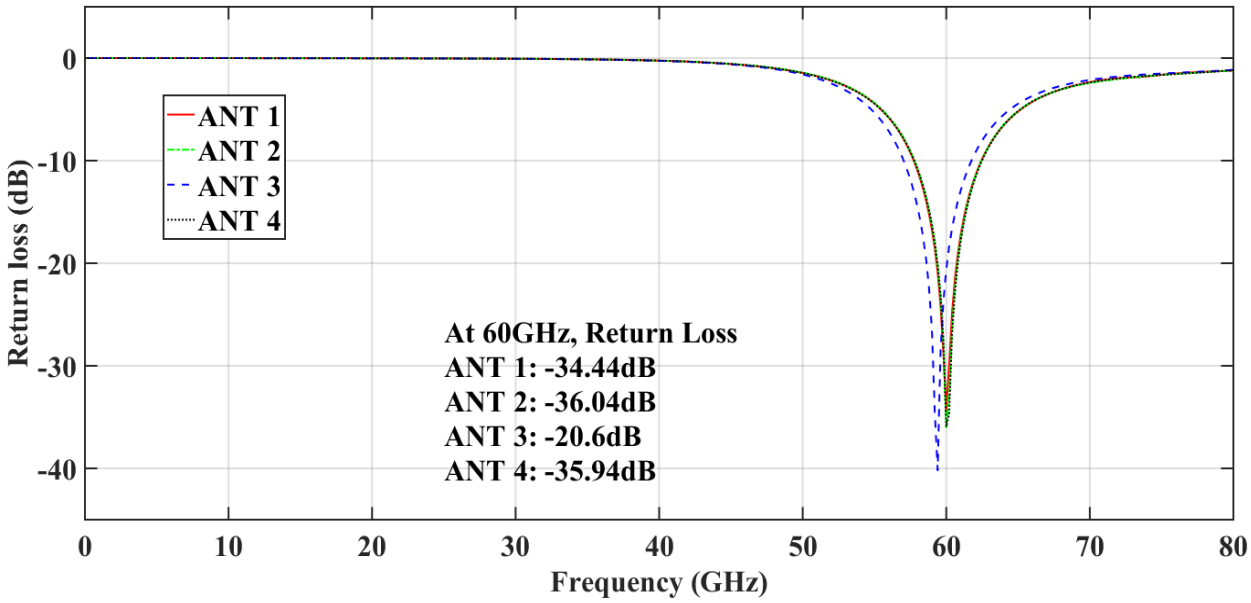


Figure 3-7: Return loss of wireless interconnects.

The transmission coefficients between antennas is plotted in Figure 3-8. It can be seen that the antenna 1 and 3 has maximum transmission coefficients. Moreover, the transmission coefficients between antenna 1 and 4 is -51dB which is the worst.

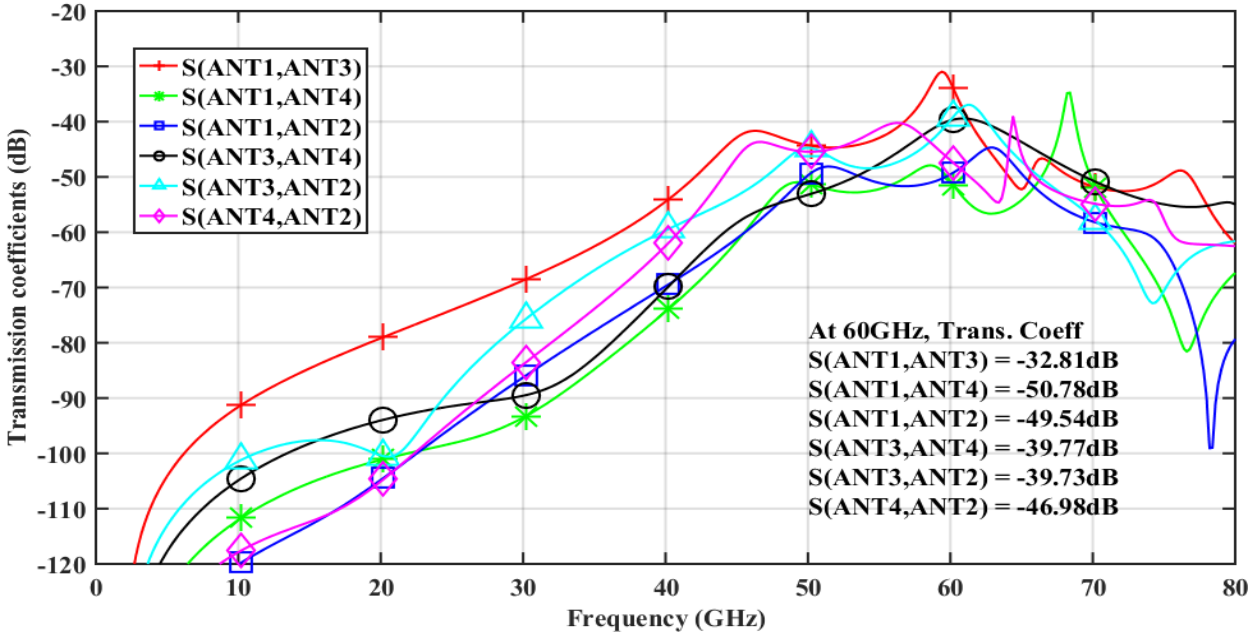


Figure 3-8: Transmission coefficients of antennas.

The radiation patterns for all four antennas are shown below which are Gain Total parameter in HFSS. It can be seen that the radiation pattern varies with antenna position. At some angles the gain reduces by 10-15dB. This tells that the antenna pattern varies with positions and antennas becomes directional.

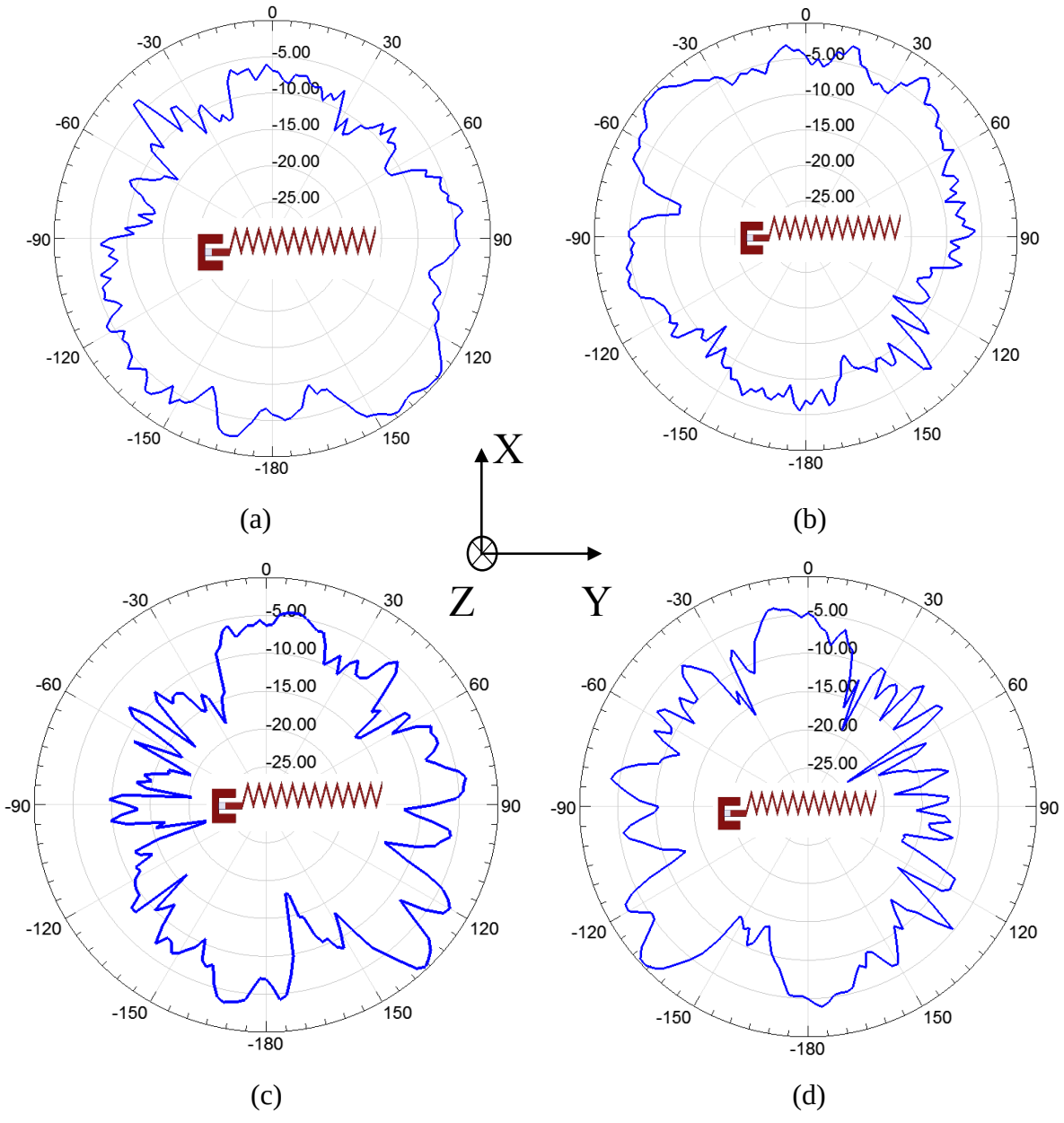


Figure 3-9: Radiation pattern (Gain Total in HFSS) in azimuthal plane for configuration #2. (a) ANT 1, (b) ANT2, (c) ANT3, (d) ANT4. Note: the antenna orientation in the model (Figure 3-6) and radiation pattern is inverted. Please read above plots carefully.

3.3. Configuration 3

In this configuration the antennas are oriented 45° to the Y-axis. It can be seen that the location of the antenna is same as configuration #2. The cross section of the setup is shown in Figure 3-1.

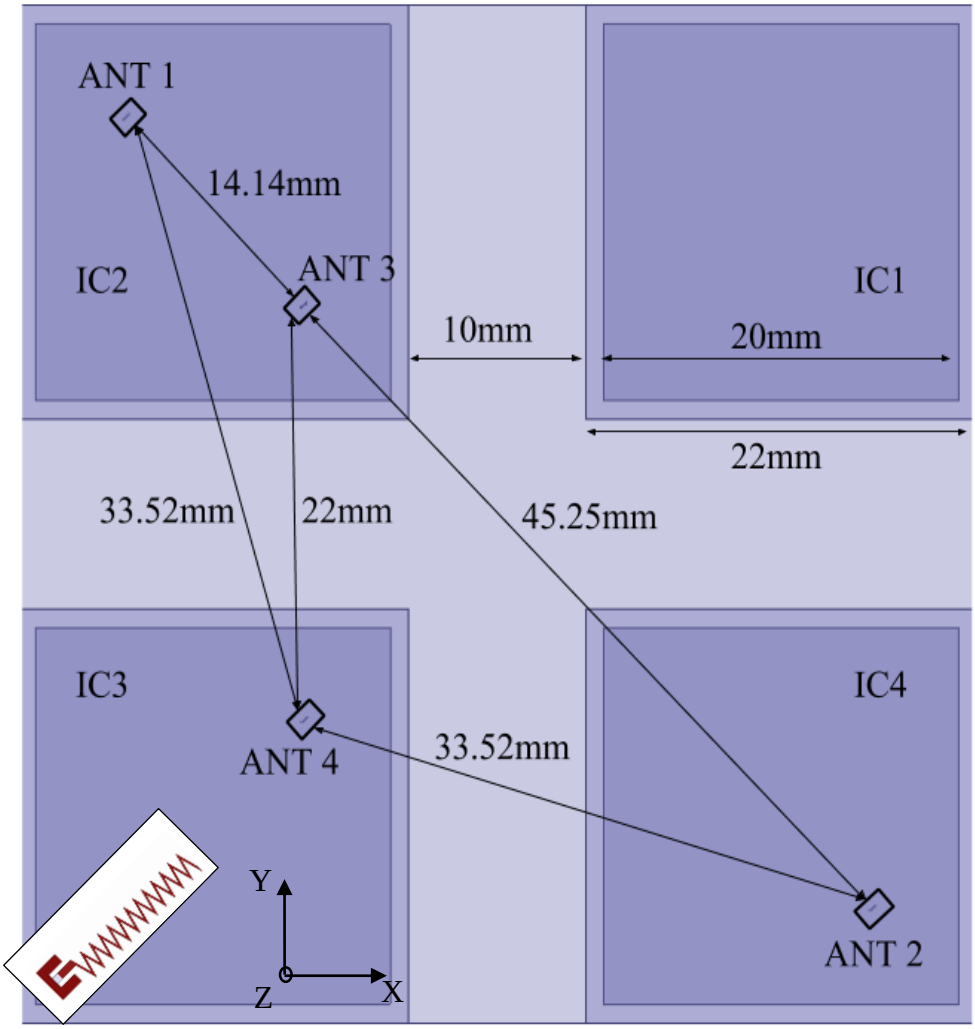


Figure 3-10: Top view of configuration #3. Inset: antenna orientation.

The return loss of the antennas are shown in Figure 3-11. The antennas are resonating at 60GHz with return loss less than -20dB.

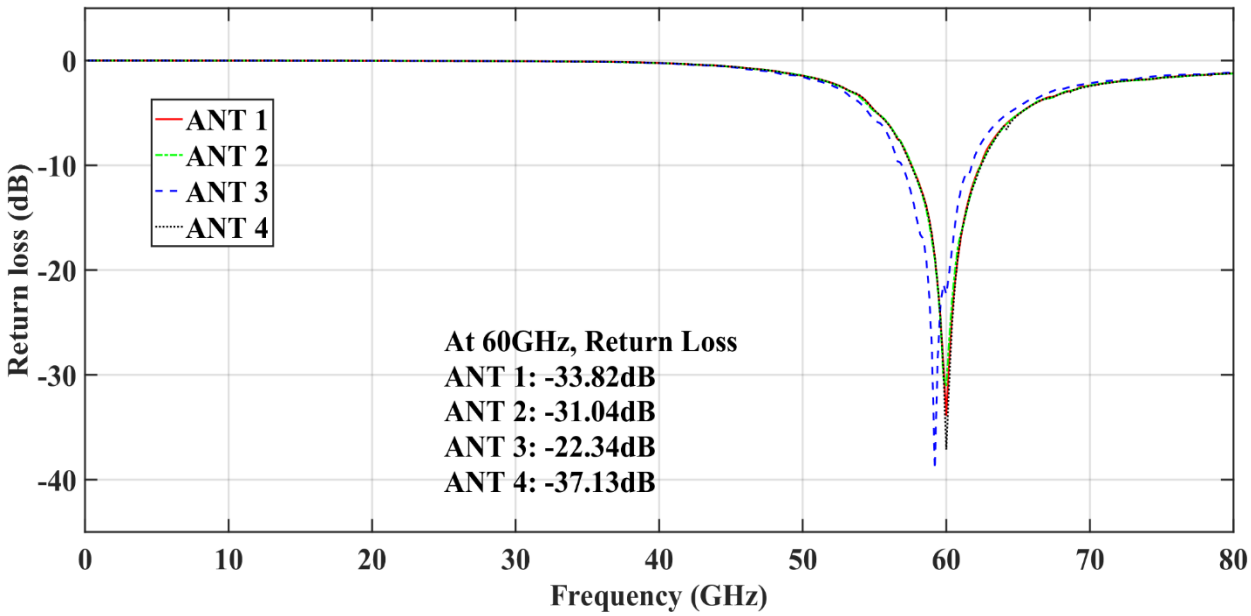


Figure 3-11: Return loss of antennas.

The transmission coefficients are shown below. It can be seen that the best transmission coefficient is -31.38 dB between pair ANT 1 and ANT 3. The worst transmission coefficient is -48 dB between pairs ANT 3 & ANT 4, and ANT 2 & ANT 4.

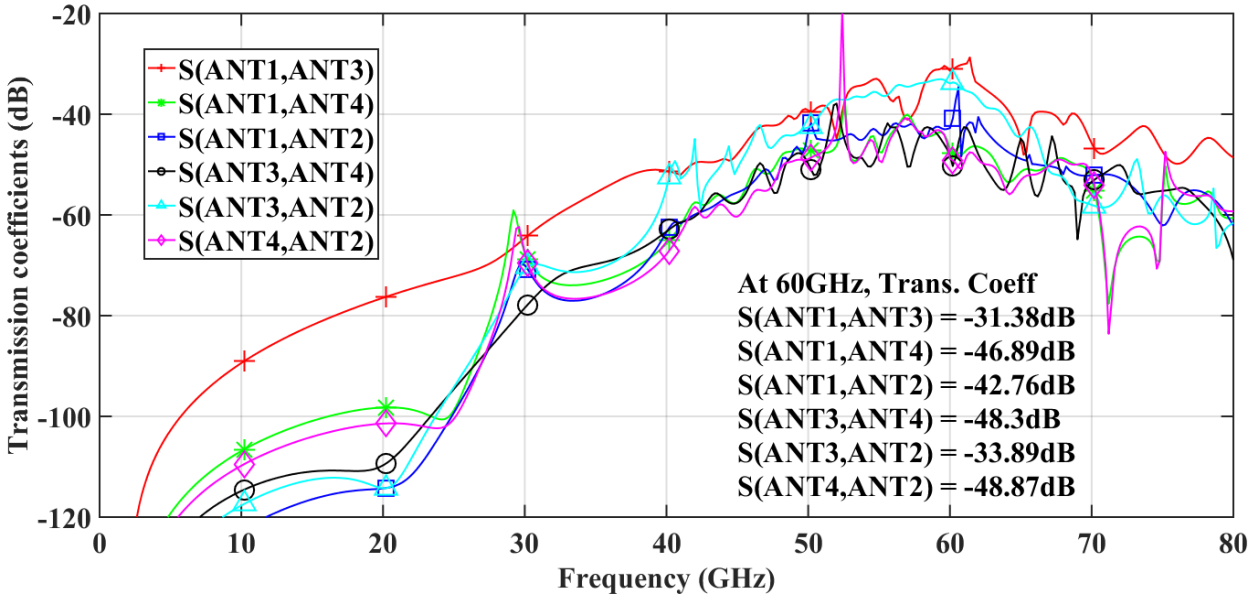


Figure 3-12: Transmission coefficients.

The transmission coefficients at 60 GHz of configuration #2 and configuration #3 is tabulated in Table 2.

Table 2: Transmission coefficients of configuration #2 and #3 at 60 GHz

Trans. Coeff. (dB)	**Configuration 2**	**Configuration 3**
S12	-49.54	-42.76
S13	-32.81	-31.38
S14	-50.78	-46.89
S32	-39.73	-33.89
S34	-39.77	-48.3
S42	-46.98	-48.87

It can be seen that the transmission coefficients for most of the antennas has improved when the orientation has been changed. Only pair ANT 3 & ANT 4, ANT 2 & ANT 4 is reduced. This is happening due to the change in radiation in silicon. The zigzag antennas are no longer omnidirectional with ground plane at the bottom. The radiation patterns for configuration #2 are shown in Figure 3-9. It is noted that the radiation pattern is not omnidirectional.

4. Fabrication of zigzag antenna for MCMC system

Zigzag Antennas are fabricated at Semiconductor and Microelectronics Fabrication Laboratory, RIT. The design and fabrication process is explained in following sections along with the measurements of return loss and transmission coefficients. First, antenna design for fabrication is discussed.

4.1. Simulation design of antennas

The zigzag antennas are designed in ANSYS HFSS [31]. Due to limitations of measuring instruments in lab till 40 GHz, the antennas are designed for 30 GHz. Moreover, antenna has probe pad which are required for taking measurements using Ground-Signal-Ground (GSG) probe. The pitch of the probe pad is 150µm. The minimum size of probe pad should be 50µm x 50µm. So it is better to take a large enough probe pad, the designed probe pad has size of 70µm x 70µm. The design is divided into three configurations with different antenna orientation. Configurations are discussed in later sections.

The simulation & fabrication setup is shown in Figure 5 1. The Si die has thickness 675 µm. The dielectric constant and resistivity of silicon die is taken as 11.7 and 55Ω-cm (σ = 1.8S/m), respectively. The SiO2 layer has thickness 2 µm and dielectric constant εr = 3.4. On top of SiO2, Al antennas are designed with a thickness of 1 µm. Same setup is used to design all the antennas.

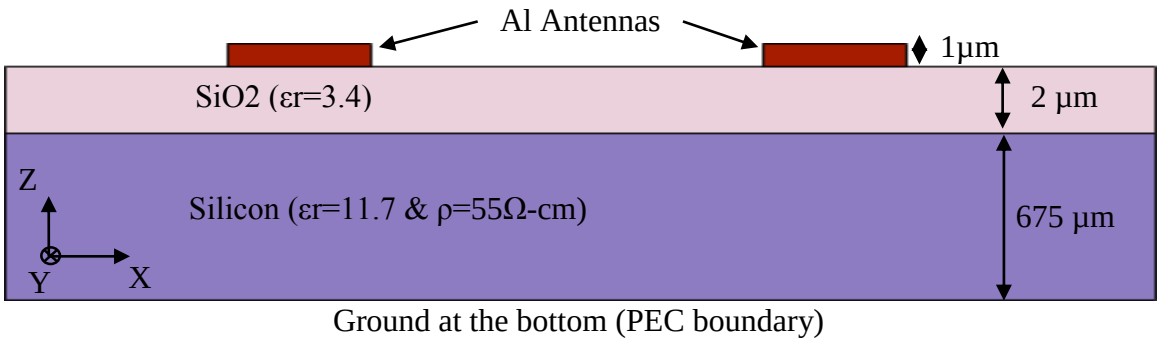
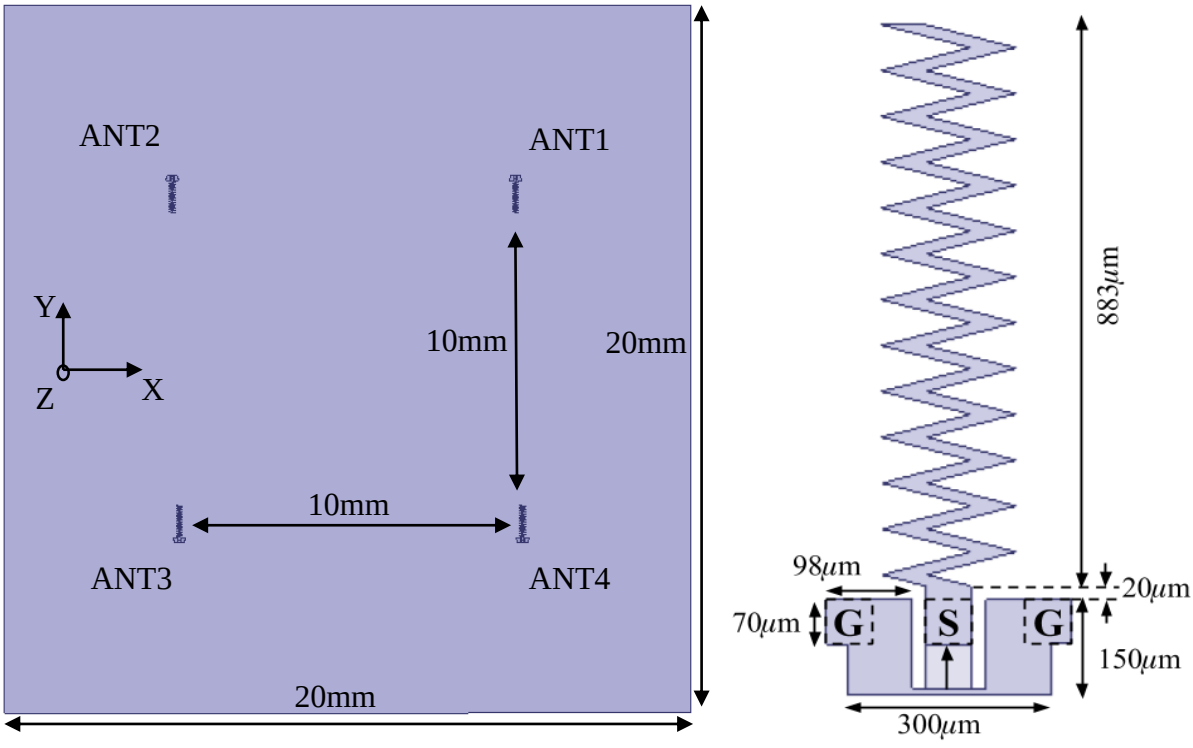


Figure 4-1: Cross-section of fabrication setup (Not to scale).

4.1.1. Configuration 1

The top view of the 20mm x 20mm die shows the arrangement of antennas. The antennas are oriented towards each other. The zigzag monopole antenna with probe pad is designed to resonate at 30 GHz. It is shown in Figure 4-2 (b). The distance between antennas is 10mm.



(a) (b)

Figure 4-2: (a) Top view of configuration 1; (b) Zigzag antenna with GSG probe pads.

All antennas are resonating at 30GHz with a return loss of around -15dB shown in Figure 4-3.

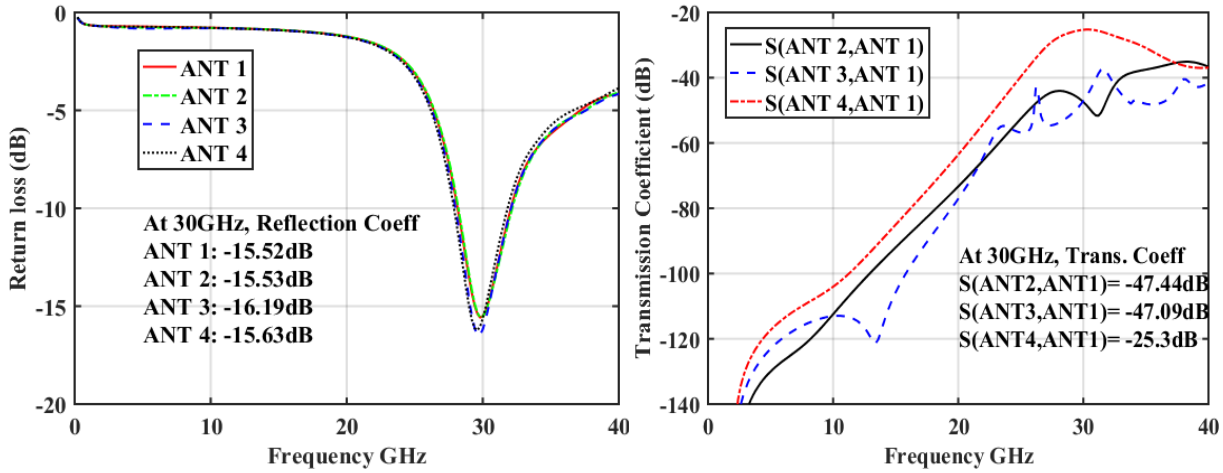


Figure 4-3: Return loss and transmission coefficients for configuration #1.

4.1.2. Configuration 2

The setup for configuration 2 is same as configuration 1 and is shown in Figure 4-1.The top view with antenna orientation for this configuration is shown in Figure 4-5. The size of die is 20mmx20mm. The distance between antennas is 10mm in Y-axis. Due to the restriction of the probe movement on probe station, additional curved feed is required for antenna orientation in this configuration. The antenna design is shown in Figure 4-4. The CPW feed gap is 15µm.

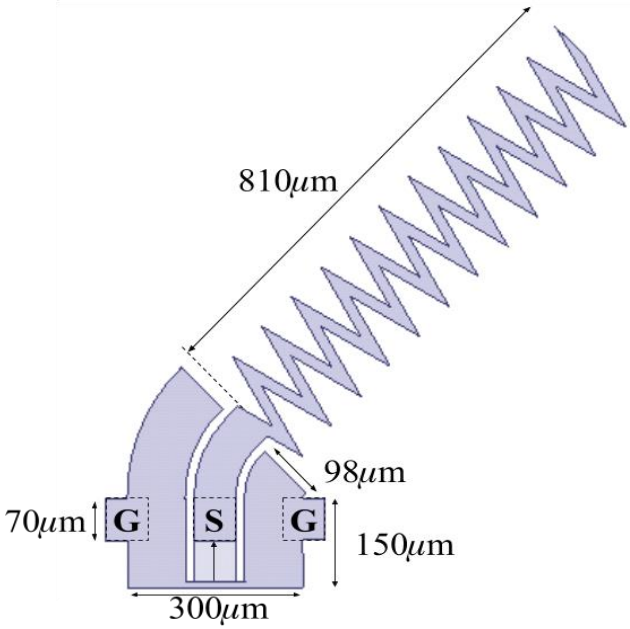


Figure 4-4: Curved CPW-fed zigzag antenna design with probe pads.

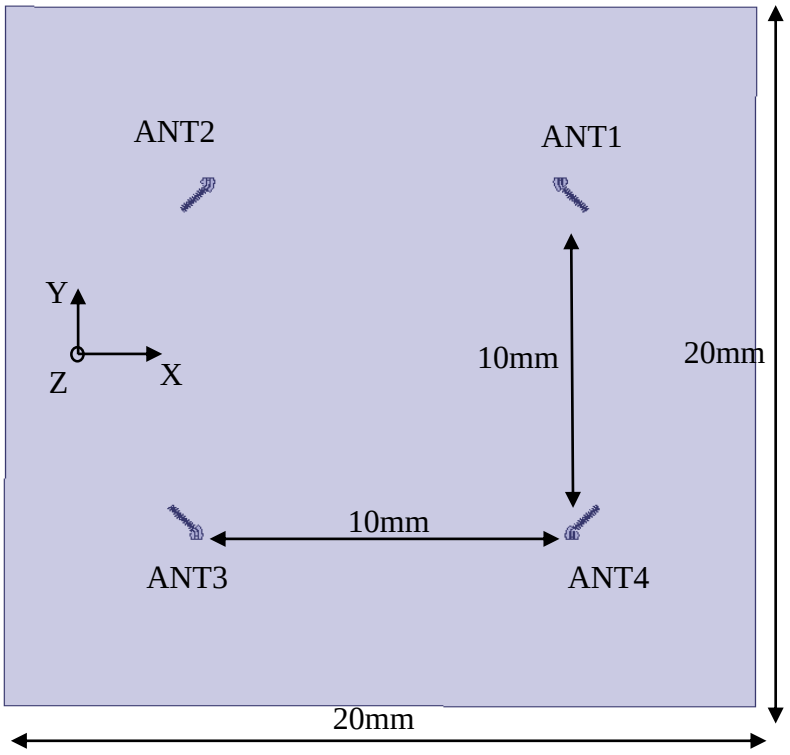


Figure 4-5: Top view of configuration #2.

All antennas are resonating at 60GHz with return loss around -20dB. The plot is shown below. The transmission coefficients between antennas are shown in Figure 4-6.

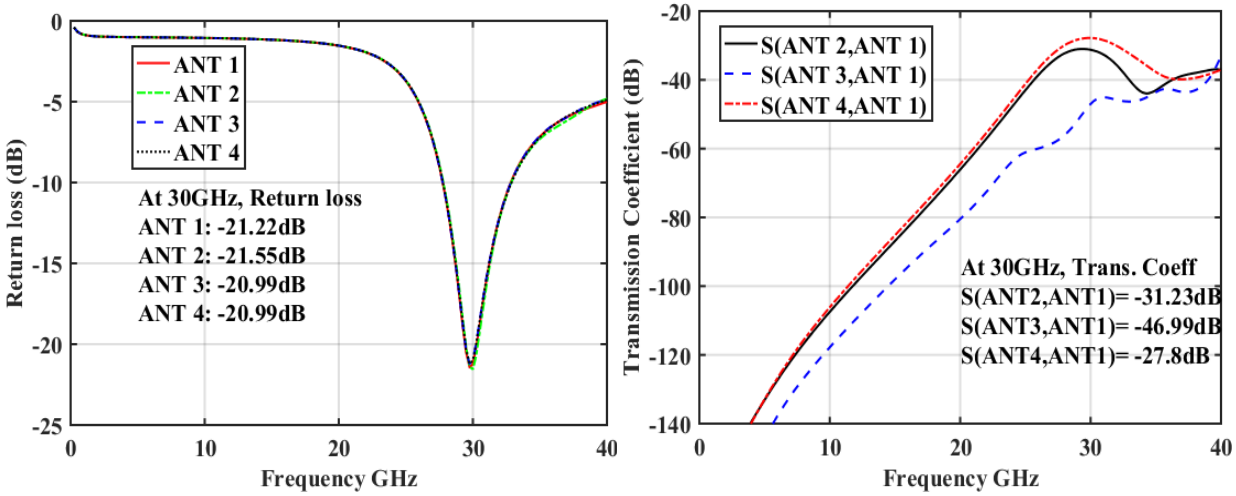


Figure 4-6: Return loss and transmission coefficients for configuration #2.

4.1.3. Configuration 3

The configuration #3 uses antenna with same dimension as used in configuration 2. The antenna is shown in Figure 4-4.

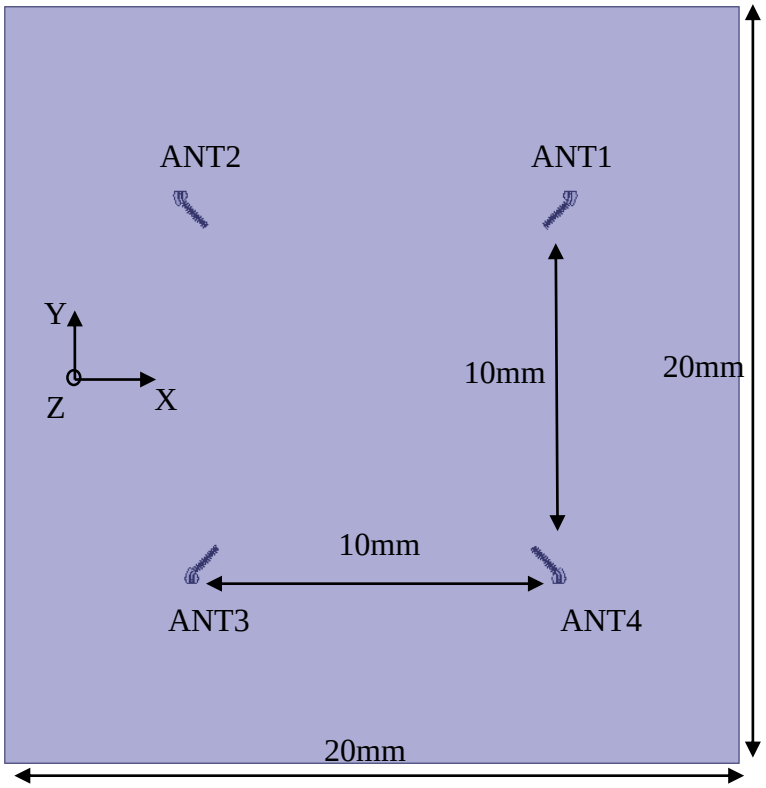


Figure 4-7: Return loss and transmission coefficients for configuration #3.

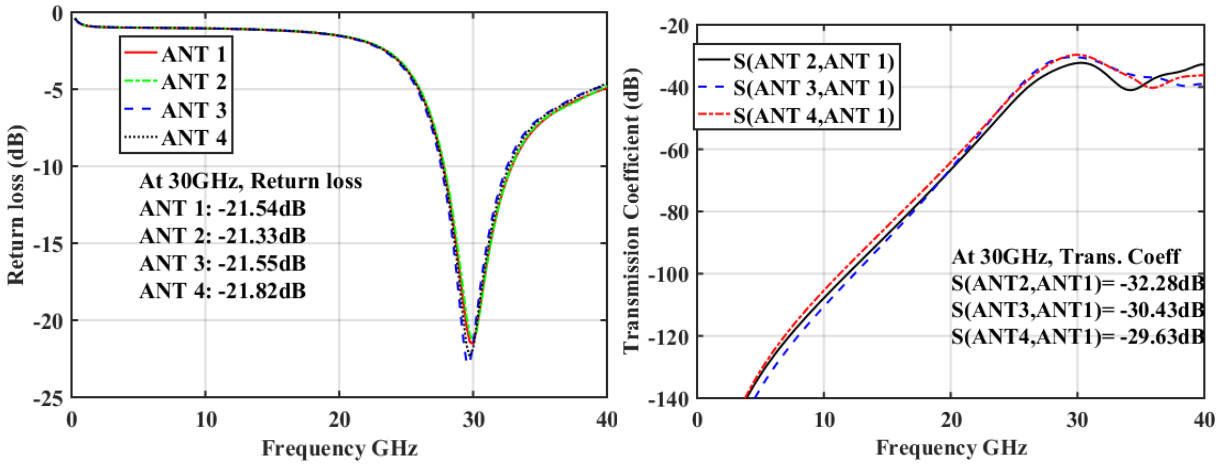


Figure 4-8: Return loss and transmission coefficients for configuration #3.

4.2.Fabrication of antennas

After simulations for three configurations were successfully performed in ANSYS HFSS, GDSII files are exported. The GDSII files from all three configurations are combined into a mask layout file which is used for mask preparation. This mask is later used for Lithography. The fabrication is done on 6'' Silicon wafer. The fabrication is performed using basic CMOS fabrication process. First, the Si wafer is cleaned with RCA cleaning process. Then resistivity of the wafer is measured. Average resistivity of wafer is found to be 55Ω-cm using four-point probe method. Further, wafer cleaning is performed since the four-point measurement technique is destructive process. Now, 2µm of SiO2 is grown on Silicon wafer using wet oxide growth process in furnace for 16 hours.

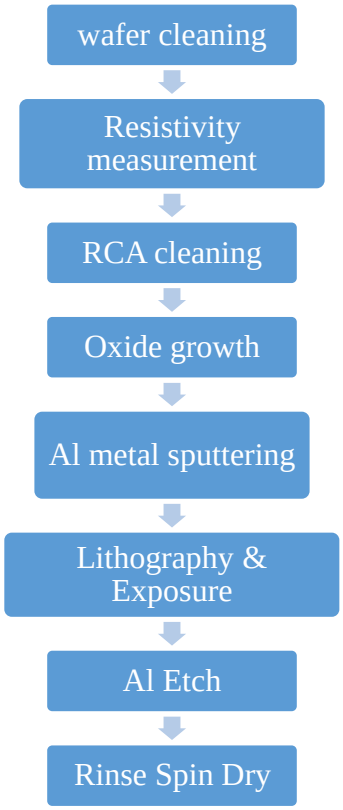
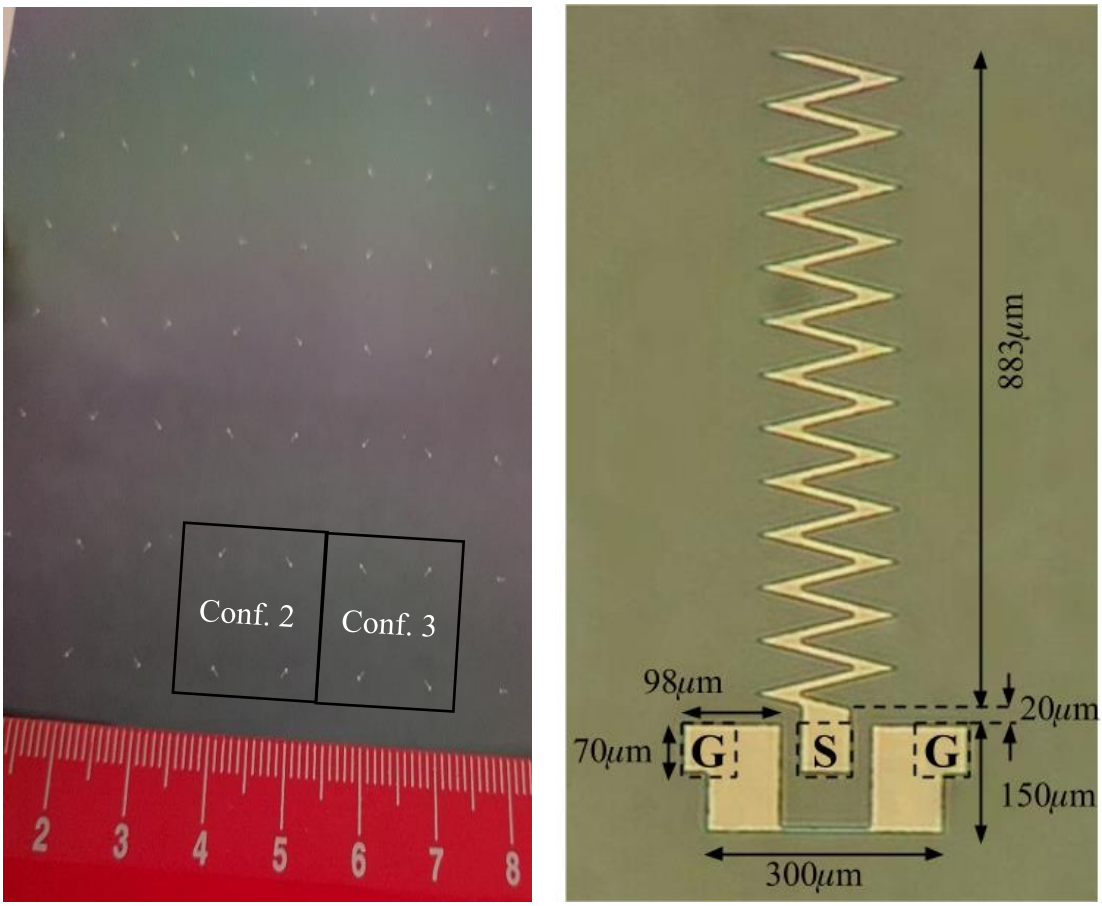


Figure 4-9: Fabrication process.

Aluminum is deposited using sputter deposition. The thickness of Al is 1µm. Photoresist is coated over the Al covered wafer. Then, wafer is exposed to light with mask in between. The excess Al is etched off the wafer. In this way zigzag antennas are fabricated on silicon wafer.



(a) (b)

Figure 4-10: (a) Fabricated antenna close up view, (b) Fabricated antenna for conf. 1.

4.3.Measurements & Results

The Cascade ACP40-A are GSG (Ground-Signal-Ground) probes. They have a pitch of 150 µm and minimum pad size requirement of 50 µm. The probes are connected to Agilent PNA 8363B with low-loss coax cables. Cascade WinCal XE 4.7 is used for calibrating PNA and exporting the measured data. A picture of measurement instruments is shown in Figure 4-11.

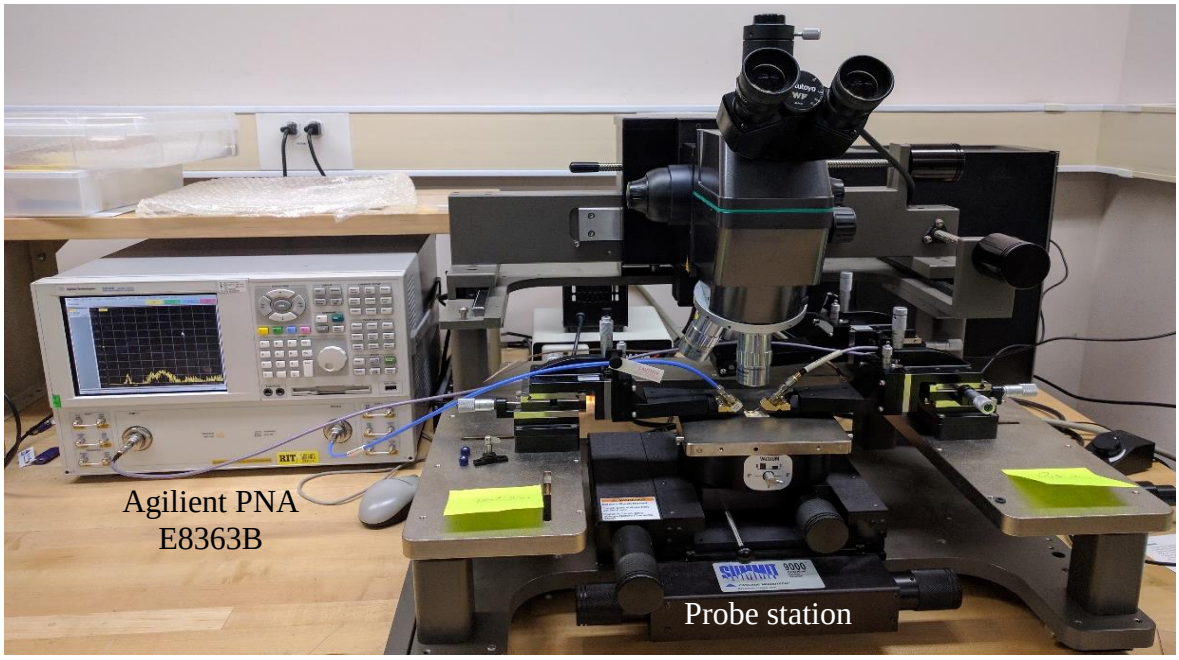


Figure 4-11: Measurement instruments.

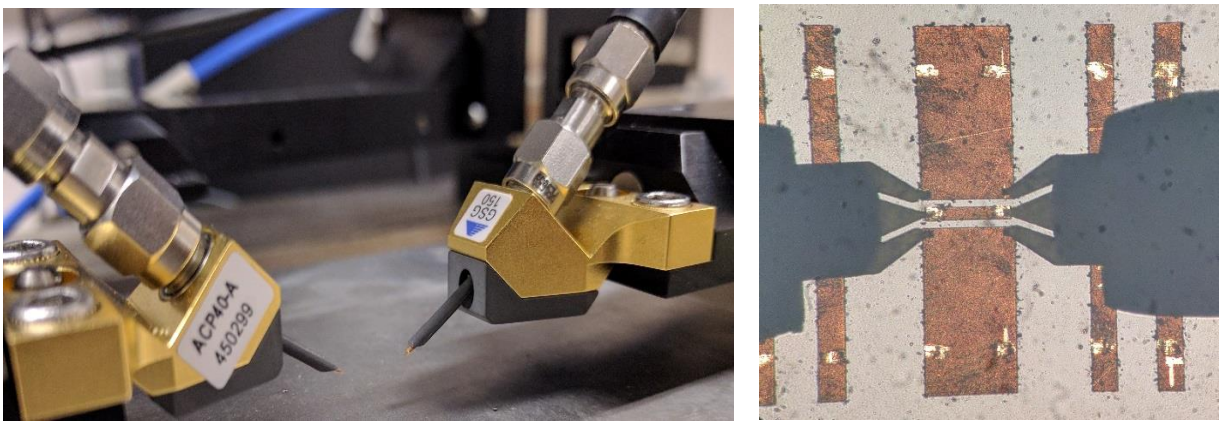


Figure 4-12: (a) Cascade ACP40-A probes, (b) Calibrating the system using standard (thru).

The calibration is performed using Cascade impedance standard substrate P/N 106-682. The network analyzer is calibrated from 1GHz to 40GHz by calibration wizard of WinCal. The probes are placed on probe pad

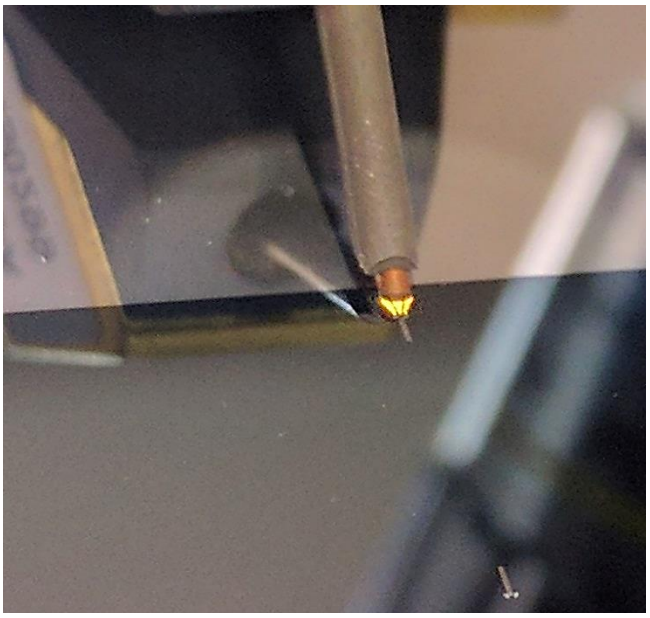


Figure 4-13: Probe placement on probe pad of an antenna. Another antenna is visible head-on.

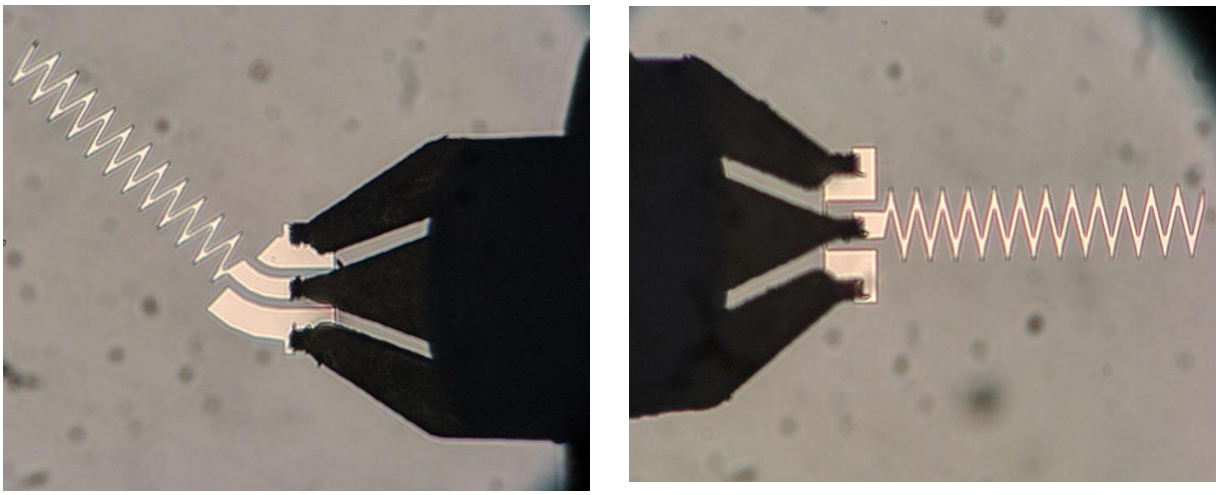
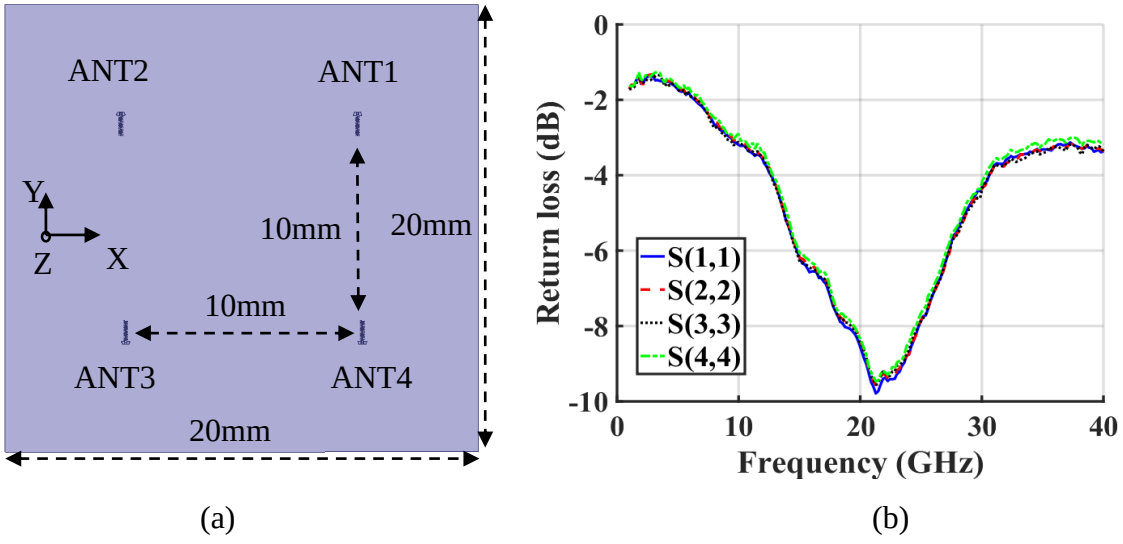


Figure 4-14: Testing fabricated antenna using GSG probes on probe pads.

It can be seen that the probe pads are properly designed. The probe can properly sit on the pads.

4.3.1. Configuration 1

Measured return loss and transmission coefficient for configuration #1 is shown below. It can be seen that the antennas are resonating at about 22 GHz with a return loss of -9dB.



(a) (b)

Figure 4-15: (a) Configuration 1, (b) Measured return loss of antennas for configuration 1.

The transmission coefficients are shown below. At 22GHz, the transmission coefficients (S31 and S41) is about -45dB. S21 cannot be measured because of probe station constraint.

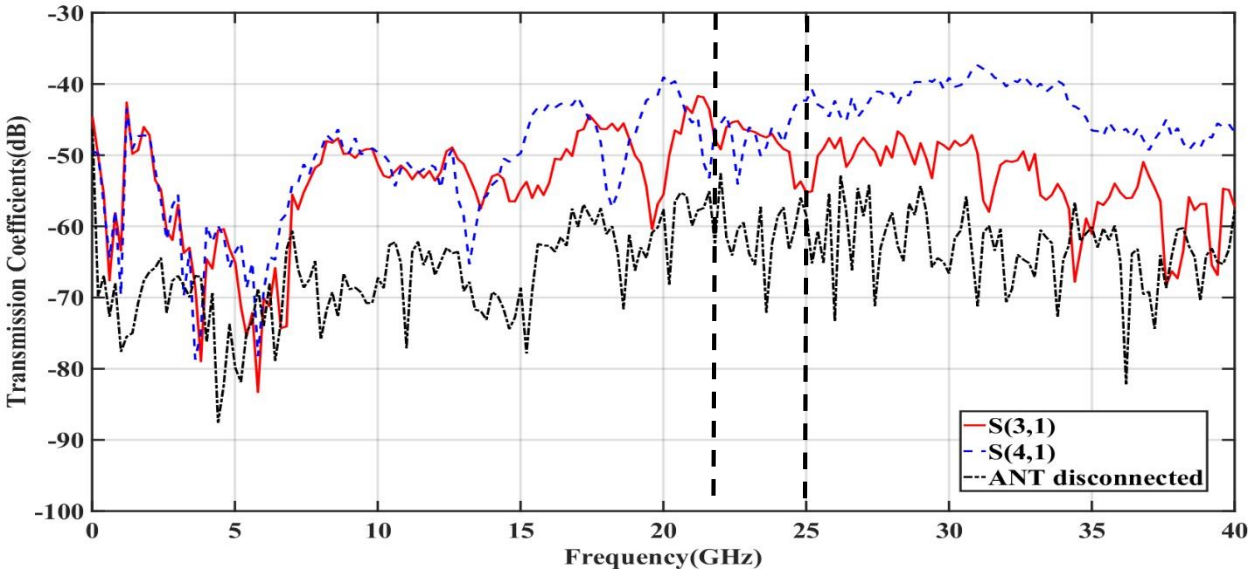


Figure 4-16: Measured transmission coefficients for configuration 1.

4.3.2. Configuration 2

Antenna in configuration 2 are resonating at 24GHz with a return loss of -12dB.

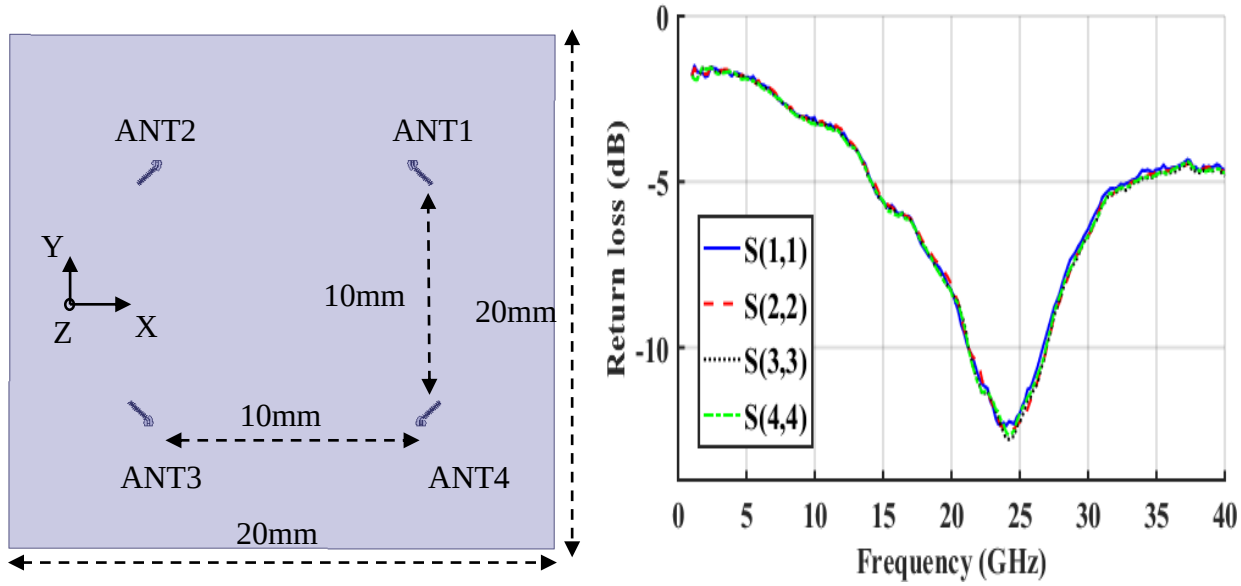


Figure 4-17: Measured return loss of antennas for configuration 2.

The transmission coefficients are shown in Figure 5 18. It can be seen that the transmission coefficients (S31 and S41) at around 25GHz is -45dB.

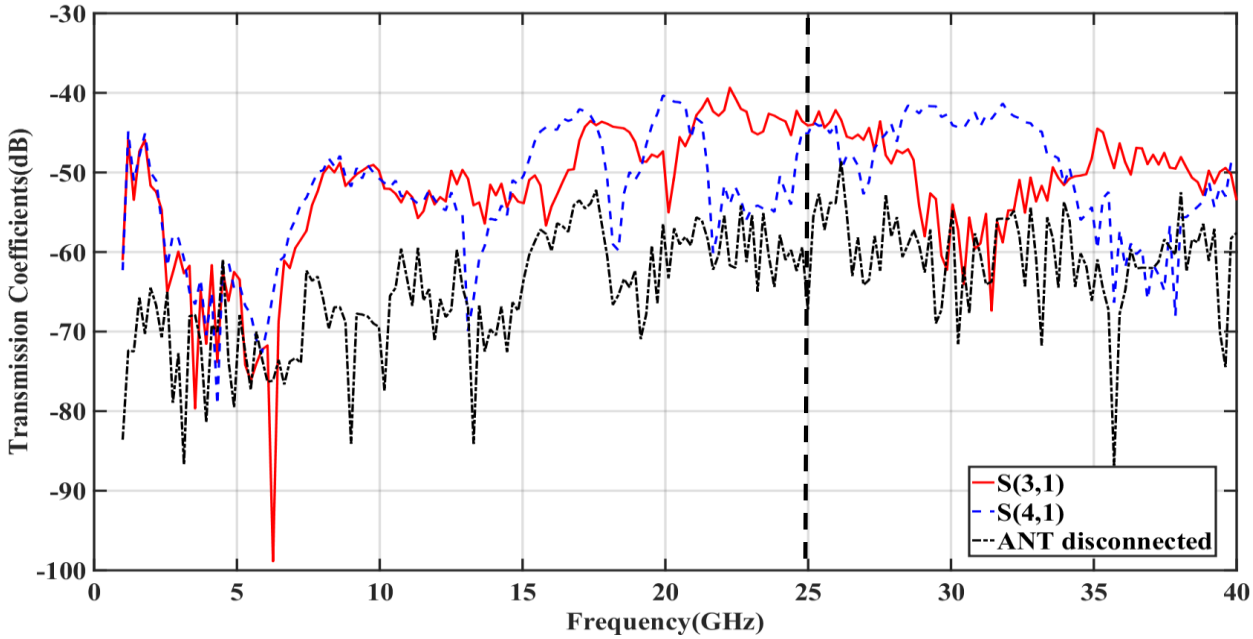


Figure 4-18: Measured transmission coefficients for configuration 2.

4.3.3. Configuration 3

For configuration 3, the return loss is similar as configuration 2 that is about -12dB at 25GHz.

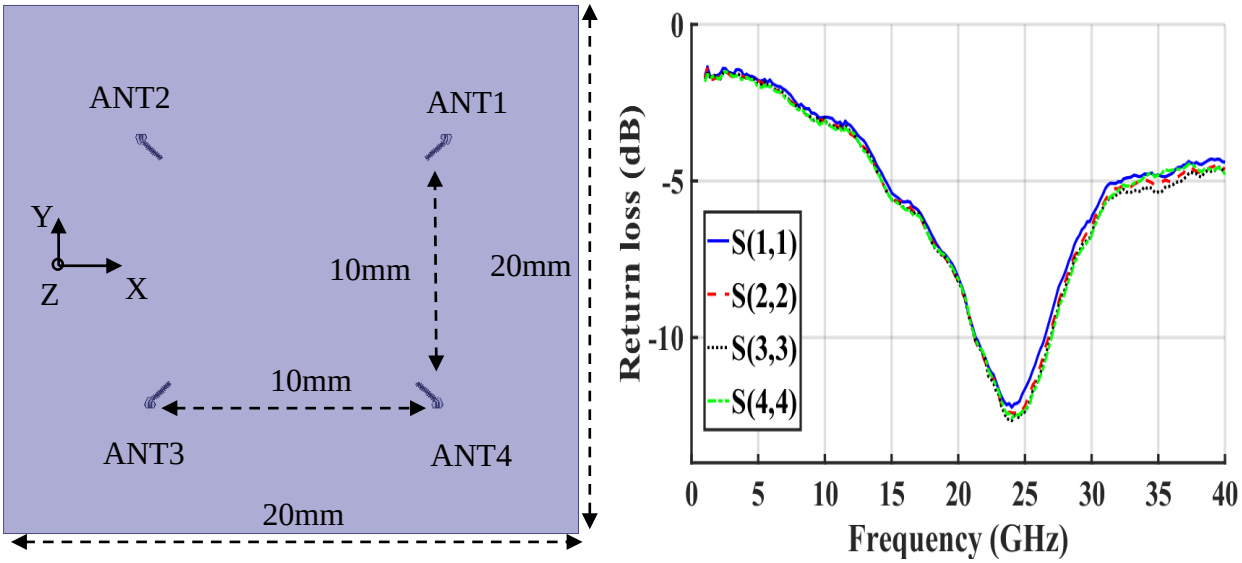


Figure 4-19: Measured return loss of antennas for configuration 3.

Note: S21 cannot be measured due to probe station constraint.

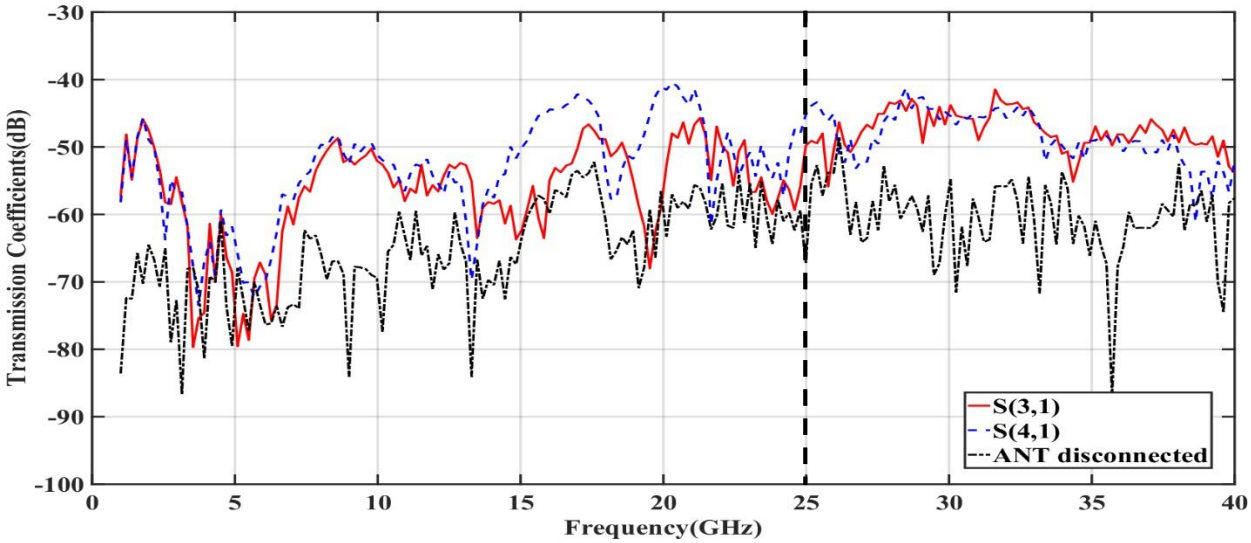


Figure 4-20: Measured transmission coefficients for configuration 3.

It should be noted from above measurements that the resonant frequency is shifted from 30GHz to 21GHz for configuration 1, and for configuration 2 and 3, the resonant frequency is shifted from 30GHz to 24GHz. This can be fixed in new designs by further reducing the size of antenna. Furthermore, silicon fabrication process allows to fabricate more than one design on a wafer at once, therefore, in future, the fabrication should be performed with manufacturing variations, so as to understand the resonance of antennas with variation of lengths. Manufacturing variation can help to find optimum length of antenna working at 30GHz.

Moreover, after comparing transmission coefficients from simulation and measurement, it is noted that the simulated transmission curves are smooth while transmission in fabricated has unexpected values. For example, in configuration #3, despite about -5dB return loss (SWR > 3) in frequency range from 28GHz to 35GHz, significant transmission can be observed. These unexpected transmissions might be due to better radiation pattern w. r. t. frequencies and angles.

Table 3 collects all the measured transmission coefficients of different configurations at frequency 25GHz. It can be seen that the transmission coefficients S(4,1) is nearly same for all three configurations. For S(3,1) transmission, configuration #2 is better than other two.

Table 3: Measured Transmission coefficient of fabricated configuration #1, #2 and #3 at 25 GHz

Trans. Coeff. (dB)	**Configuration 1 at 25GHz**	**Configuration 2 at 25GHz**	**Configuration 3 at 25 GHz**
S(3,1)	-55.26	-44.10	-49.78
S(4,1)	-42.34	-45.17	-45.18

Moreover, measured transmission at low frequencies (1-3GHz) is around -50dB which is unexpected since there is no transmission (less than -100dB) at low frequencies in simulations. A

plot of measured transmission coefficients at lower frequencies 0.1-10GHz is provided in Figure 4-21 for configuration #1. The reason is under investigation.

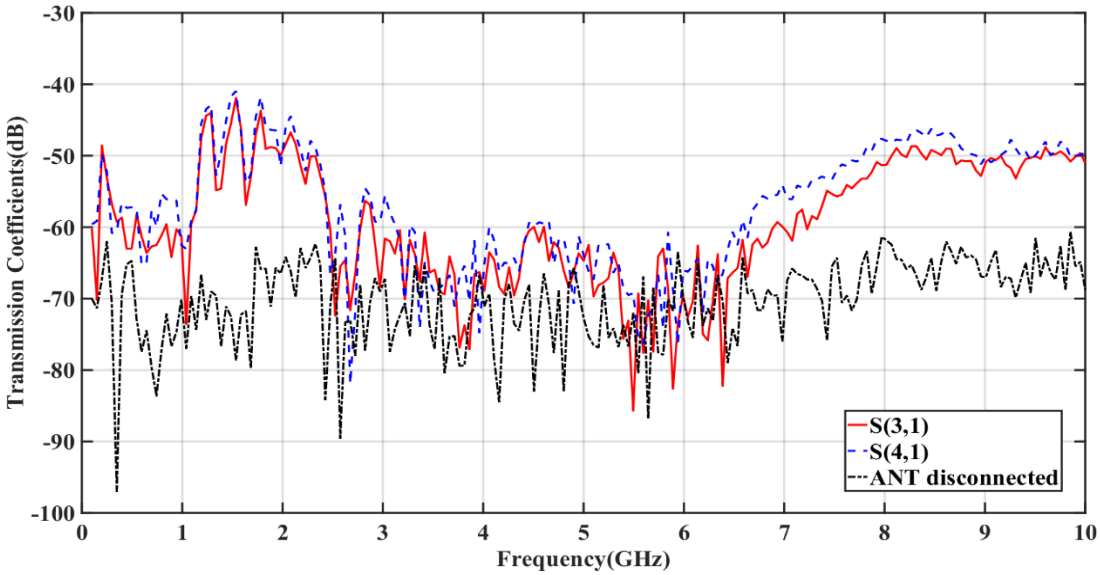


Figure 4-21: Measured transmission coefficients for configuration #1 for frequencies 0.1-10GHz

5. Wireless Interconnects for 3D IC

Recently, Vertical Integrated circuit (3D IC) is of great interest to researchers. One of the 3D IC paper is [45] which implements meander antennas. This work is based on [30] which is simulation based study in 3D IC where zigzag antennas are wireless interconnects. The design is further optimized in different environment with different coolants and antenna orientation.

5.1. Setup of 3D IC

This section presents setup for simulation using ANSYS HFSS of four different designs of 3D IC. Designs have two different configurations – Configuration #1 & Configuration #2. In configuration #1 (Figure 5-1), all the antennas, in all four active silicon layers, are aligned towards Y-axis. In configuration #2 (Figure 5-2), all antenna are aligned towards the center of corresponding Si layer. Two different coolants. Coolant #1 is 3M™ Fluorinert™ Electronic Liquid FC-72 [47] with a dielectric constant (ε_r) of 1.75, and coolant #2 is deionized (pure) water with dielectric constant(ε_r) of 78 [48] at ambient conditions. In all, there are four set of designs.

A 3D IC consists of multiple silicon layers which have transistors and circuits. These silicon layers are known as active silicon. Setup has four such layers with a silicon dioxide layer on top of each of them. The cross section view of 3D IC is shown in Figure 5-3. It is assumed that these four layers will generate heat because of wired metal interconnect. This can increase the temperature, therefore at the center of the IC a cooling layer is designed with multiple microchannels which has continuous flow of liquid coolants. These channels are designed as rectangular tunnels through a bulk silicon layer. For this analysis, microchannels are used due to more heat sinking as per thermal analysis. The dimensions of each layers are shown in Figure 5-3. A total of 16 antennas are placed in middle of silicon dioxide layer.

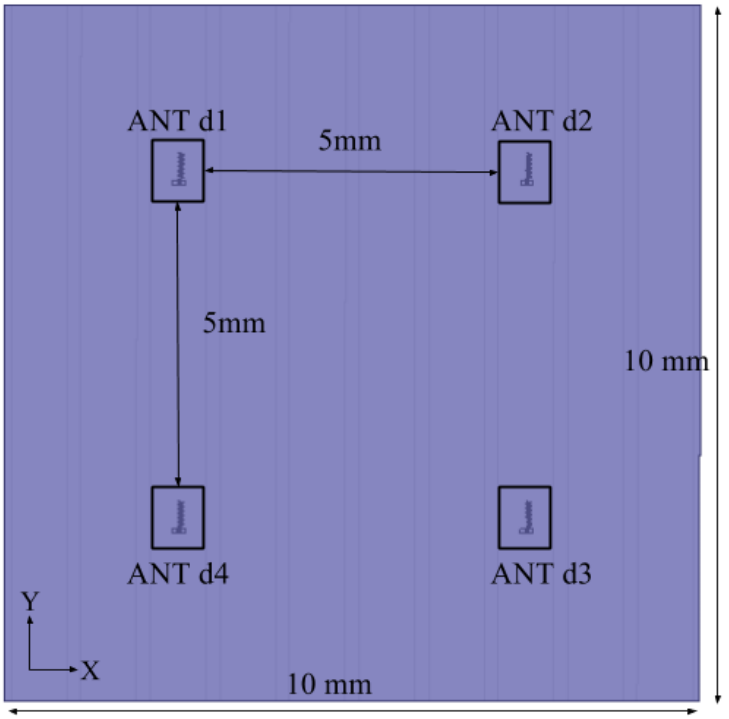


Figure 5-1: Top view of configuration #1.

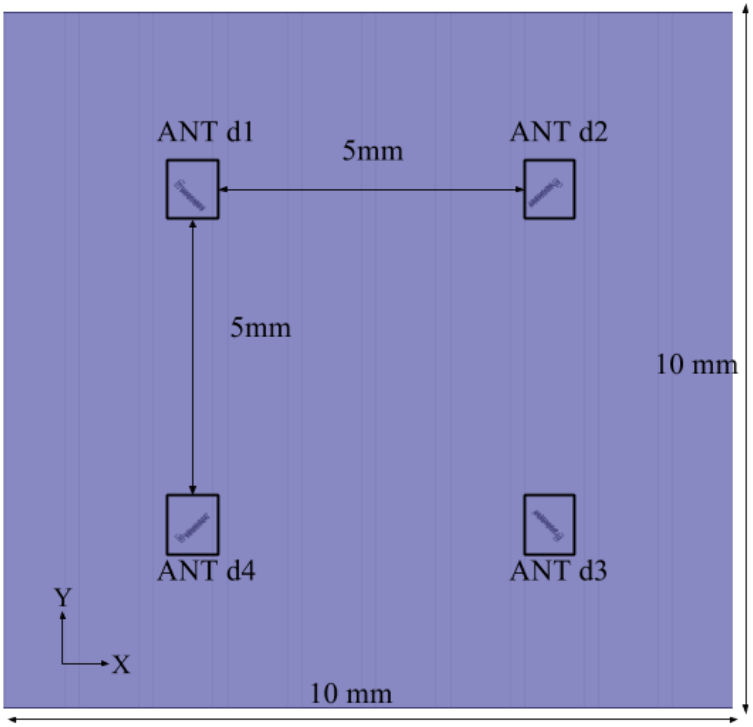


Figure 5-2: Top view of configuration #2.

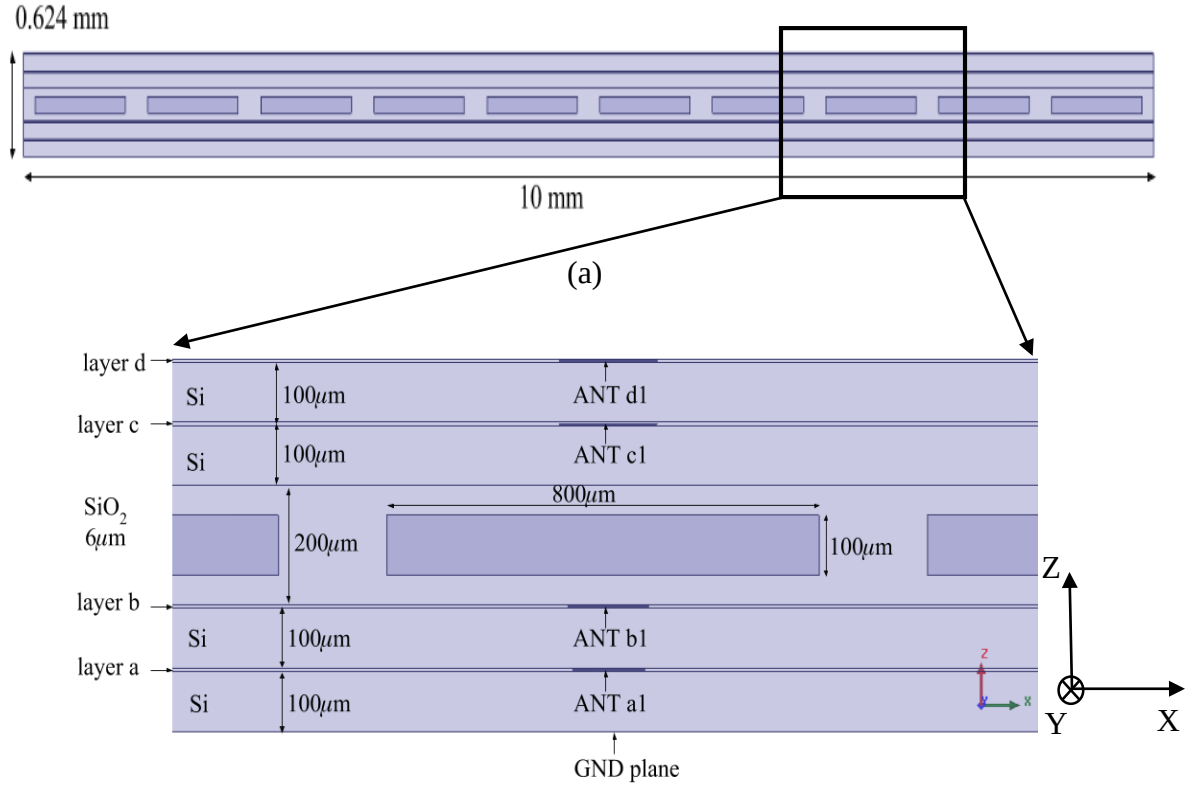


Figure 5-3: (a) Full Side view, (b) close-up view of box in (a), (c) close up view (Not to scale).

Zigzag antennas are placed in the middle of SiO_2 layers. Each layer has different dimension of zigzag antenna, but all antenna in a layer has same dimension. Moreover, each coolants changes the environments and shift the resonance frequency, therefore it is important that antennas should be optimized for each coolant. Below are two different dimensions of antenna used for two different coolants.

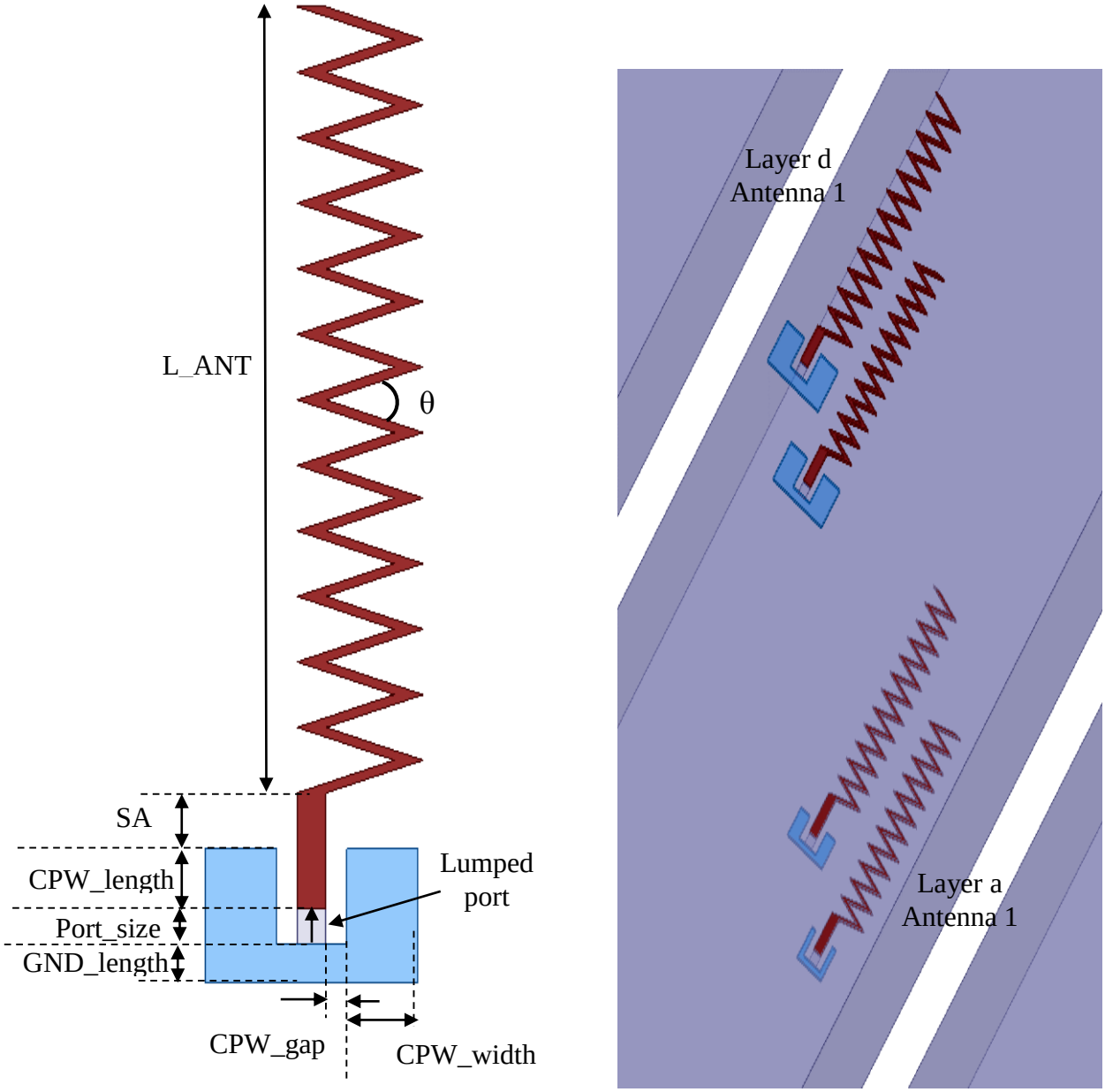


Figure 5-4: Zigzag antenna with variables. 3D view of Zigzag antenna.

Table 4: Dimensions of antenna for coolant #1 (in µm).

CPW_gap = 13.7µm, θ = 30°, Trace/feed thickness is 2 µm, trace width = 5µm, feed width = trace_width/sin(θ/2) = 19.32µm; Port Size = 19.32µm x 19.32µm						
Antenna #	Number of Elements	L_ANT	SA	CPW_length	CPW_width	GND_length
a-1	23	360	40	25	10	10
b-1	24	372	50	20	25	10
c-1	23	345	30	31.41	45	15
d-1	24	420	30	31.41	48	20

Table 5: Dimensions of antenna for coolant #2 (in µm).

CPW_gap = 13.7µm, θ = 30°, Trace/feed thickness is 2 µm, trace width = 5µm, feed width = trace_width/sin(θ/2) = 19.32µm; Port Size = 19.32µm x 19.32µm						
Antenna #	Number of Elements	L_ANT	SA	CPW_length	CPW_width	GND_length
a-1	23	365	40	18	10	10
b-1	24	335	50	20	20	10
c-1	23	350	30	31.41	25	10
d-1	24	425	30	31.41	40	15

5.2. Results

This section is divided into multiple subsections. First, return loss of zigzag antennas for different coolants, since the dimensions of antennas vary only when the coolant is changed. Therefore, no return loss for configuration are specified. Later transmission coefficients are discussed for antenna a-1, b-1, c-1 and d-1 w.r.t all other remaining antennas. Transmission coefficients at 60GHz are tabulated for each antennas according to configuration and coolant. Results are discussed after tabulation.

5.2.1. Return Loss Coolant #1

All antennas are resonating at 60GHz with return loss of less than -18dB.

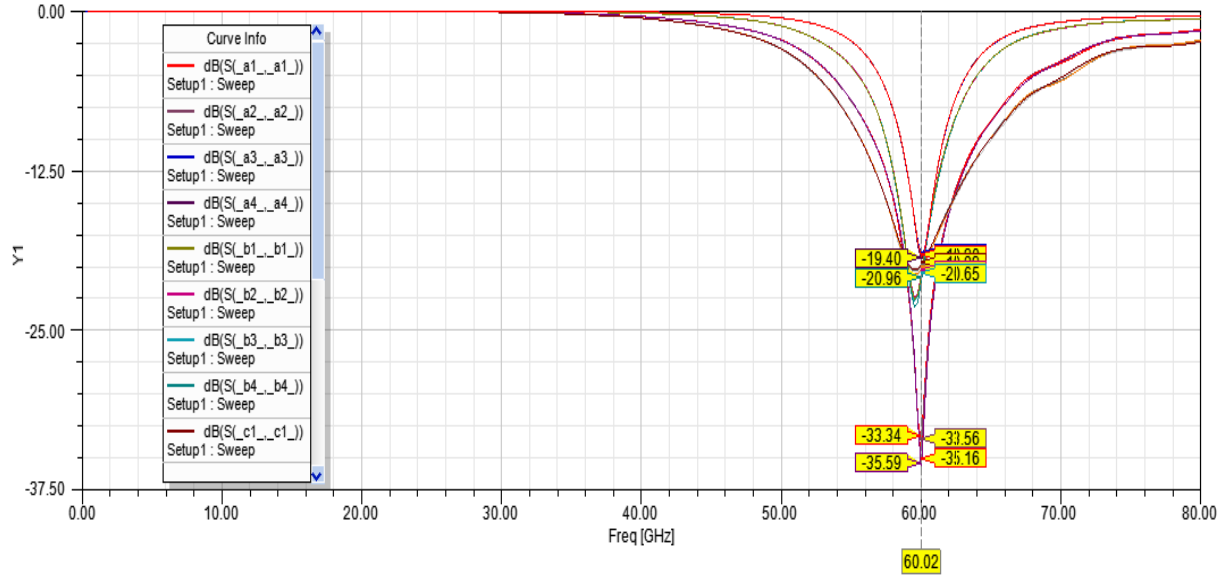


Figure 5-5: Return loss of all 16 antennas in setup with coolant #1.

5.2.2. Return Loss Coolant #2

All antennas are resonating at 60GHz with return loss of less than -15dB.

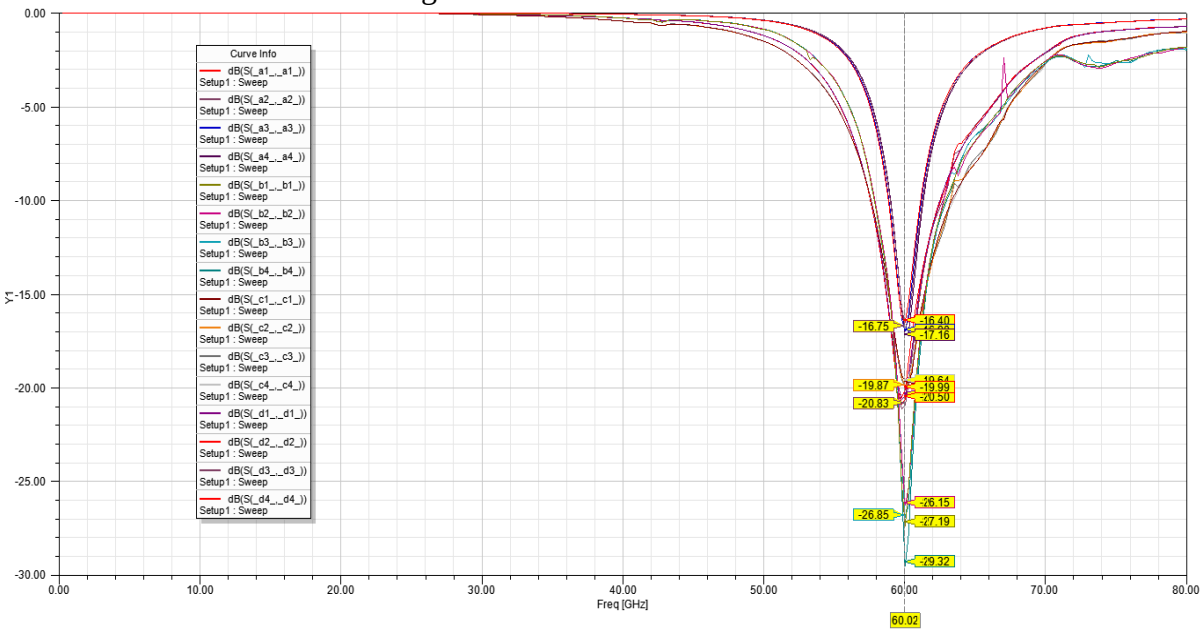


Figure 5-6: Return loss for all 16 antennas in setup with coolant #2.

5.2.3. Transmission Coefficients – Antenna ‘a-1’

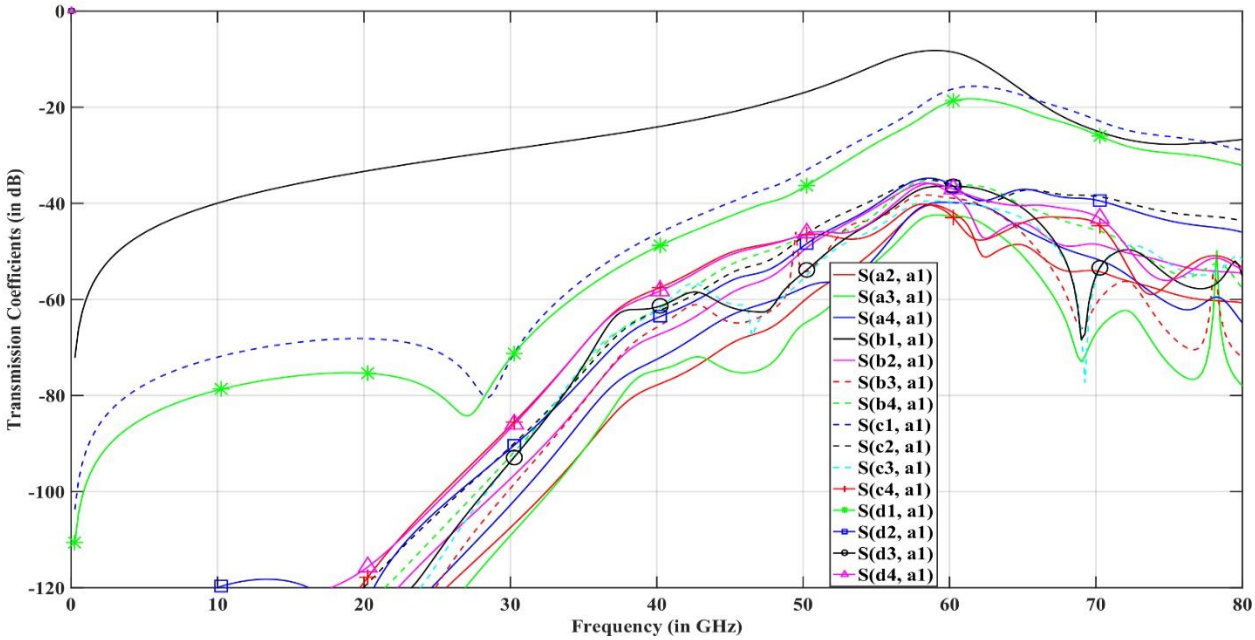


Figure 5-7: Transmission coefficients of antenna ‘a-1’ in conf. #1 coolant #1.

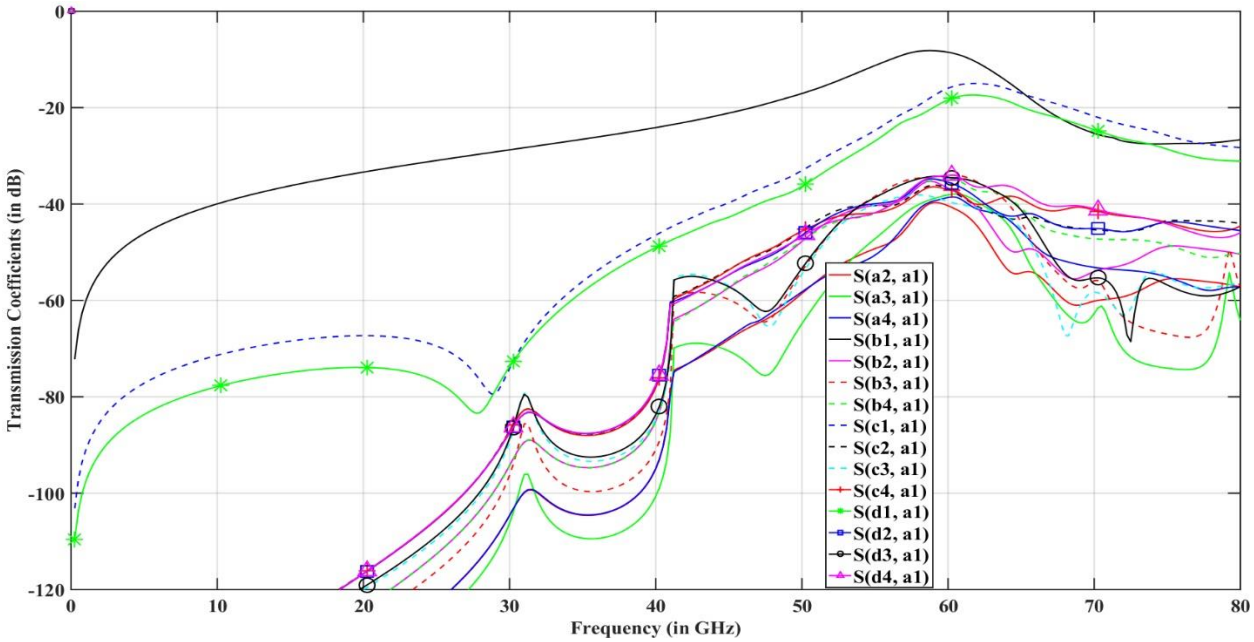


Figure 5-8: Transmission coefficients of antenna ‘a-1’ in conf. #2 coolant #1.

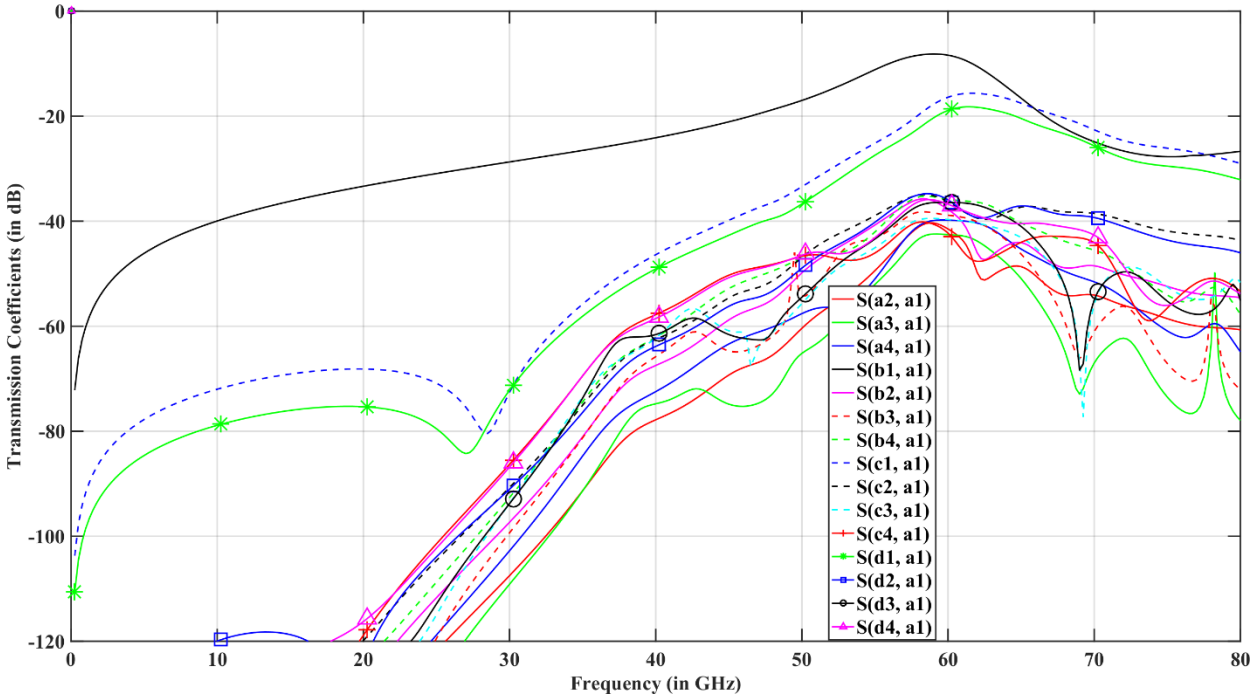


Figure 5-9: Transmission coefficients of antenna ‘a-1’ in conf. #1 coolant #2.

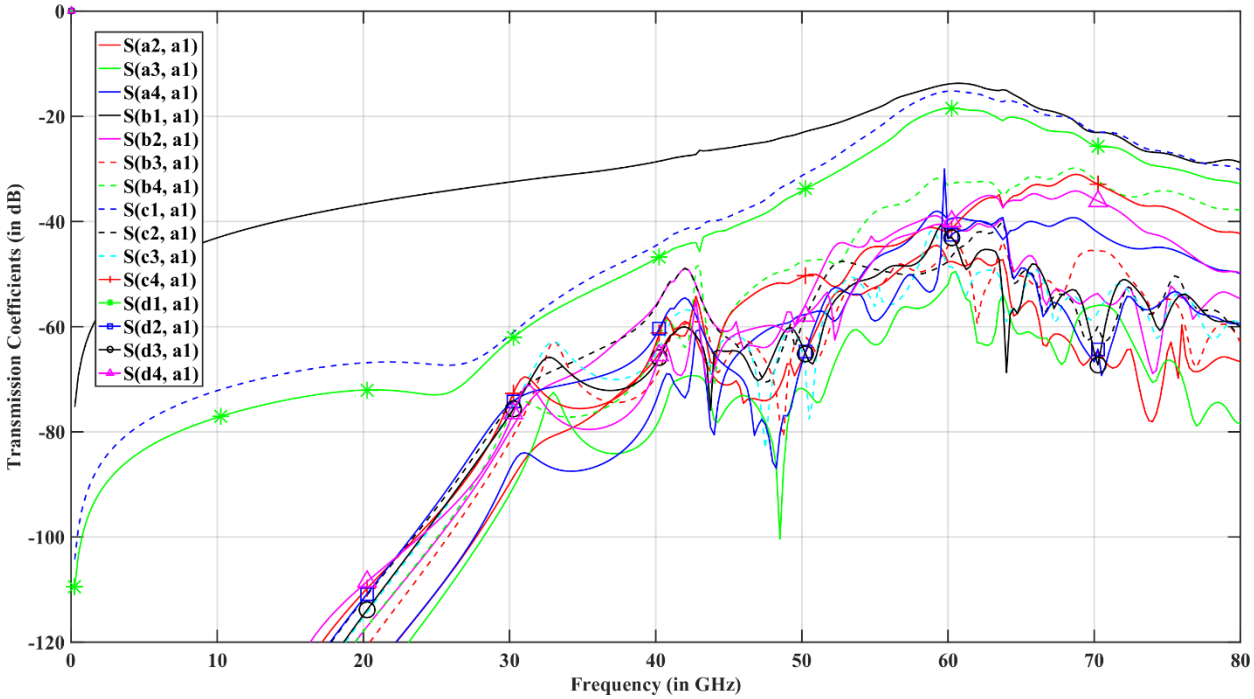


Figure 5-10: Transmission coefficients of antenna ‘a-1’ in conf. #2 coolant #2.

Table 6: Transmission coefficients for antenna a-1.

Trans. Coeff. (in dB)	**Configuration 1 coolant #1**	**Configuration 2 coolant #1**	**Configuration 1 coolant #2**	**Configuration 2 coolant #2**
S(a-2, a-1)	-41.48	-40.35	-48.24	-47.70
S(a-3, a-1)	-42.56	-38.09	-41.53	-51.92
S(a-4, a-1)	-39.79	-38.63	-55.19	-39.70
S(b-1, a-1)	-8.38	-8.50	-13.33	-13.86
S(b-2, a-1)	-37.76	-36.70	-40.83	-41.00
S(b-3, a-1)	-38.85	-34.07	-35.06	-44.67
S(b-4, a-1)	-35.82	-34.85	-46.90	-33.11
S(c-1, a-1)	-16.39	-15.97	-15.32	-15.20
S(c-2, a-1)	-36.35	-36.87	-46.60	-47.63
S(c-3, a-1)	-39.67	-39.47	-52.68	-48.54
S(c-4, a-1)	-42.27	-36.97	-38.80	-42.17
S(d-1, a-1)	-18.90	-18.39	-18.81	-18.44
S(d-2, a-1)	-35.95	-35.47	-40.96	-43.24
S(d-3, a-1)	-36.43	-34.44	-41.96	-43.15
S(d-4, a-1)	-36.76	-34.05	-35.76	-40.76

It can be seen that the transmission coefficients vertically above a-1 such as b-1, c-1 and d-1 (near-field links) are having best transmissions in their layer regardless of coolants and configurations. This is because near-field links “exhibit strongly enhanced propagation characteristics with respect to farfield links” [49]. However, the cross-microchannel transmission of antenna a-1 is degraded in configuration 1 expect only in case of d-4, c-4. For configuration 2, opposite results of just discussed transmission coefficients can be seen in the table. Deionized water with a dielectric constant 78, is a hostile material for antenna. It has degraded the performance of many antennas. However, appropriate orientation may be used to overcome the performance degrading.

5.2.4. Transmission Coefficients – Antenna b-1

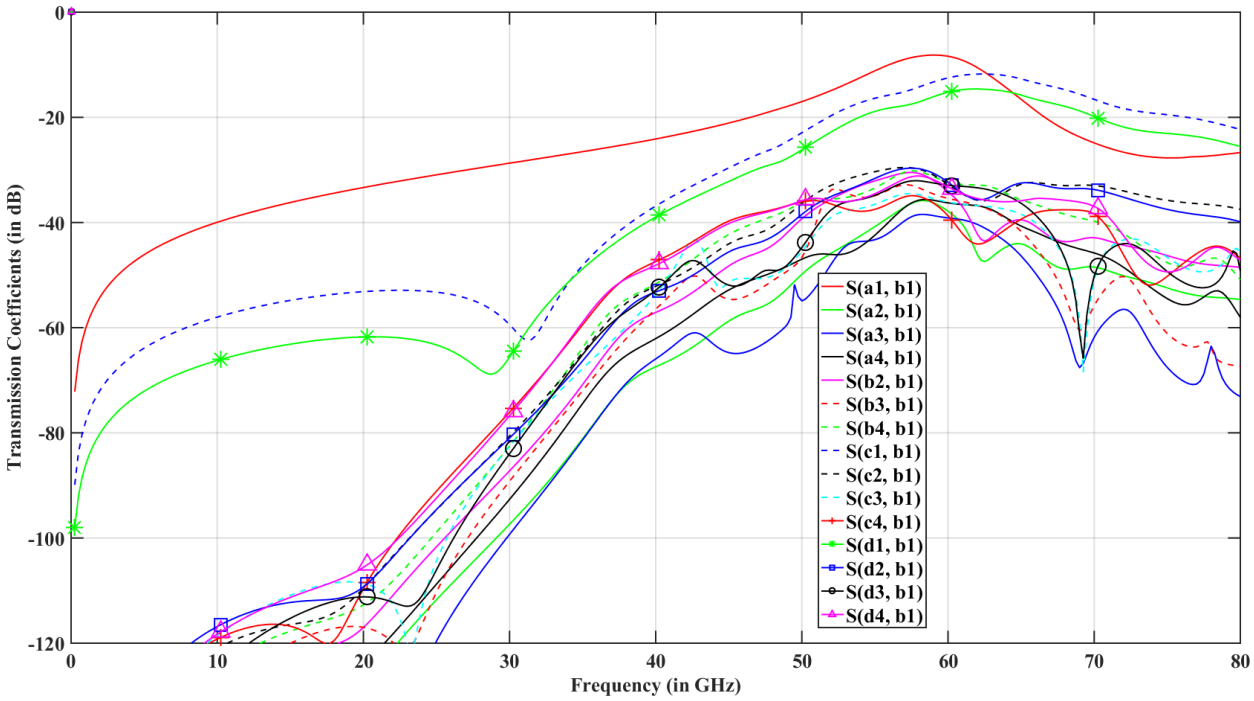


Figure 5-11: Transmission coefficients of antenna ‘b-1’ in conf. #1 coolant #1.

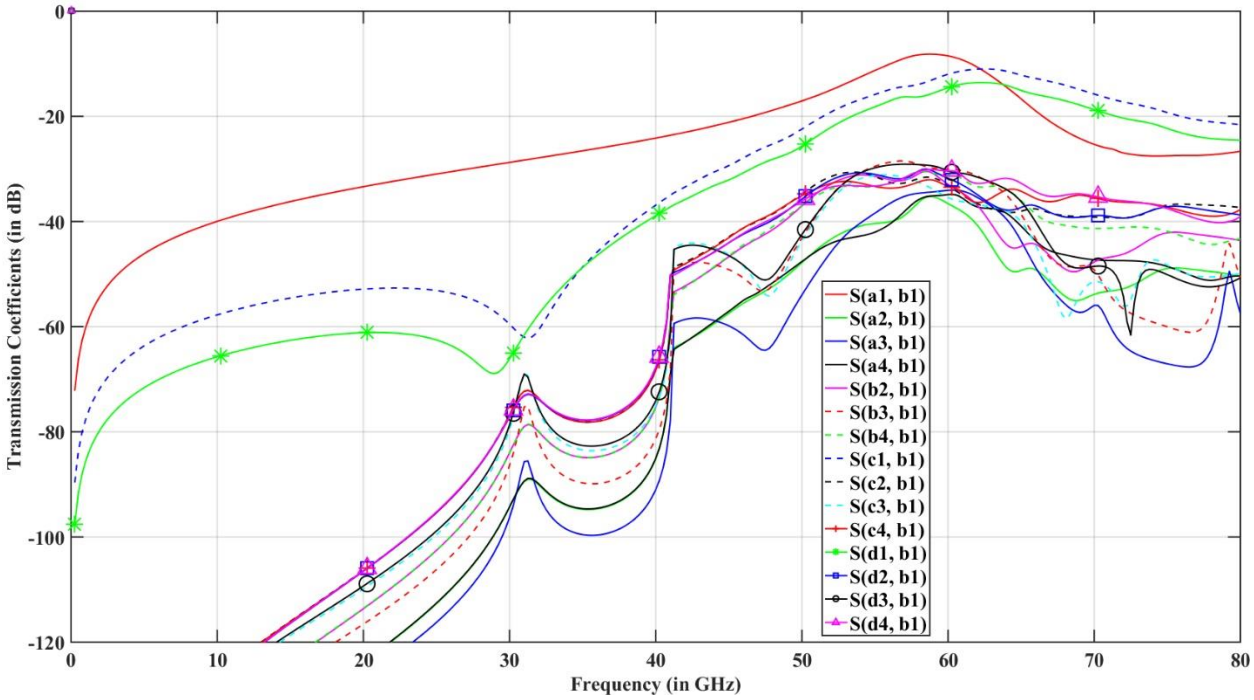


Figure 5-12: Transmission coefficients of antenna ‘b-1’ in conf. #2 coolant #1.

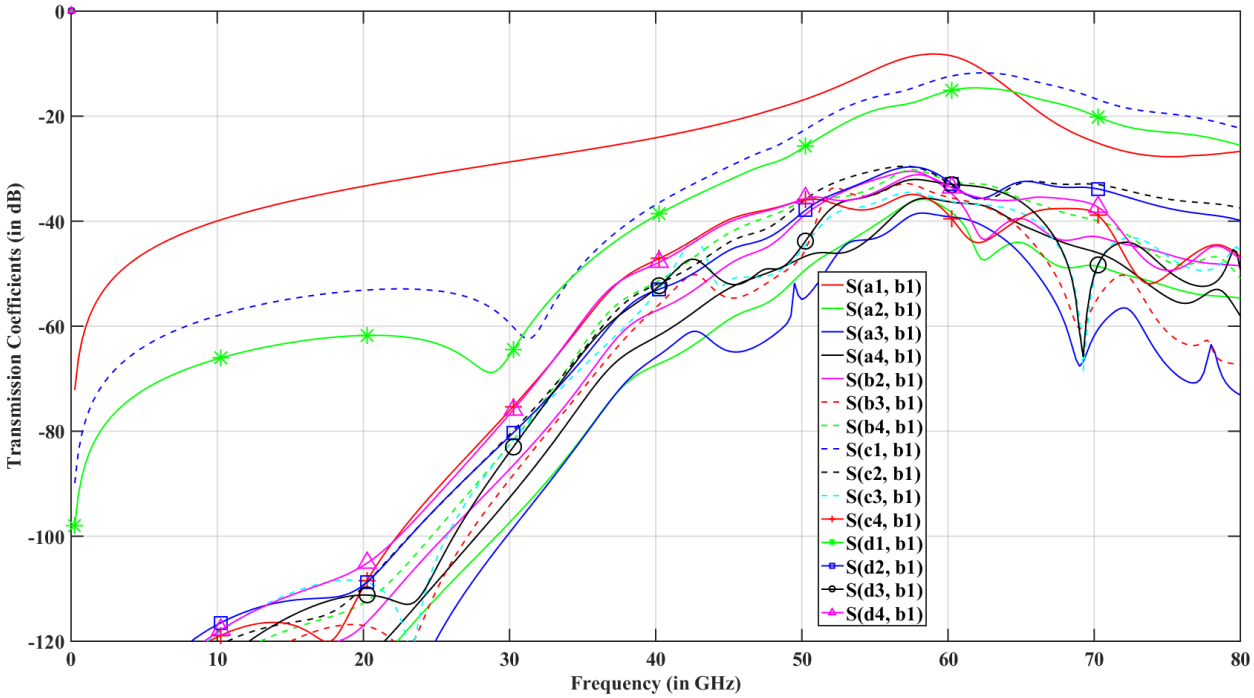


Figure 5-13: Transmission coefficients of antenna ‘b-1’ in conf. #1 coolant #2.

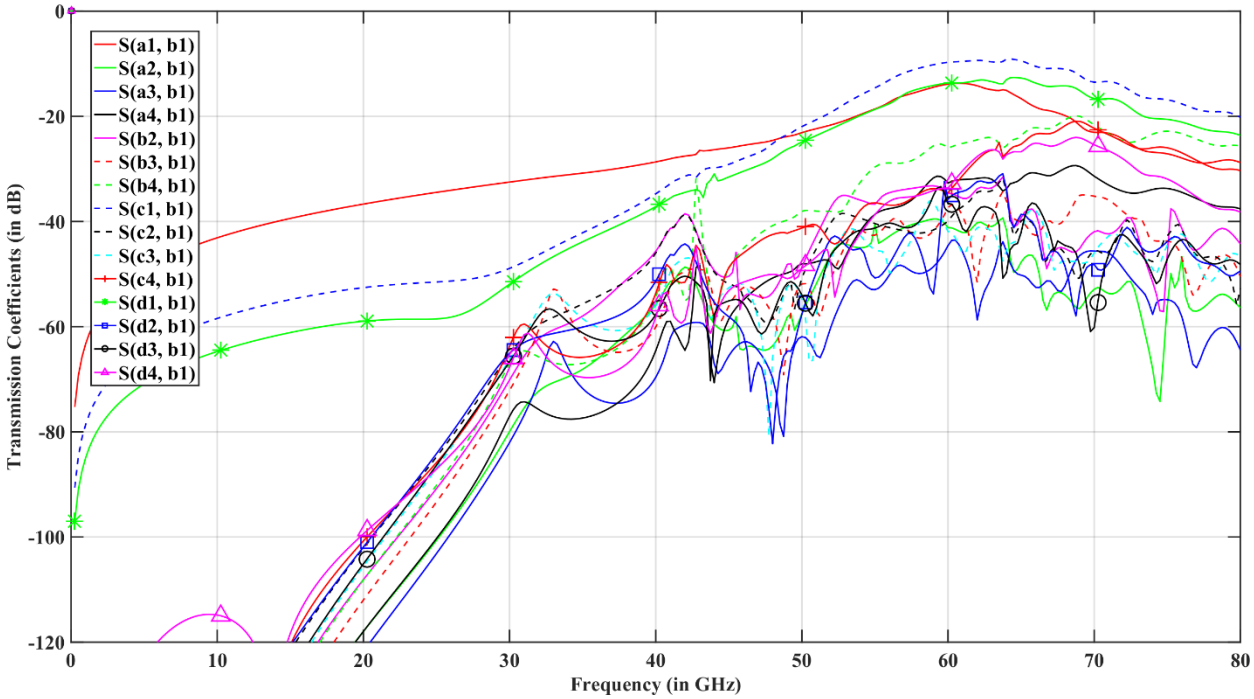


Figure 5-14: Transmission coefficients of antenna ‘b-1’ in conf. #2 coolant #2.

Table 7: Transmission coefficients for antenna b-1.

Trans. Coeff. (in dB)	**Configuration 1 coolant#1**	**Configuration 2 coolant#1**	**Configuration 1 coolant#2**	**Configuration 2 coolant#2**
S(a-1, b-1)	-8.38	-8.50	-13.33	-13.86
S(a-2, b-1)	-37.86	-36.58	-41.76	-41.16
S(a-3, b-1)	-39.12	-34.06	-34.46	-44.56
S(a-4, b-1)	-36.26	-34.88	-51.34	-32.68
S(b-2, b-1)	-34.13	-32.93	-34.25	-34.60
S(b-3, b-1)	-35.41	-30.03	-27.95	-37.33
S(b-4, b-1)	-32.30	-31.10	-41.86	-26.08
S(c-1, b-1)	-12.49	-11.93	-9.87	-9.71
S(c-2, b-1)	-32.74	-33.13	-40.03	-39.95
S(c-3, b-1)	-36.12	-35.45	-45.15	-41.90
S(c-4, b-1)	-38.72	-33.32	-31.64	-34.51
S(d-1, b-1)	-15.21	-14.56	-13.97	-13.63
S(d-2, b-1)	-32.34	-31.76	-34.65	-35.77
S(d-3, b-1)	-32.90	-30.40	-34.81	-36.58
S(d-4, b-1)	-33.23	-30.37	-28.85	-33.64

Cross-microchannel transmissions like between antenna b-1 and antenna d-1 or c-1 improved when water is used. However, cross-microchannel transmissions are mostly degraded for configuration 1. Transmission between b-1 and a-1 is degraded when coolant is changed to water. The transmission coefficients in vertically aligned to b-1 remained changed despite change in configuration. It should be noted that the transmission between antenna b-1 and d-4/ c-4 is improved when water is used as coolant in configuration 1, this may be because the microchannel is above the antenna b-1, EM radiation is affected by water (very high permittivity).

5.2.5. Transmission Coefficients – Antenna c-1

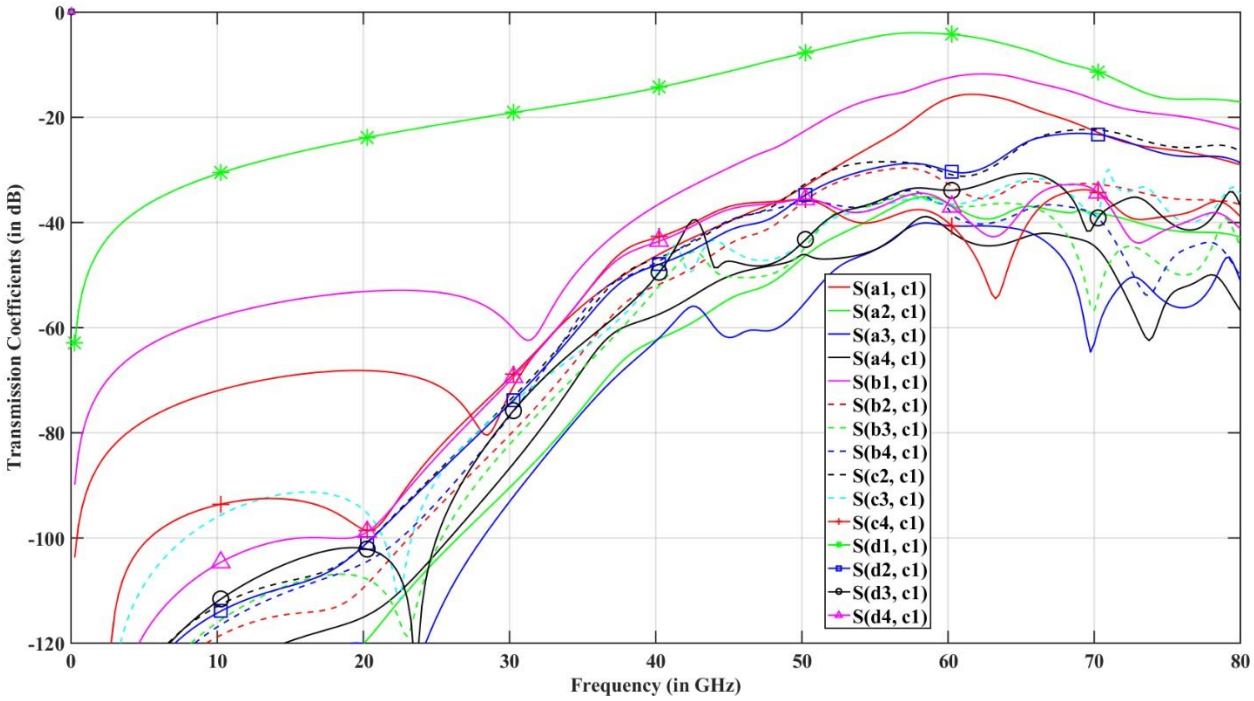


Figure 5-15: Transmission coefficients of antenna ‘c-1’ in conf. #1 coolant #1.

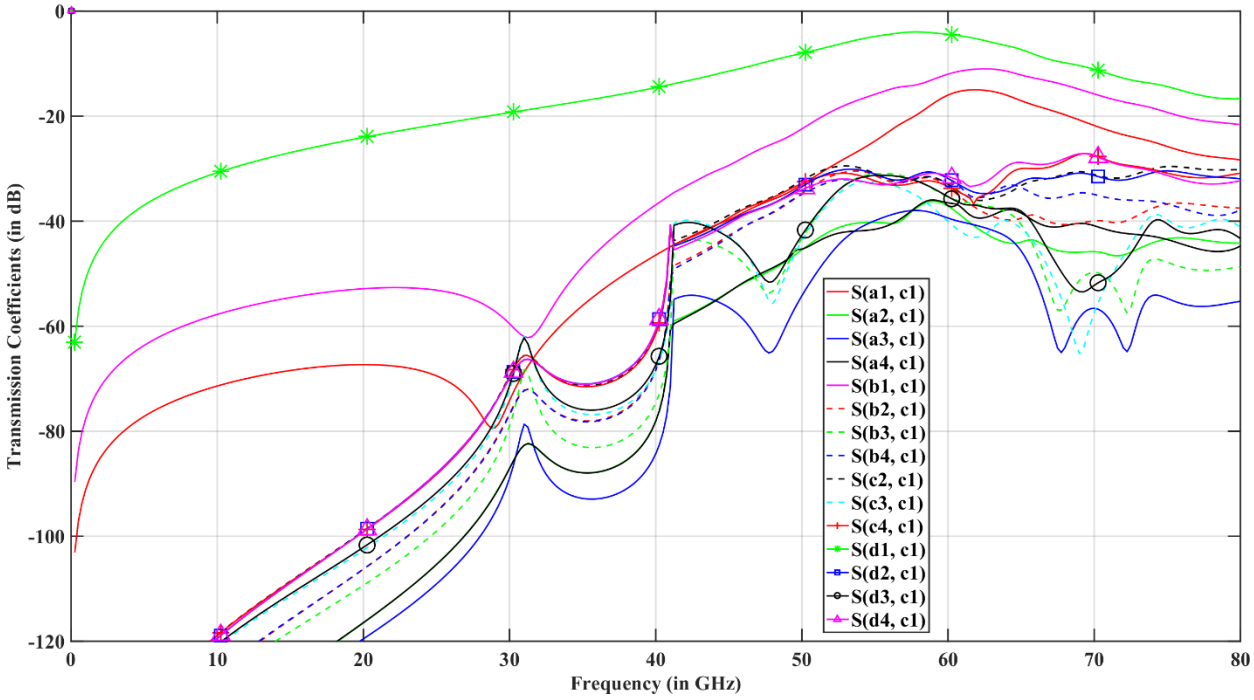


Figure 5-16: Transmission coefficients of antenna ‘c-1’ in conf #2 coolant #1.

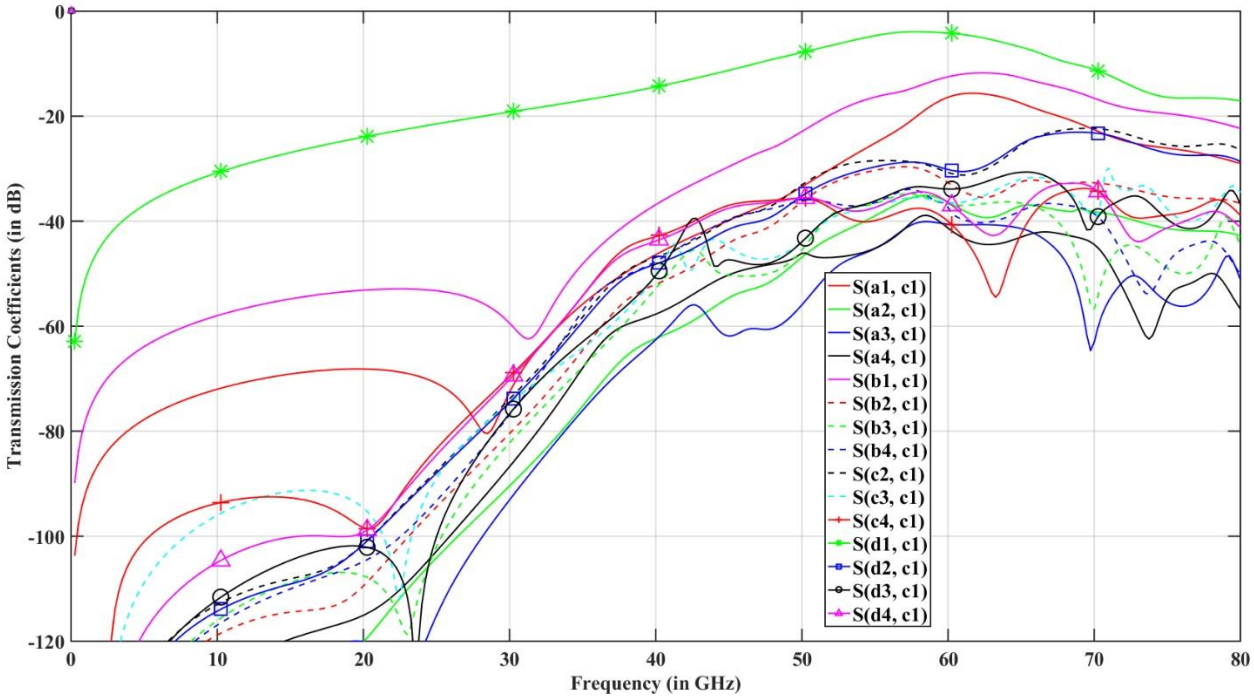


Figure 5-17: Transmission coefficients of antenna ‘c-1’ in conf. #1 coolant #2.

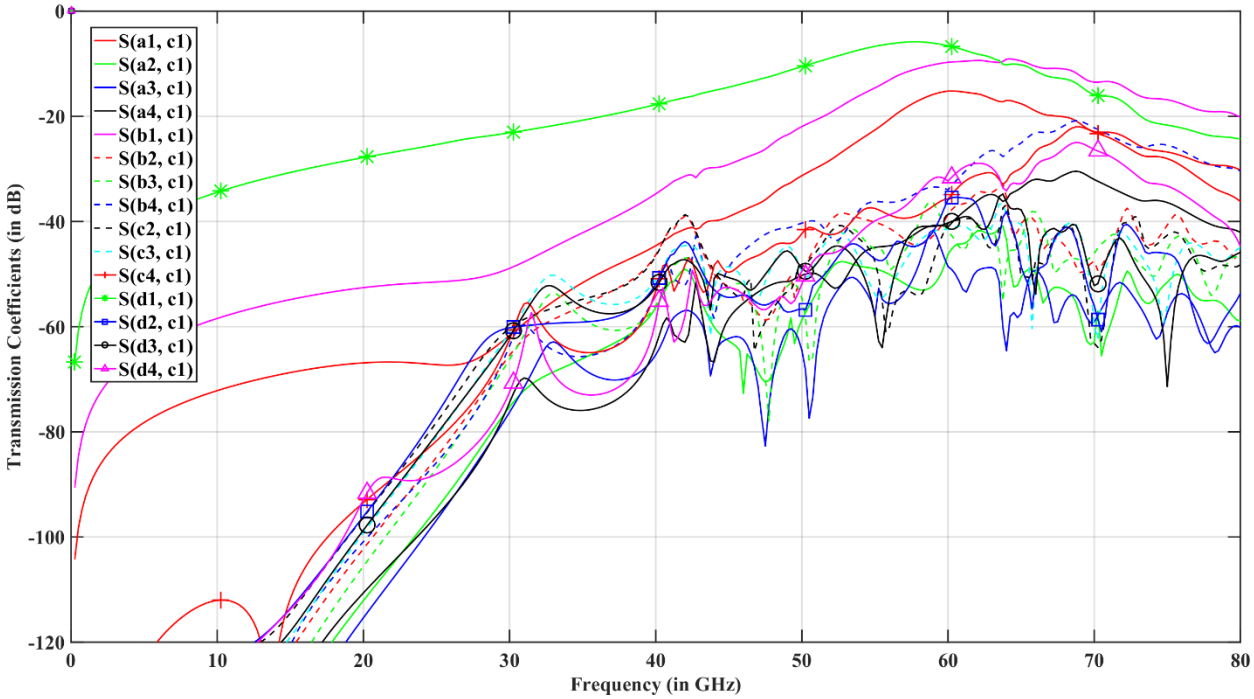


Figure 5-18: Transmission coefficients of antenna ‘c-1’ in conf. #2 coolant #2.

Table 8: Transmission coefficients for antenna c-1.

Trans. Coeff. (in dB)	**Configuration 1 coolant#1**	**Configuration 2 coolant#1**	**Configuration 1 coolant#2**	**Configuration 2 coolant#2**
S(a-1, c-1)	-16.39	-15.97	-15.32	-15.20
S(a-2, c-1)	-36.36	-37.12	-48.23	-46.22
S(a-3, c-1)	-40.55	-39.40	-55.13	-48.57
S(a-4, c-1)	-41.31	-36.51	-38.43	-41.04
S(b-1, c-1)	-12.49	-11.99	-9.87	-9.71
S(b-2, c-1)	-32.66	-33.50	-41.00	-38.64
S(b-3, c-1)	-36.77	-35.38	-52.88	-42.02
S(b-4, c-1)	-37.39	-32.77	-32.03	-33.95
S(c-2, c-1)	-30.72	-32.96	-47.65	-40.34
S(c-3, c-1)	-36.44	-40.03	-44.62	-41.52
S(c-4, c-1)	-40.01	-33.40	-34.98	-35.71
S(d-1, c-1)	-4.17	-4.41	-6.42	-6.58
S(d-2, c-1)	-30.16	-31.87	-42.37	-35.82
S(d-3, c-1)	-33.88	-35.33	-43.57	-40.26
S(d-4, c-1)	-36.43	-31.46	-37.52	-32.31

As seen above, the best transmission of antenna c-1 is in vertical direction that is a-1, d-1 and b-1 as mentioned above because of near-field transmission [49]. It should be noted that the cross microchannel transmission in vertical direction improved for b1, and remained unchanged for antenna a-1. For antennas in layer ‘a’ except antenna a-1, their transmission with antenna c-1 is much affected by the coolant 2. The performance has degraded by more than 7dB. Moreover, the antenna c-1 transmission performance degraded in its layer c and d when coolant is changed to deionized water. The transmission between c-1 and c-2 or c-3 has gone down by 10dB or more in configuration 1.

5.2.6. Transmission Coefficients – Antenna d-1

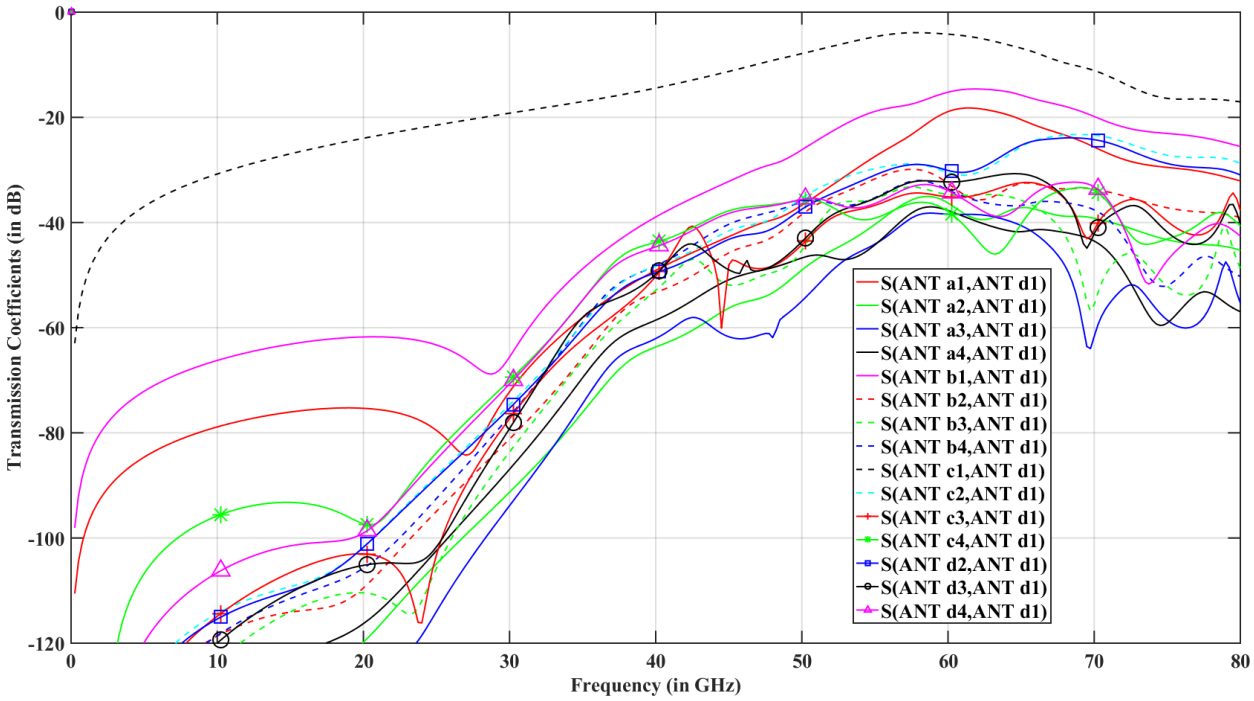


Figure 5-19: Transmission coefficients of antenna ‘d-1’ in conf. #1 coolant #1.

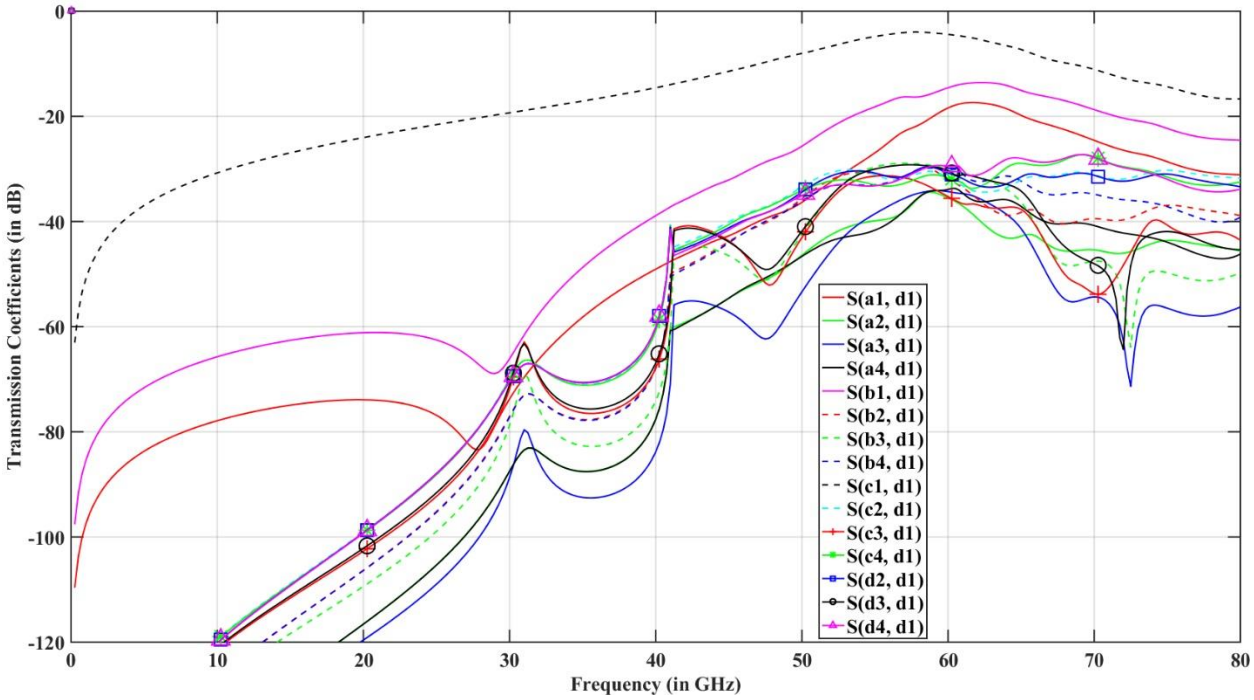


Figure 5-20: Transmission coefficients of antenna ‘d-1’ in conf. #2 coolant #1.

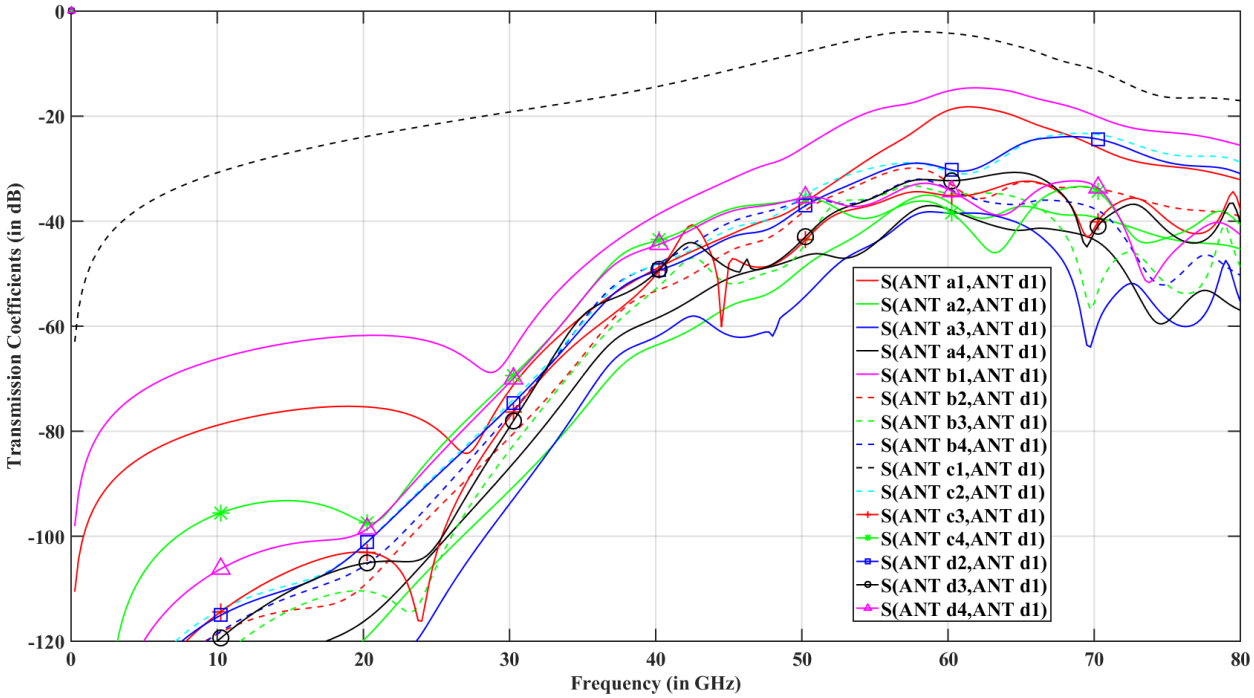


Figure 5-21: Transmission coefficients of antenna ‘d-1’ in conf. #1 coolant #2.

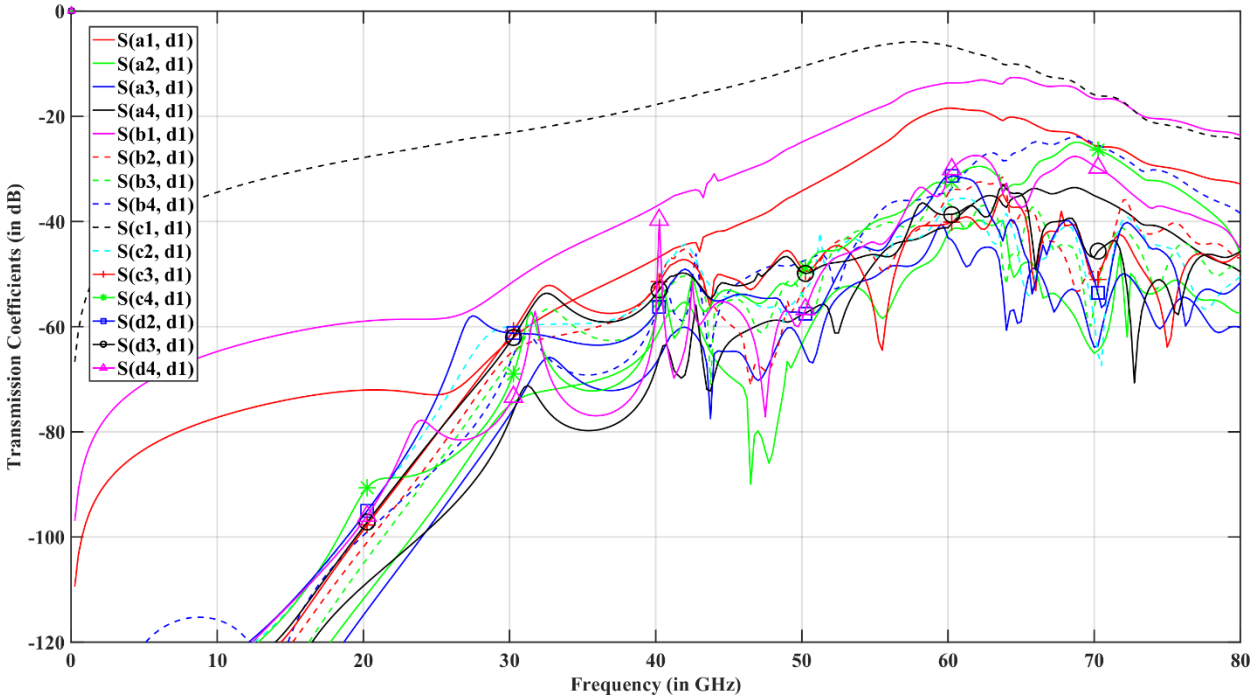


Figure 5-22: Transmission coefficients of antenna ‘d-1’ in conf. #2 coolant #2.

Table 9: Transmission coefficients for antenna d-1.

Trans. Coeff (in dB)	**Configuration 1 coolant#1**	**Configuration 2 coolant#1**	**Configuration 1 coolant#2**	**Configuration 2 coolant#2**
S(a-1, d-1)	-18.90	-18.39	-18.81	-18.44
S(a-2, d-1)	-36.28	-35.50	-44.78	-42.09
S(a-3, d-1)	-38.43	-34.30	-41.01	-43.10
S(a-4, d-1)	-37.71	-33.90	-37.63	-41.18
S(b-1, d-1)	-15.21	-14.56	-13.97	-13.63
S(b-2, d-1)	-32.58	-31.91	-37.87	-34.65
S(b-3, d-1)	-34.67	-30.26	-34.83	-36.62
S(b-4, d-1)	-33.79	-30.16	-30.97	-34.56
S(c-1, d-1)	-4.17	-4.41	-6.42	-6.58
S(c-2, d-1)	-30.50	-31.65	-44.97	-36.17
S(c-3, d-1)	-35.13	-35.26	-48.13	-40.38
S(c-4, d-1)	-37.89	-31.67	-40.55	-33.21
S(d-2, d-1)	-30.09	-30.76	-38.88	-31.64
S(d-3, d-1)	-32.28	-30.32	-45.53	-38.60
S(d-4, d-1)	-33.92	-29.48	-41.37	-30.75

It can be seen that the transmission in vertical direction towards antennas a-1, b-1 is unchanged despite the coolant or configuration, though c-1 is affected little by coolant. This is because near-field links “exhibit strongly enhanced propagation characteristics with respect to farfield links” [49]. Due to coolant 2, deionized water, the transmission between antenna d-1 and layer c antennas is affected by more than 5dB. Across the channel, transmission between antenna a-4 to d-1 remained unchanged for configuration 1 and changed for configuration 2 when coolant is changed. In layer d, the transmission coefficients have improved for antenna d-3 and d-4.

Conclusions

Zigzag antennas are designed and analyzed using ANSYS HFSS. Antennas such as linear monopole, zigzag monopole antennas and loop antennas are designed and simulated to work at 60GHz. It was seen that the radiation pattern of all aforementioned antennas in free space is similar to the wire dipole. These antennas are also simulated with different setups on silicon chip (with or without ground plane at the bottom). Antennas on silicon chip without ground plane were found to have omnidirectional radiation pattern. However, antennas in silicon chip with ground were found to have directional pattern with radiation directed in vertical direction away from ground. Ground plane has reflected the radiation.

Zigzag antennas are analyzed for multichip multicore systems using ANSYS HFSS. Different configurations and orientations are analyzed to find optimum transmission. Zigzag antennas are resonating at 60GHz with return loss less than -25dB. Transmission coefficients are plotted. Transmission coefficients vary from -30 to -50dB. It can be seen that the transmission coefficients for most of the antennas has improved when the orientation has been changed. Moreover, it was found that changing the orientation can improve the transmission coefficients. This also implies that the radiation pattern of antennas becomes directional when placed on a large silicon wafer with ground plane at the bottom.

Moreover, Zigzag antennas are designed on silicon wafer to work at 30GHz using ANSYS HFSS. Zigzag antennas are fabricated in RIT SMFL, later antennas are tested using Cascade probe station and PNA 8363B. The antennas are working between 20GHz to 25GHz with return loss of around -10dB. The average transmission coefficients vary from -45dB to -50dB at resonating frequency for various antenna pairs. Though, the results are shifted from design frequency, the

results are satisfactory. The change in frequency can be adjusted by manufacturing variation, that is, reducing the size of antennas. Furthermore, transmission in low frequency range is under investigation.

Antennas as wireless interconnects are analyzed for 3D IC. All wireless interconnects are resonating at 60GHz. Transmission coefficients were analyzed. It was found that the antennas vertically aligned (in near-field region) have best transmission coefficients. This is because near-field links "exhibit strongly enhanced propagation characteristics with respect to farfield links" [49]. It was hard to optimize for the layer near to the ground. The reverse image current generated by the ground plane reduces the performance of the antennas. PEC boundary or ground plane is considered in simulation as a surface of metal heat sink. As seen in presented work that PEC boundary affects the antenna properties like radiation pattern, input impedance, et al. Using Electromagnetic Bandgap (EBG) structures [50] may help mitigate the PEC boundary effect (heat sink).

Future Work

Wireless systems will also generate heat due to lossy nature of silicon. An investigation is required to find how the radiation from antennas affect the silicon wafer. It is required for 3D IC since; it is already limits by the heat dissipated by the metal interconnect. It is required to do a performance evaluation of wireless interconnects in terms of heat generation. This analysis can be performed using ANSYS HFSS integrated with ANSYS Icepack, which is a package distributed with ANSYS Mechanical.

It is suggested that the EBG structure should replace the PEC boundary. EBG structures provide better antenna performance than PEC boundary when used near to an antenna. Moreover, the EBG structures can be used to separate heat sink (ground plane) from the antenna system. Further investigations are required to cancel the effect of heat sink using EBG structure.

Future work requires analysis of near field of present antenna in 3D IC, even designing an efficient proper near field antenna. Moreover, the antenna implemented as wireless interconnect in this thesis is narrowband. To take the advantage of full unlicensed spectrum (57-64GHz), implementation of a broadband antenna is suggested.

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