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Editorial

These proceedings contain papers presented at the 24th Annual Microelectronic Engineering Conference held at the Rochester Institute of Technology (RIT) on May 12 through 14, 2008 by senior undergraduate students of Microelectronic Engineering of RIT. The students graduating with BS degree in Microelectronic Engineering are required to take a two-course sequence of capstone design courses, 0305-681 and 0305-691 entitled Senior Design Project I and II in their fifth year. The first course consists of submission of a research proposal, related to the field of semiconductor devices and processing, by each student. Following the approval of the proposal, the students carry out their projects through the ten-week spring quarter. Toward the end of the spring quarter, the students are required to present their work at the Microelectronic Engineering Conference held at RIT annually in the month of May and publish in this Journal of Microelectronic Research.

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# The Journal of Microelectronic Research

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<table>
<thead>
<tr>
<th>Title</th>
<th>Student</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Investigation of microplasma cells fabricated on silicon wafer</td>
<td>Koffi Abalo-Akuvi</td>
<td>1</td>
</tr>
<tr>
<td>Theoretical Study and Device Modeling of III-V Nanostructured Photovoltaics</td>
<td>Ryan Aguinaldo</td>
<td>6</td>
</tr>
<tr>
<td>Developing an Empirical Model for Tunable Porosity in Porous Nanocrystalline Silicon Membranes</td>
<td>Jon-Paul S. DesOrmeaux</td>
<td>13</td>
</tr>
<tr>
<td>Deep Submicron Pattern Formation for Selective Epitaxial Growth of III-V Semiconductors</td>
<td>Kenny Fourspring</td>
<td>17</td>
</tr>
<tr>
<td>Fabrication of Metal-High-κ Capacitors on Germanium</td>
<td>Rahul Gupta</td>
<td>22</td>
</tr>
<tr>
<td>Fabrication of an Esaki Tunneling Diode by Proximity Rapid thermal diffusion</td>
<td>Sankar Krishnan</td>
<td>26</td>
</tr>
<tr>
<td>Double Patterning Technique Using an Aluminum Hardmask</td>
<td>Brian Lindenau</td>
<td>31</td>
</tr>
<tr>
<td>Process Development for the Fabrication of a Double-Sided Photodiode</td>
<td>Kimberly Manser</td>
<td>37</td>
</tr>
<tr>
<td>Three Dimensional Nanochannel Formation by Reflective Interference Lithography</td>
<td>Michael Many</td>
<td>43</td>
</tr>
<tr>
<td>Germanium Esaki Diodes by N-type In-Situ Doping</td>
<td>Amy Miller</td>
<td>48</td>
</tr>
<tr>
<td>Active Matrix Polymer Cholesteric Liquid Crystal Display</td>
<td>Graham Mhyre</td>
<td>51</td>
</tr>
</tbody>
</table>
Integrated Thin Film Crystalline Silicon Photoactive Components

Reclaimed Silicon Solar Cells

Surface Micro-Machined Capacitive Pressure Sensor

Thermal SiO2 Growth Rate Enhancement at Low Temperatures using an NF3 Additive

Fabrication of Thermally Actuated Micromirror using CMOS Compatible Surface MEMs Process with XeF2 Release etch

Process Characterization for Integration of Esaki Diodes into Aspect Ratio Trapping Material

Biomedical Lance Ion Sensitive System

Characterization of P-N Junctions for Variation in Dose and Annealing Temperatures

Fabrication of aligned metallic structures based on block copolymer lithography

Electrolysis-Bubble-Actuated Micropump

Development of a Linear Source, Atmospheric Pressure RF Glow Discharge Plasma

Optical Ring Resonator and Other Photonic Devices

Unbalanced Mach-Zehnder Electro-Optic Modulator and Waveguide Components
Investigation of microplasma cells fabricated on silicon wafer

Koffi Abalo-Akuvi, Microelectronic Engineering, Rochester Institute of Technology

Abstract—The objective of this project was to investigate the possibility of producing an array of microplasmas, having aluminum and silicon electrodes, and oxide as a dielectric with cavity size as large as 30x30 μm². One of the potential applications among many was to use such device as a photodector. A new class of photodetectors, hybrid semiconductor-microplasma devices, to exhibit photoresponsivities in the visible and near infrared that are more than an order of magnitude larger than those typical of semiconductor avalanche photodiodes [1]. After fabrication processing, the route causes of failure were determined. Processing problems were diagnosed and process evaluation test structures characterized using optical microscope, and scanning electron microscopy (SEM). Oxide insulation between the metal layers (Aluminum) was tested using a multimeter. Continuity tests revealed a short between the metal electrodes. The application of SEM in this failure analysis of a finished device shows aluminum stringers left in the cavities. This was the confirmation of a potential short previously diagnosed with the multimeter test.

Index Terms—Microcavity plasma device (MPD), microplasma, plasma, photodetector.

I. INTRODUCTION

Techniques developed originally for semiconductor processing, offer exciting opportunity to fabricate devices capable of producing weakly ionized microplasmas [1]. The reduction of the plasma typical dimensions down to the micrometer range or less is expected to bring previously unobserved physical phenomena to the fore as well as to offer new device applications [2]. Research activities along this direction have been increasing on a worldwide scale especially in the US and Japan since the late 1990s [1,2]. These researches are pursuing two main goals: (1) to investigate the physics of weakly ionized plasmas confined to sub-millimeter dimensions and (2) to develop materials and structure platforms that allow microplasma to be integrated with electronic and photonic components, as well as to be mass produced economically. In this paper, microplasmas design, fabrication and testing was investigating.

II. THEORY

A. What is plasma?

Plasma is often referred to a fourth state of matter in addition to solid, liquid, and gas. In plasmas the degree of ionization is high and therefore high densities of ions and electrons are found. Plasma can conduct electricity and interact strongly with electric and magnetic fields.

Specifically, plasma is ionized gas. That is, gas that has been given energy by being stripped of electrons. Such ionized gas is the most abundant observable form of matter in the universe, being a main ingredient in stars and nebula. It is also what the main part of a flat panel displays called "plasmas". Why? Because when you apply an electromagnetic field to the pixel, plasma glows, making for a high contrast, vibrant TV screen, computer monitor, or digital sign [3].

B. Generation of Microplasma

1) Generation method:

To create plasma, energy must be supplied to gas. This energy can be provided in various ways, including heat, or electromagnetic (EM) field.

There are many ways to generate plasmas of small scales. Plasma generation methods are classified on the basis of the frequency of the power sources; the range spreads from DC to GHz. In DC operation, the most popularly used design is the hollow cathode (HC) type, which has been studied by the Schoenbach’s group recently from miniaturized structures and integrated assemblies [7,8].

In the pulse discharge mode, the dielectric barrier discharge (DBD) configuration is often used, in which both or at least one of the electrodes is covered with an insulating material, as shown in Fig. 1 [1]. An example of this DBD scheme is seen in the unit cell of current commercial plasma display panel (PDP) show in Fig. 1 as a coplanar type (a) [10]. The structure (b) is called the counter-electrode type, which was used in the earlier phase of the PDP research. Recently, its modified structure of a horizontal type (b') has become manufacturable [11]. The structure (c) can be called a coaxial type, in which the discharge is sustained between the upper and lower electrode [12], while the type (c') is a version with an auxiliary mesh electrode. The type (b') and (c) or (c') may be preferable for material processing purposes since the source gas be fed vertically to the electrode plane through the hole.
2) Media for microplasma

High-pressure gases are mostly used as media for the generation of microplasma, where the design of the gas flow is an important issue for realizing the nonequilibrium state under controlled conditions. The additional gas flow driven by the ion drag force flowing toward the cathode may have a large influence as the operating pressure increases [1].

C. Characteristics of Microplasma

In general, plasmas have reactive, radioactive, and conductive properties. When these properties are combined with the characteristics of microplasma such as plasmas (electrons) density $n_e$, residence time of electrons $\tau_e$ and temperature, there are a variety of possibilities for the application of microplasmas.

III. SILICON MICROPLASMA PHOTODETECTORS

A. Mask design

![Figure 2: Layout of oxide mask (lithography 1)](image)

The masks design specifications are summarized in Table 1. There were two masks, oxide and metal. The only difference between the mask was the size of the dark boxes, 25x25$\mu$m$^2$ for oxide (Figure 2) and metal 30x30$\mu$m$^2$.

<table>
<thead>
<tr>
<th>Cell Layout size</th>
<th>9980$\mu$m</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plate size</td>
<td>5&quot;x5&quot;x0.0090&quot;</td>
</tr>
<tr>
<td>Array</td>
<td>Array with 10 rows and 10 columns</td>
</tr>
<tr>
<td>Field type</td>
<td>Dark field</td>
</tr>
<tr>
<td>Orientation</td>
<td>Mirror 90</td>
</tr>
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</table>

Table 1: Mask Specifications

<table>
<thead>
<tr>
<th>#</th>
<th>STEP NAME</th>
<th>Area</th>
<th>RIT Tools</th>
<th>RECIPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Scribe</td>
<td>Metrology</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ResMap</td>
<td>Metrology</td>
<td>CDE Res Map</td>
<td>4 inch Rs 25pt</td>
</tr>
<tr>
<td>3</td>
<td>RCA Clean (#1)</td>
<td>Wet</td>
<td>Wet Bench</td>
<td>SMFL Standard process</td>
</tr>
<tr>
<td>4</td>
<td>Oxide Growth (Dielectric)</td>
<td>Thermal</td>
<td>BRUCE 01 TUBE 01</td>
<td>Recipe: 440 1100C Wet Ox - 35hrs soak time</td>
</tr>
<tr>
<td>5</td>
<td>Cavity level 1: Litho</td>
<td>Sus MA 150 Aligner</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Oxide Etch</td>
<td>Wet</td>
<td>BOE 5:2:1</td>
<td>40 min</td>
</tr>
<tr>
<td>7</td>
<td>Resist Strip</td>
<td>Dry Etch</td>
<td>Branson L3200 Asher</td>
<td>Branson Asher in normal or hard ash</td>
</tr>
<tr>
<td>8</td>
<td>Cavity Etch</td>
<td>Wet Etch</td>
<td>Dr. Fuller: 20 wt% KOH</td>
<td>Dr. Fuller KOH set up: 75C, rate at 30 $\mu$m/hr (it would take about 15 min to get down to 10 $\mu$m deep)</td>
</tr>
<tr>
<td>9</td>
<td>Decontamination</td>
<td>Wet</td>
<td>Need to Contact Sean</td>
<td></td>
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<tr>
<td>10</td>
<td>Al Deposition(Front)</td>
<td>Thermal</td>
<td>CVC601 - Sputter Al</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Al Deposition(Back)</td>
<td>Thermal</td>
<td>CVC601 - Sputter Al</td>
<td></td>
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<tr>
<td>12</td>
<td>Litho level 2: (Metal)</td>
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<td>Sus MA 150 Aligner</td>
<td>SVG track Standard Coat/Develop Recipe</td>
</tr>
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<td>LAM 4600 Metal Etch</td>
<td>LAM 4600</td>
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<tr>
<td>14</td>
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<td>Branson L3200 Asher</td>
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<td>Sinter</td>
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<td>425C for 20 minutes in H2/N2</td>
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<td>16</td>
<td>Dicing</td>
<td>Packaging</td>
<td>KS780 Dicing Saw</td>
<td></td>
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<tr>
<td>17</td>
<td>Test</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Process Details

The process details are tabularized in Table 2.
Figure 3 shows SEM picture of a segment of the microplasma array. The device pitch for this array is 50µm with a 30x30µm² opening (Oxide and Al, without Si Etch).

IV. RESULTS AND ANALYSIS

Oxide insulation between the metal layers (Aluminum) was tested using a multimeter. Continuity tests revealed a short between the metal electrodes. The application of SEM in this failure analysis of a finished device (Figure 3, 4) shows aluminum stringers left in the cavities. This was the confirmation of a potential short previously diagnosed with the multimeter test.

On a working device one expects a capacitance, due to the electrode gap, to be in parallel with an oxide capacitance as illustrates in Figure 5. Contrarily the aluminum presence in the cavity resulted in a short of the cavity capacitance. Figure 6 shows equivalent circuit of the potential microplasma shorted by the aluminum presence in the cavity.
V. CONCLUSION

In this project, the investigation of microplasma fabrication has been reviewed. Overall, it was found that changes needed to be made in the process flow as well as the mask design to successfully complete the device. Such changes include using thinner oxide, a self-aligned etch to reduce the oxide undercut. In addition a fairly visible alignment mark is needed on the mask to alleviate alignment with a dark field mask.

ACKNOWLEDGMENT

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[4] J. Benedict, K. Focke, A. Yanguas-Gil, and A. von Keudell. “Atmospheric pressure microplasma jet as a depositing tool” Arbeitsgruppe Reaktiven Plasmen, Fakultät für Physik und Astronomie, Ruhr-Universität Bochum, Universitätsstr. 150, 44780 1 Bochum, Germany (Received 15 August 2006; accepted 24 November 2006; published online 22 December 2006)
Theoretical Study and Device Modeling of III-V Nanostructured Photovoltaics

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Abstract — A methodology for the modeling and theoretical analysis of novel nanostructured photovoltaic devices is presented in this work. The nanostructures in consideration are quantum wells and quantum dots composed of III-V materials. Their incorporation into the space charge region of an otherwise conventional solar cell is presented as a means to increase photovoltaic energy conversion efficiency. The enhancement for both single- and multi-junction solar cells is also outlined. Limitations of the available models are briefly discussed. Analyzed results allow for the further optimization of these novel devices.

I. INTRODUCTION

The efficiency of a single-junction, crystalline solar cell is limited by the laws of thermodynamics to a maximum efficiency of approximately 30% under one-sun illumination [1] and approximately 40% under full solar concentration [2]. Using a multi-junction approach, the efficiency of state-of-the-art crystalline photovoltaics has recently surpassed 40% under solar concentration [3]. Although impressive in its own right, this number is nowhere close to the theoretical maximum for such a device. Detailed balance calculations indicate that the bandgap of the middle junction in this type of architecture is slightly larger than ideal thus causing it to be the limiting component within the device stack [4].

The use of low-dimensional nanostructures provides a means to introduce a smaller bandgap material into the otherwise non-ideal device structure thus increasing photovoltaic efficiency. Additionally, the incorporation of nanostructures has been proposed in the literature as a viable way to increase the efficiency of single-junction cells by the absorption and photoconversion of sub-bandgap photons. In this work, the term nanostructures refers to quantum wells and quantum dots.

Nanostructured solar cells are being fabricated at the Rochester Institute of Technology. The development of such devices requires a fundamental understanding of the nanostructure arrays, the behavior of such structures within a single- or multi-junction solar cell, and a means to predict the operational performance of these devices. Therefore, it is the purpose of this work to develop theoretical methodologies that adequately describe the performance of fabricated devices and that are able to gauge the necessities for future device architectures.

The main focus of this work is to evaluate the ability to use a commercially available physics-based model to describe the operation and internal physics of these nanostructured devices. Additionally, bandstructure calculation of the nanostructure superlattices are also performed to give further insight into the internal workings and further optimization of nanostructured photovoltaic devices. The materials systems present here will focus on the InAs/GaAs (confined/device) system.

II. MOTIVATION

The conversion efficiency of a traditional single-junction solar cell is limited by the bandgap of the material used to make the device. The light output of the sun is made up of a wide range of wavelengths corresponding to a wide range of photon energies. However, photons with energies less than that of the bandgap in consideration are not absorbed by the device and thus do not contribute to photogeneration of charge carriers. As an example, the air-mass zero (AM0) solar spectrum [5] is shown in Fig. 1 with useful and non-useful regions for solar energy conversion for a GaAs solar cell. Additionally, the most efficient conversion of photons into free charge carriers occurs at the bandgap. Higher energy photons will exhibit a lower degree of photoconversion efficiency.

The incorporation of either quantum wells [6] or quantum dots [7] have been proposed as a method to absorb some of the otherwise wasted radiation. This in turn will increase photovoltaic efficiency of a single-junction device and serves as a motivation for this work.

Another method employed to make better use of the solar spectrum is by the use of a multi-junction architecture. In this scheme, several p-n junctions, each composed of a different material, is grown in tandem. This type of device is optimized by placing the largest bandgap junction as the top cell and by making each subsequent junction of a smaller bandgap material. In this sense, the highest energy photons (those which are quickly absorbed) are efficiently photoconverted while sub-bandgap photons, being transparent to one junction, propagate further down through the stack until they are able to be absorbed.

The state-of-the-art lattice-matched cell is the InGaP-GaAs-Ge stack as seen in Fig. 2.a. The useful regions of absorption corresponding to each stack are illustrated in Fig. 2.b. A similar scheme has recently been employed to
Boltzmann’s constant, $T_s$ is the temperature of the sun, $T_C$ is the temperature of the device, $X$ is the number of suns for solar concentration, and $f_\Omega = \Omega/\pi \approx 2.16 \times 10^5$ is a geometrical factor based on the solid angle $\Omega$ subtended by the sun with respect to a planar solar cell. Efficiency is thus given as

$$\eta = \frac{qV(\phi_s - \phi_c)}{P_s}$$

where $P_s$ is the solar constant.

For a multi-junction cell, each junction will be imbued with the quantity $(\phi_s - \phi_c)$; however, due to the constraint of current-matching, this quantity must be equal for each specific cell. This determines the potential across each junction. For the InGaP-GaAs-Ge cell under one sun blackbody illumination, the maximum efficiency is calculated to be approximately 33%. Figure 3 shows a plot of triple junction iso-efficiency contours as a function of the bandgaps of the top two junctions. The bottom cell bandgap is fixed to that of Ge (0.67 eV). As the plot indicates, decreasing the middle junction from that of GaAs (1.42 eV) to 1.2 eV yields an increase in the maximum efficiency of the triple-junction cell from 33% to 47%. This is not easily accomplished by traditional means because there is no material with this bandgap that is lattice matched to Ge and InGaP. The incorporation of nanomaterials, however, provides for an effective decrease in bandgap thus serving for an additional motivation for this work.

Extending upon the detailed balance formulation [1], [4], the calculation of solar efficiency can be shown to be dependent on the flux of absorbed photons with energies greater than the semiconductor bandgap $E_g$:

$$\phi_S = \frac{2\pi}{hc^2} Xf \Omega \int_{E_e/k_BT} \frac{e^{E/g}}{e^{E/g}+1} dE$$

and the flux of radiative emission:

$$\phi_C = \frac{2\pi}{hc^2} \left[ \int_{E_e/k_BT} \frac{e^{E/g}}{e^{E/g}+1} dE - (1-Xf\Omega) \int_{E_e/k_BT} \frac{e^{E/g}}{e^{E/g}+1} dE \right]$$

where $h$ is Planck’s constant, $c$ is the speed of light, $q$ is the elementary charge, $V$ is the applied bias, $k_B$ is Boltzmann’s constant, $T_s$ is the temperature of the sun, $T_C$ is the temperature of the device, $X$ is the number of suns for solar concentration, and $f_\Omega = \Omega/\pi \approx 2.16 \times 10^5$ is a geometrical factor based on the solid angle $\Omega$ subtended by the sun with respect to a planar solar cell. Efficiency is thus given as

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where $h$ is Planck’s constant, $c$ is the speed of light, $q$ is the elementary charge, $V$ is the applied bias, $k_B$ is

III. NANOSTRUCTURES

When the size of a system is on the order of the de Broglie wavelength, quantum mechanical effects are realized. In the case of semiconductor heterostructures, a
thin layer of a smaller bandgap material sandwiched between a larger bandgap material may form a quantum well. In this sense, the smaller bandgap material forms a potential well for charge carriers. In this well, energy levels are quantized. The band diagram is drawn for an array of quantum wells in Fig. 4. If quantum confinement occurs in all three spatial dimensions then a quantum dot is formed. An atomic force micrograph of InAs quantum dots grown on a GaAs substrate is shown in Fig. 5.

Fig. 4. Band diagram of a quantum well/dot array. A smaller bandgap material placed in a host material of larger bandgap creates potential wells for charge carriers. Quantization of energy levels occurs in these wells. Electron and hole wavefunctions are superimposed over the energy levels.

Fig. 5. Atomic force micrograph of InAs quantum dots grown on a GaAs substrate. Average quantum dot height is 6 nm. Such structures are grown by metal-organic vapor phase epitaxy.

From Fig. 4, it is easy to see that the incorporation of a nanostructure array within a host material allows for additional absorption mechanisms. Sub-bandgap photons which are not absorbed by the host material may be absorbed by the nanostructures thus increasing solar cell efficiency. Also, due to the fact that the introduced energy transitions represent smaller energies than the host bandgap, an effective bandgap decrease may be realized for the case of increasing the efficiency of the triple-junction cell as previously discussed.

In Fig. 4, eigenfunctions are drawn for each of the quantized energy levels. For thick barriers (i.e. the host material between adjacent quantum wells), the eigenfunctions resemble that of an isolated quantum well. Decreasing the barrier thicknesses, such that non-negligible overlap of carrier wavefunctions occurs, leads to the formation of minibands as diagramed in Fig. 6. This allows for additional absorption and carrier transport mechanisms. A periodic array of quantum wells or quantum dots thus forms a superlattice in the sense that a periodic array of atoms forms a traditional crystal lattice. Miniband formation is necessary in the theory of the intermediate band solar cell [7], [8].

![Miniband formation](image)

**IV. DEVICE MODELING**

**A. Simulation Methodology**

The modeled device is a GaAs p-i-n solar cell as seen in Fig. 7. The presence of a thin intrinsic region serves to increase the depletion width. Additionally, the nanostructure array is centered within the i-layer. The InGaP window and back surface field (BSF) reflect minority carriers towards the junction.

The device is modeled as a two-dimensional structure as shown in Fig. 7.a. Additionally, only one grid finger of the solar cell is simulated. These approximations keep computation time to a minimum. After calculations are completed, geometrically dependent results, such as current, are multiplied by a scaling factor that accounts for the three-dimensional nature of an actual device; this simulates the device structure as seen in Fig. 7.b. Finally, another multiplication factor is included to account for the desired number of grid fingers; this simulates the structure in Fig. 7.c and is comparable to an experimental device.

The Silvaco Atlas software package is utilized for the device simulations. Silvaco Atlas is a physics-based device simulator that numerically solves coupled Poisson and continuity equations by iteration. Additional models are included and invoked as necessary. Due to the relatively large dopings encountered throughout the simulated device, Fermi-Dirac statistics are used to determine carrier concentrations. Shockley-Reed-Hall and radiative recombination models are also invoked.
Additional recombination is handled at the hetero-
interfaces and the terminal surface. Thermionic emission
is also accounted for at the InGaP-GaAs interfaces.
Photogeneration of charge carriers is modeled using AM0
illumination.

![Fig. 7. The solar cell is modeled as a) a two-dimensional structure using
only one grid finger. These approximations keep computation time to a
minimum. Final results that are dependent on geometry, e.g. current, are
modified by a scaling factor to account for b) the three-dimensional
nature of an actual device. An additional factor is included to c) account
for the desired number of grid fingers to make the model comparable to
an actual device.]

For the simulation of a nanostructured device, an InAs
quantum well array is centered within the i-region of
Fig. 7. This is done to simulate the InAs quantum dot
solar cells that are being fabricated at the Rochester
Institute of Technology. The justification for using the
quantum well model in the device simulation is that this
model calculates quantum confinement only in the y-
direction (referring to Fig. 7). In the actual device, the
quantum dots are more strongly confined in the y-
direction; this is also the direction of current flow. Thus
the use of the quantum well model to approximate a
quantum dot array is justified.

While invoking the quantum well model, the effective
mass Schrödinger equation is numerically solved in and
around quantum confined regions. The solution gives
energy eigenvalues for further use in bandstructure-
dependent optoelectronic models to be discussed.
Corresponding eigenfunctions are also determined as part
of the solution.

The bandstructure-dependent optoelectronic models
incorporated in Atlas use the results from the quantum
well model to determine the effects of optical gain and
spontaneous emission [9]. These effects are useful for
laser and LED simulations, respectively. They do not,
however, adequately describe quantum mechanical
photogeneration of electron and holes. What would be
necessary is a model that emulated or solved the selection
rules which govern carrier transitions determined from
Fermi’s golden rule. An appropriate model for quantum
mechanical photogeneration has not been identified.

B. Results

A baseline device, i.e. one without a quantum well
array, was simulated and gave a close match to an
experimentally fabricated baseline device. The purpose
for doing this was to confirm validity of the device
simulator with a conventional device; once confirmed, a
novel device may be simulated with impunity. Both the
simulated and empirical device resulted in a short circuit
current $I_{sc}$ just under 25 mA/cm² and an open circuit
voltage $V_{oc} = 1.04 V$. The quantum well device exhibited
slightly better device characteristics ($I_{sc} = 26.8$ mA/cm²,
$V_{oc} = 1.05 V$) but nowhere near the expected enhancement
for either an ideal quantum well [6] or quantum dot [7]
cell. Current-voltage characteristics of the fabricated
device and the two simulation types are plotted in Fig. 8.

![Fig. 8. Current-voltage characteristics for the fabricated baseline device
and model and quantum well model. The baseline model gives a close
match to experiment thus allowing for the further simulation of novel
device. The quantum well model gives a slight improvement in the
device characteristics but not to the degree expected for such a device.]

Analysis of the quantum efficiencies of the discussed
examples, as in Fig. 9, gives information regarding the
spectrally-dependent device response. For the baseline
comparison, although the model underestimates the red
response of an actual device, it overestimates the blue
response thus accounting for the close match as seen in
Fig. 8. As for the quantum model, sub-bandgap
absorption is observed, however, characteristic peaks
corresponding to quantized energy transitions are not.
These peaks are commonly observed in quantum
well [10] and quantum dot [11], [12] solar cells. The
reason for not observing these peaks is as was discussed
regarding the lack of an appropriate model that handles
quantum mechanical photogeneration.
In lieu of obtaining the desired electrical results from the quantum well model, the analysis may be focused on the fundamental physics of the nanostructured device. The simulated band diagram in the nanostructured region of the quantum model is shown in Fig. 10. Calculated energy eigenstates are plotted within the InAs wells. For the system plotted, a single eigenstate occurs in the InAs conduction band and five heavy hole states and a single light hole state is realized in the InAs valance band. Also plotted is the wavefunction corresponding to the InAs conduction band eigenstate. This type of analysis is paramount in the research because the results summarized in Fig. 10 constitute values that cannot be directly measured experimentally but that lead to a better understanding of the device and its further development.

In the modeling that lead to Fig. 10, the well thickness was chosen to match the average height of the quantum dots analyzed in Fig. 5; the barrier thickness was chosen because it allows for non-negligible wavefunction overlap. Based on the model, for 6 nm InAs wells, non-negligible wavefunction overlap occurs in the conduction band for approximately 8 nm barriers and thinner. Therefore, for this specific system, an 8 nm barrier thickness represents the threshold necessary to induce miniband formation. A plot of the wavefunctions for 10 nm and 7 nm barriers is given as an example in Fig. 11. In this plot, the 7 nm wavefunction can be seen to overlap throughout the well region while the 10 nm wavefunction does not.

V. BANDSTRUCTURE CALCULATIONS

In the previous section, results were interpreted arguing for the formation of a superlattice miniband. Exact information regarding the miniband is necessary to confirm the Atlas results as well as to take advantage of it in a photovoltaic device. One such way of determining
this information is by calculation of the superlattice bandstructure.

Bandstructure calculations for the InAs/GaAs superlattice are performed by invoking the Kronig-Penny model. This model approximates the crystal potential to be in the form of a periodic square potential. Although a poor approximation for a real crystal, this model proves to be an excellent choice of the superlattice since the band edges are in the approximated form.

The textbook example of the Kronig-Penny model is derived from the Schrödinger equation [13]:

\[
-\frac{\hbar^2}{2m} \nabla^2 \psi + U \psi = E \psi
\]

(4)

where \(\hbar\) is the reduced Planck’s constant, \(m\) is the particle mass, \(U\) is the potential energy, \(E\) is the energy eigenvalue, and \(\psi\) is the eigenfunction. For a semiconductor superlattice, \(U\) is set equal to the band edge and \(m\) is replaced by the effective mass \(m^*\). As a caveat, the effective mass in a superlattice becomes spatially dependent due to the presence of different materials. Thus the kinetic energy operator

\[
T = -\frac{\hbar^2}{2m^*} \nabla^2
\]

(5)

in (4) has the property

\[
\langle f | T g \rangle = \left( m^* \frac{\nabla f}{m} \right) \langle g \rangle
\]

(6)

for quantum states \(|f\rangle\) and \(|g\rangle\). Therefore (5) is non-Hermitian making (4) no longer valid. Equation (4) must then be replaced with the effective mass Schrödinger equation [14]:

\[
-\frac{\hbar^2}{2m^*} \nabla^2 \psi + U \psi = E \psi
\]

(7)

This form contains a Hamiltonian that is Hermitian and reduces to (4) in the limit of a spatially independent effective mass. Using (7), the Kronig-Penny model of a semiconductor superlattice may be derived in a similar fashion to the traditional method of using (4) [13].

The calculated electron dispersion is shown in Fig. 12 for a 7 nm barrier system and a 1 nm barrier system. Energy is referenced with respect to the InAs conduction band edge. The dashed bands correspond to orbitals that overlap with the GaAs continuum; electrons at these energies therefore belong to the GaAs continuum and not the superlattice bandstructure. The bottom band corresponds to the calculated conduction band eigenstate as in Fig. 10. The second band in Fig. 12.a is not realized in the Atlas simulation due to its close proximity to the GaAs continuum (~0.59 eV). This is further exemplified in Fig. 12.b where the second band transitions from a bound to a scattering state.

Fig. 12. Calculated electron dispersion in an InAs/GaAs superlattice for a) 7 nm GaAs barriers and b) 1 nm GaAs barriers. Dashed bands indicate orbitals that overlap with the GaAs continuum. Energy is referenced with respect to the InAs conduction band edge.

From Fig. 12, the width of the miniband is easily determined. This information is especially important for the intermediate band solar cell in which a fundamental requirement is that the intermediate band be half-filled with electrons [15]. The miniband width is plotted as a function of barrier thickness in Fig. 13. Decreasing barrier widths gives rise to an asymptotic increase in miniband width due to enhanced well-to-well coupling brought about by stronger wavefunction overlaps.

Fig. 13. The decrease in barrier width gives rise to an asymptotic increase in the width of the miniband. This is due to the larger degree of wavefunction overlap that occurs for ever decreasing barrier widths.

VI. CONCLUSION

The modeling of novel photovoltaic devices based on nanostructure arrays has been undertaken. The specific system investigated here was the incorporation an InAs quantum dot array in a GaAs host. For device simulations, the InAs quantum dots were approximated as quantum wells for the sake of invoking an available model.
Justification for doing so was given and viable results were obtained. The ability to simulate a baseline device was presented and allowed for further simulation with the inclusion of the nanostructured arrays. Although an appropriate model for quantum mechanical charge carrier photogeneration was not identified, basic quantum effects were adequately simulated and analyzed. As an extension to this, bandstructure calculations were performed based on an effective mass Kronig-Penny model. With these analysis methods, optimization of the nanostructured arrays are now possible and will lead way to more efficient photovoltaic devices.

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Developing an Empirical Model for Tunable Porosity in Porous Nanocrystalline Silicon Membranes

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Abstract—In this study, a new process for the fabrication of porous nanocrystalline silicon (pnc-Si) membranes is proposed, and the early stages in the development of an empirical, stress-based model for tunable porosity are revealed.

Pnc-Si membranes that were fabricated by the proposed process showed substantial improvements in membrane morphology, i.e., porosity and pore uniformity across the wafer. These improvements were assumed to be related to stress, as suggested by the addition of materials that differ in Young’s Modulus and in coefficients of thermal expansion. In order to explore this assumption, stress measurements were conducted via stylus trace on a Tencor P2 Profilometer. Extensive average stress (dynes/cm²) measurements were performed by varying thermal and RF Magnetron sputtered SiO₂ thickness on bare, 400 um thick, <100> orientation, double-sided polished silicon wafers.

It was found that the stress-profile differences between the standard and proposed processes were significant as the change in the wafer bow (due to film stress), across the wafer (relative to the bare substrate), were plotted for varied oxide thickness during the three major stages of pnc-Si development. The resulting plots were 2nd order polynomials (best-fit RMS = .970-.999), which agree with the form given by Stoney’s equation for macro stress acting in a coating deposited on a thick substrate. These differences have been consistent in multiple experiments and are currently being evaluated for their role in membrane porosity.

Index Terms—porosity, porous nanocrystalline silicon (pnc-Si) membranes, profilometer.

I. INTRODUCTION

This study is based on a new type of porous silicon material in the form of an ultrathin nanoporous membrane, first reported in the journal Nature¹. Termed porous nanocrystalline silicon (pnc-Si), this material is fabricated through solid-phase crystallization of a sputter deposited amorphous silicon (a-Si) film on a silicon wafer substrate.

Pores in the size range of 5 nm to 100 nm form during a brief annealing step and pass completely through the original 5 nm to 25 nm thick amorphous film. Following photolithographic and etching processes, freely suspended porous membranes are made that offer unprecedented efficiency in nanoscale separation processes and are sufficiently thin for transmission electron microscopy (TEM) applications.

II. OBJECTIVE

The standard process in the fabrication of pnc-Si membranes is shown below (Fig. 1):

Fig. 1. Standard process for the fabrication of pnc-Si membranes.
the center of the wafer, but maintain reasonable densities in positions along the wafer edge (Fig. 2):

![Figure 2](image.png)

Fig. 2. Three regimes of pore formation across the wafer for pnc-Si membranes fabricated with the standard process.

The non-uniformity in porosity was verified by analysis of TEM samples across several wafers fabricated by the standard process in Fig. 1. The TEM images in Fig. 3 (below) show the porosity difference that was observed in samples positioned in the center and edges of the wafer:

![Figure 3](image.png)

Fig. 3. TEM micrographs of two pnc-Si membrane samples taken from center and edge positions on the same wafer. This non-uniformity in porosity has been frequently observed for membranes fabricated with the standard process in Fig. 1.

This non-uniformity in porosity has hindered yield and has impeded efforts in developing a model for predictable porosity in pnc-Si membranes.

III. EXPERIMENT

A. Proposed Process

In this study, a new process is presented that offers improvements to the traditional pnc-Si process deficiencies as described above (Fig. 4):

![Figure 4](image.png)

Fig. 4. Proposed process for the fabrication of pnc-Si membranes resulted in improved porosity and pore uniformity across the wafer.

The main feature of this newly developed process is the replacement of the RF magnetron sputtered SiO\textsubscript{2} (underneath the membrane) with a thin (20nm-40nm) thermally grown oxide that protects the silicon front surface during the entire process. Tetra-ethyl-ortho-silicate (TEOS) is also deposited on the backside of the wafer (PECVD), after the initial thermal oxide growth, in order to provide a robust pattern that can withstand the ethylenediamine pyrocatecol (EDP) etch of silicon in subsequent processing.

B. Process Improvements

Consequently, the addition of back-side TEOS and thermally-grown SiO\textsubscript{2} has resulted in substantial improvements in membrane morphology, i.e., porosity and pore uniformity across the wafer. The difference in porosity can be observed from two TEM micrographs that were generated from two different processes (Fig. 1 & Fig. 4), taken from the same position on the wafer (Fig. 5 & Fig. 6):

![Figure 5](image.png)

Fig. 5. TEM image of a pnc-Si membrane (magnified 150kX) for membranes fabricated with the standard process in Fig. 1. The resulting porosity is low (0.33%-2.7%) and non-uniform across the wafer.
Further analysis of membrane porosity was conducted using a Matlab image simulator to generate statistical porosity data for TEM micrographs to provide quantitative results. The results show that the standard pnc-Si process produces membranes with porosity ranging from 0.33%-2.7%, while the proposed process achieves porosity in the range of 4.2%-12.4%.

To show that pore uniformity across the wafer had been achieved using the proposed process, refer to Fig. 7 where TEM micrographs of the membrane at the center and edge of the wafer are shown (Fig. 7):

![TEM micrographs of two pnc-Si membrane samples taken from center and edge positions on the same wafer.](image)

These TEM images can be compared directly to the images in Fig. 3. After several samples had been fabricated and compared, it became evident that, for membranes fabricated with the proposed process, porosity had been maintained across the wafer. The improvements in porosity and in pore uniformity across the wafer with this process was assumed to be stress-related, as suggested by the addition of materials that differ in Young’s Modulus and in coefficients of thermal expansion.

C. Stress Characterization

In order to explore this assumption, stress measurements were conducted via stylus trace on a Tencor P2 Profilometer. Extensive average stress (dynes/cm²) measurements were performed by varying thermal and RF Magnetron sputtered SiO₂ thickness on bare, 400 um thick, <100> orientation, double-sided polished silicon wafers. These results were then compared to reliable experimental average stress values (as determined by C.H. Bjorkman et al.²) to assure confidence in the accuracy of the profilometer.

To obtain results for analysis, the change in the wafer bow (due to film stress), across the wafer (relative to the bare substrate), were plotted for varied oxide thickness during the three major stages of pnc-Si development. The resulting plot is shown below for membranes fabricated with the standard process (Fig. 8):

![Stress-profile across the wafer for deposited SiO₂ layer beneath the membrane. Measurements were conducted for i) initial oxide on bare silicon, ii) three-layer stack (SiO₂/a-Si/SiO₂) before anneal iii) three-layer stack after anneal.](image)

All of the RF magnetron sputtered SiO₂ stress-difference curves that were generated in this experiment exhibit a translational shift in relative minima/maxima from the initial SiO₂ deposition (on bare Si) to the three film layer stack (SiO₂/a-Si/SiO₂). The translational shift is given in its general form as:

\[ f(x) \Rightarrow f(x \pm \beta) \]

where \( \beta \) describes the shift in terms of wafer position.

The same stress measurements were conducted for a bottom thermal SiO₂ layer that is introduced with the proposed process:
This study has shown that the proposed process not only succeeded in reducing process steps and controlling pore uniformity, but has also revealed the necessity for stress-based pnc-Si experiments. To address this, the initial stages in the development of an empirical model for pnc-Si stress-based measurements were conducted. This development is profound since a model characterizing the effects of stress modulation on pnc-si membrane pore formation has never been reported.

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APPENDIX
Deep Submicron Pattern Formation for Selective Epitaxial Growth of III-V Semiconductors

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In the world of optoelectronics a common barrier has been integrating logic and device circuits on a single substrate, as it was generally only possible to optimize the device for the logic, or the optoelectronic device at hand. However, a new approach that uses metal organic chemical vapor deposition (MOCVD) enables the growth of III-V semiconductors on silicon substrates. The fact that III-V semiconductors can now be integrated within the current silicon CMOS processes may allow new possibilities. An approach to investigate the feasibility of this process has been investigated. The enabler to integrate III-V is an innovative approach called aspect ratio trapping (ART) developed by Amberwave. This method involves the use of oxide trenches to trap defects in a buffer region during crystal growth (Figure 1). The growth process is a selective growth that only occurs on silicon and this process. ART on III-V's only works well with a ratio greater than 2:1 for oxide thickness to patterned oxide opening. The objective of this project is to develop a process to build these structures at RIT, perform a growth in Amberwave's reactor, and then characterize the film. In the future, RIT may also become involved in the Chemical mechanical planarization (CMP) process for these structures.

A mask was designed with four different pitches to characterize different density of features (fig. 5). Text labels were also added on the mask so that one could optically determine the pitch and in addition the reticle had labels that describe the relative field position to be used for CMP characterization. In order to be able to pattern the submicron features with a positive tone resist, a bottom antireflective coating (BARC) donated by Brewer Science was used to increase the process window in which a useable image was present. The thickness of this layer was tuned specifically to minimize the substrate reflection. By optimizing film thickness parameters and setting the focus near the bottom of the resist, this yielded much greater process latitude. After this the patterns were etched using the P5000’s magnetically enhanced etch chamber, the etched features were imaged a new Zeiss SEM at University of Rochester and the 3:1 etched features yielded acceptable profiles (fig. 10).

In order to prepare patterned wafers here at RIT, the level of contamination in the process and toolset at RIT must to be characterized. The main concern is to not contaminate the growth chamber that Amberwave will be using to perform the growth of the semiconductor materials. A method of metals analysis called vapor phase decomposition-inductively-coupled plasma mass spectrometry (VPD ICP MS) was utilized as a surface contamination metric. After sending the samples to ChemTrace, it was determined that an RCA would dramatically reduce the surface contaminates present on the wafer to acceptable levels for the MOCVD reactor (fig. 6).

Interesting future projects include building and characterizing a GaAs laser. Another appealing project involves building silicon drive transistors connecting them to GaAs tunneling or memory devices. It was shown that the pattern transfer portion is indeed possible at RIT and this project has set the stage for future projects regarding aspect ratio trapping.

Index Terms—Aspect Ratio Trapping, Gallium Arsenide epitaxy, VPD ICP MS

I. INTRODUCTION

This project investigates the task and process steps involved in patterning and characterization of submicron high aspect ratio structures at the Rochester Institute of Technology. ART (aspect ratio trapping) is a selective growth process developed by Amberwave Systems. Shown in fig. 1 there are two different samples of GaAs epitaxially grown on silicon. The first sample does not contain any oxide side walls to act as a trapping site. Observe on in fig. 1 b. the images shows single crystalline silicon with no defects at the device surface.

Fig. 1a. Bulk GaAs on silicon with surface defects b. ART GaAs

Currently Amberwave does all of their patterning with a company that performs interference beam lithography. This is a rather expensive process, and it is desirable to build a process at RIT to be able to pattern these kinds of structures. Their current process also lacks additional items that were added to the current reticle design to make characterization less complicated. Motivation to work with ART samples it is a very efficient way to integrate III-V’s on silicon substrates. This process also would work well to make optoelectronic/photonics devices on silicon substrates and high mobility MOSFET channels.

The goals for this project were to pattern high density oxide openings for Amberwave’s structures. Amberwave has determined that they would like to characterize growth on two different profiles. The profile on the left (fig. 2 a) is a high aspect ratio 2:1 RIE (reactive ion etched) oxide sample. The profile on the right (fig. 2 b) is a similar sample, but it has an additional Etch performed to give it a V shaped profile on the bottom. Another key aspect of this project

Fig. 2a. High aspect ratio 2:1 RIE oxide sample b. High aspect ratio V profile
is to design a reticle that can be patterned with the equipment here at RIT. Finally, the appropriate process conditions were determined which included the following: minimum feature size, transferring this pattern via an etch, and characterizing the contamination levels in our lab. Finally the final profiles were evaluated.

Fig. 2a. RIE etched Sample b. RIE KOH etched sample.

II. THEORY

2.1 VPD ICP MS Concepts

The VPD ICP MS process involved several steps. First the wafer was placed in an ultra clean wet etch chamber. This chamber was highly saturated with hydrofluoric acid vapor. The oxide then reacts with the HF vapors. A drop of ultra pure acid etchant was added to the surface of the wafer and the surface contaminates were then incorporated into this liquid. This liquid was then collected and the ICP-MS analysis was then performed. A Perkin-Elmer Sciex ELAN 6100 DRC ICP-MS was used in the ICP MS analysis. It was calibrated with the three different NIST standards for the thirty metals under examination. The thirty elements were Al, As, B, Ba, Be, Bi, Ca, Cd, Co, Cr, Cu, Ga, Ge, Fe, In, K, Li, Mg, Mn, Mo, Na, Nb, Ni, Pb, Sb, Sn, Sr, Ta, Ti, Tl, V, W, Zn and Zr. The detection limit was generally on the order of \(10^3\) or \(10^4\) atoms/cm\(^2\) depending on the size of the wafer and trace element being tested. The accuracy of this method was based on the level of the signal above the detection limit. Generally when the signal was greater than one order of magnitude above the detection limit, the data had an accuracy of +/- 15%, but when it was lower than this threshold value it had an accuracy of +/- 30%.

Equation 1 can be explained as the method of how the amount of material in the liquid sample is converted into atoms/cm\(^2\) on the wafer surface. \(C_0\) is the concentration of the sample material at interest in the solution and \(C_b\) was the concentration of the baseline sample. \(V\) is the volume of the etchant solution in mL and \(D\) is the density of this solution in g/cm\(^3\). \(N_A\) was Avogadro’s number to convert for the number of moles of the sample. \(AW\) was the atomic weight of the trace metal of interest and finally \(S\) represented the analysis surface area.

The Perkin Elmer Sciex ELAN offers many advantages in comparison to many of the other ICP MS systems available. It used several novel design features that enable it to have very good sensitivity to elemental species that before were very difficult to analyze. One of the main problems with many past ICP MS systems was that there are polyatomic interferences species that are the same atomic weight as the analyte species at hand. The Perkin Elmer system used a dynamic reaction cell (DRC) that chemically scrubbed the interfering species from the ion beam by using a reaction gas that did not interfere with the plasma chemistry and also does not change the signal of the analyte ion. Shown below (fig. 3) is the typical setup for the DRC system. This system, along with several other features, have been shown to drop the background noise by a factor of 1,000,000 in comparison collision based systems. A common interference is an argon oxygen plasma species which has an atomic weight of 56, which is the same atomic weight of the most common isotope of iron. By using this chemical scrubbing technique it almost completely eliminates all of the background noise resulting in very low and efficient detection limits. This method of metals analysis was also much more sensitive than SIMS, TXRF or similar methods.

Fig. 3 IC P system basic layout [2]

2.2 LITHOGRAPHY SIMULATIONS

The first part of the project involved determining what the minimum pitch to pattern here at RIT. Prolith was used to perform lithography simulations. Generally for imaging to occur a NILS value of 3 or greater was determined to be desirable, so this was what determined the minimum half-pitch. The minimum half pitch used was 400 nm for all in the process window. This ended up being a K1 of .58 which is fairly aggressive for full field imaging.

\[
P = \frac{k \lambda}{2 \cdot N_A}
\]

Equation 2 Resolution minimum half pitch equation.

In order to achieve the desired pitch on a wafer with a thermally grown oxide wafer, an additional step had to be taken to increase the process window. An I-line BARC was chosen to perform this task. Brewer Science’s ARC I-CON 16 was generously donated to RIT by Brewer Science. This BARC was chosen because it was not developable in CD-26. This BARC had to be etched, so it should end up with a much more anisotropic profile giving a much better process window rather than an isotropic wet developable BARC. A BARC or bottom antireflective coating increases the process window by minimizing the substrate reflection. Shown here are three profiles. It can be seen that the second sample with the oxide has 3 interfaces, more that allow interference to occur which can cause standing waves to form during the exposure process. Standing waves are generally undesirable and decrease the process window. By tuning
the thickness of the BARC layer the optical path length can be set correctly so destructive interference occurs at the photoresist-BARC interface and thus reflection is minimized at this surface and consequently standing waves are minimized.

![Fig. 5 Substrate reflections with various films](image)

III. DESIGN

The first part of the design phase of this project was to push the lithography to the limits of the toolset and process capability at RIT. The limiting factors on the Cannon FPA-2000i i-line stepper were a numerical aperture of .52 and a sigma of .6. Based on the NILS simulation a reticle was designed to incorporate the most dense features capable here at RIT.

The lithography constrains were that patterning must occur on 6 inch wafers, because there would be more useful die on 6 in wafers and also this size will work well with the geometry of their reactor. The field size was also limited by bulk device and optical characterizing. RIT in the future may be involved with the CMP of some of these post growth structures. Fig. 1 shows the results of performing a growth and the CMP of these samples is not trivial, due to dishing in the oxide spacer sidewalls, hence the reason for the four different pitches chosen. Finally these features must be transferred to the underlying oxide and maintain a high aspect ratio: greater than 2:1. This means that in order for the current process to be acceptable the structure will need at least a micron of oxide to be able to obtain these high aspect ratio features based on the 400 and 500 nm limitation in the lithography process. Figure 5 shows the arrangement of the new reticle with contacts in the KERF regions.

![Fig. 5 RIT ART mask design](image)

IV. CHALLENGES ENCOUNTERED

The first main concern was to determine the metal levels in our laboratory. A method of characterizing this process was to perform a vapor phase decomposition inductively coupled plasma material spectrometry (VPD ICP MS) analytical test to determine the metal levels running though our process flow. This must be completed so that Amberwave's rector does not become contaminated.

Another Main issue during the process development was the writing of a reticle. These current features written were some of the smallest and certainly the most dense patterns written at RIT. The main problem in getting the reticle to write was that the time out feature on the tool was set too long so the mask writer would write for 10 minutes and then perform another baseline registration. This time was too long and the tool would simply drift too long during this time and it would not be able to continue writing due to reregistration errors. This problem was simply fixed by setting this time to a much shorter more reasonable value such as 2 minutes between reregistration.

Some initial tests were performed and it was determined that the process window was very small when patterning on oxide. An initial FE had shown that a bare silicon wafer had a minimum resolvable feature of 350 nm. However once this patterning was done on a wafer that had a thermal oxide grown on it, the minimum feature size was 550 nm, because the CD swing was much greater with this additional interface.

Initially the OLN-620i resist was thinned down to a ratio of 2:1 by adding a 50:50 mixture by volume of resist to PGMIA solvent. This new lower viscosity resist had a new spin speed range of 400-500 nm. However it was determined after an etch screening this would not protect sufficiently during the etch process. In order for a usable image to occur in the normal viscosity resist a bottom anti reflective coating or BARC was used to improve the process window. Brewer Science's ARC-ICON was chosen to be the best choice for advanced I-line processing. Another challenge that this involves is the fact that with a positive tone resist and a darkfield reticle this process involved imaged spaces rather than lines and due to the energy distribution this also caused a decreased exposure latitude. In the future there may be more process latitude to work with a clear field reticle and a negative resist.

Another problem that occurred was the variation in oxide thickness that resulted in pattern fallout at the edge of the wafer. Even though the variation from center to edge was only about 1.5% when these non-idealities compounded with an additional 1.5% thickness variation in BARC thickness and resist thickness, it causes significant difference in optical path length that increases substrate reflection to a non optimal location on the swing curve. Future work could improve upon the oxide thickness variation, and more importantly improve spin coating with a designed experiment. Some of the important input factors may be ramp rates and really controlling how the photoresist and BARC flow and remove solvents across the wafer.

Initially the oxide etch was performed in the Drytec Quad RIE system and it was determined that this tool was not optimum for etching 6 inch wafers due to the electrode design. A much better tool for 6 inch wafers, the P5000 was utilized in the etch process. However it was determined after trial and error in this tool that the wafers could not have oxide on both the front and back side, otherwise arcing would occur and could potentially ruin the process kit. The reason that this arcing occurs is based on the fact that the tool

V. PROCESS PARAMETERS

The first step in preparing a device wafer was to grow the thermal oxide. Bruce tube 1 was used to grow the wet thermal oxide. This oxide was chosen to be wet thermal oxide, rather than a dry thermal due to time constants and the fact that growing oxide on the order of 1 micron was expensive and takes a relatively long time and can use significant chemical. Also an thermal oxide much thicker than 1 micron causes such a great amount of stress that it induces oxidation induced stacking faults which may not be annealed out. This oxide could be deposited, but one of the constraints was that this must be a thermal oxide due to its higher interface quality. A deposited TEOS may be interesting to investigate for backend devices with a lower
allowance for a thermal budget. The SMFL 10000 angstrom recipe was used. An oxide thickness of 950 nm was measured. Next a blanket resist coat was performed so that the front side of the wafer could be protected. A ten minute HF etch was then performed in the 5.2:1 BOE etch to remove all of the oxide off of the backside of the wafer so that arcing would not be a problem in the P5000 etch chamber.

A Prolith simulation was performed to determine where the minimum substrate reflection is for the BARC. The thickness that yielded excellent results was around 100 nm BARC thickness. This thickness was limited by the speed of spinning 6 inch wafers. Ideally it would have been easier for the BARC to be coated around 150 nm, and the originally targeted oxide thickness would allow for this, but due to the offset in the oxide thickness. The spin speed curve was used for both Brewer Science’s datasheet. This curve was verified by measuring the thickness with both the profilometer and nanospec at three different spin speeds so that an optically measured thickness and a profilometry measurement was obtained.

The BARC was coated using the appropriate spin speed. A spin speed of 4000 RPMs was used to obtain a BARC thickness of 110 nm. A single stage 180 degree bake was used to crosslink the BARC. No prime was used for both the resist step and the BARC coating. The resist was then coated by using the standard coat recipe with a spin speed of 3250 RPMs. A post apply bake (PAB) of 90 degrees Celsius was used. Two separate step bake jobs were ran. The first job (RIT_ART) was programmed to run with reticle carrier 12 and used the recently designed RIT ART reticle. An optimum exposure of 130 mJ/cm² was used. A best focus of 1 um was found to be focusing to the bottom of the resist stack. The resist thickness was verified to be 1050 nm. The second exposure RIT_ART2, was done just to form open areas in which bulk film could be grown directly on silicon without spacers. This region was also very beneficial to measure film thickness and to watch during the etch process because there was no optical end point set up on the P5000 etch tool. The post exposure bake (PEB) was kept at the default 110 degrees centigrade. A single stage puddle develop was used. A two stage puddle develop was also experimented with, but it did not yield any better results. Finally the hard bake was lowered from 132 degrees to 125 degrees to ensure that the resist did not flow.

The final etch process used on the P500 was composed of three steps: a stabilize step which the gas flows, 40 Gauss electric field turned on for 20 seconds, followed by the etch step which turned on the RF power to 500 W, and finally the gases were turned off and the chamber was pumped down. The gases used were 100 SCCM of CHF₃, 50 SCCM of CF₄, and 10 SCCM of O₂. A hard ash was then done to remove all of the organics from the wafer surface. After this was completed a 2 minute KOH etch was performed to give the v-groove profiles. Finally an RCA clean was completed to remove any surface contaminates.

VI. DISCUSSION OF RESULTS

While charactering the lithography some screening ran some screening runs through the process flow to determine if the SMFL fab was in fact clean enough to run samples through an outside companies reactor. Due to cost only several samples were sent to a sample called Mentron Chemtrace. Several wafers were ran through a blanket version of our process flow and the analysis method used was VPD ICP MS. This analysis method must be done on wafers without topography. Notice the results of the top ten contaminates on the right. The first wafer was the bare starting substrate. This sample was run to get a baseline for our starting material and to determine that our starting material was not the source of the surface contaminates. The second sample was one that ran through the complete pattern transfer process. Finally the last sample was exactly the same as the second one with the exception that it had an RCA clean after wards. It can be seen that generally speaking the cleaned wafer came out much lower than the process flow run, and in some cases even lower than the starting substrate. Notice the high levels of Al this is probably due to the fact that a lot of the etch chamber is made of aluminum. Also many of the other metals are components of stainless steel. A further investigation needs to be done to confirm where these contaminates have come from. These metal levels are at acceptable levels to perform a growth in an outside reactor.
reflection. Figure 8 illustrates the idea that the process latitude and allowable film thickness variation is quite good in this region. However when the device wafers were grown the oxide thickness came out a bit thinner than the previous run. This now put the swing and reflectivity in a non optimal location can be seen by the 2 in fig. 8. These wafers were reworked with an adjusted speed on the BARC to give another thickness and my small features again appeared when the other minimum was used. This is a good verification that PROLITH can be used to accurately predict the process at RIT.

In the etch process the selectivity was characterized while etching the BARC and after the BARC had been etched. Initially the selectivity was about 1.2:1 while etching the BARC because some of the photosist was etching was well due to the oxygen in the etch chemistry. The BARC needed oxygen to etch well. The oxide then had an selectivity of about 2:1. Notice in fig. 9 there was remaining resist and this allows for an over etch to account for etch non-uniformities.

It can be seen that the etched profiles turned out well for the 3:1 features however a slight over etch has occurred. The 1:1 features showed some scalloping, or summing issue that was most likely caused by the dramatic over etch. It is interesting to see that this image shows the aspect ratio dependence of the etch.

Finally a KOH etch was done to generate the additional samples that Amberwave had wanted to characterize. One of the main concerns was that all of the etch material was not cleared out, and the fact that V groves formed is a good indication that this occurred.

VII. CONCLUSION

It has been shown that high aspect ratio patterning here at RIT was indeed possible, but the process window was very slim. Many of the challenges presented involved working with an outside company, and several delays occurred during the project that was not planned for in the project timeline. An interesting side project involved running several screening experiments to determine the metal contamination levels in our the SMFL laboratory. Metal contamination levels are low enough after a RCA clean to send material out and several samples are ready to send to Amberwave. Future work to continue this project includes improving the current process. One method of patterning significantly smaller features would be to make a chromeless phase shift reticle. Once these structures are generated it would be possible to build a GaAs laser. Other device related projects could work on integrating silicon devices with other III-V's such as high mobility MOSFET channels. It was seen that ART is a key enabler to integrating III-V semiconductor materials into the current silicon infrastructure.

ACKNOWLEDGMENTS

Amberwave provided a great deal of project support and without them this project would have not existed. Brewer Science was very generous in the donation of the ARC i-con BARC which was a key enable in this project. The National Science foundation was also very accommodating. Finally Brian McIntyre from the University of Rochester provided a great service by taking high quality SEM images of the etched samples. In addition Mentron's Chemtrachemdivision was very helpful in performing analytical metal level analysis tests. Finally Prolith version 7.1.1 was used for all of the simulations.

REFERENCES


Kenny Fourspring (M'08) was born in Erie Pennsylvania, and graduated from Northwestern Senior High School in 2003. He is currently attending the Rochester Institute of Technology studying microelectronic engineering.

He had worked for the Office of Naval Research in Washington DC in the Summer of 2005, doing research on carbon nanotubes for field emitters. Then his work led him to Richmond, VA and he worked for Infineon Technologies as a lithography process engineer. Intel technologies was the next stop on his road map in the winter of 2007 again working as a lithography process engineer.

Mr. Fourspring has been a student member of IEEE at the Rochester Institute of Technology, in the past helping out with their design conference. Also he is a member if MESA (Microelectronic Engineering Student Association) which contributes to many projects at the SMFL (Semiconductors and Microsystems Fabrication Laboratory).

Fig. 8 Substrate Reflectivity vs. film thickness

Fig. 9 Etch Rate of oxide and photosist

Fig. 10 a 3:1 500 nm spaces, 1:1 400 nm lines, 1:1 500 nm v-grooves
Fabrication of Metal-High-κ Capacitors on Germanium (May 2008)

Rahul K. Gupta, Student, Department of Microelectronic Engineering

Abstract—The objective of this study is to gain understanding of MOS devices built on germanium. Ge PMOS transistors were simulated using Silvaco. MOS capacitors have been fabricated using hafnium oxide, a high-κ dielectric, and molybdenum, a metal gate. The capacitance-voltage (CV) characteristics of the devices were obtained and studied. During the deposition of hafnium oxide on germanium substrate, the surface integrity plays a significant role. Two different surface treatments for the Ge substrates were implemented: one with NH₃ immersion at 650°C for one minute, the other with a deionized (DI) water rinse for one minute. In doing so, one can examine how nitrogen passivation prior to the dielectric deposition impacts device performance compared to a standard rinse with DI water.

Index Terms—Carrier mobility, crystallinity, drive current, germanium, nitrogen passivation

I. INTRODUCTION

The use of silicon (Si) in the semiconductor industry will soon reach a physical barrier due to drive current saturation in scaled Si metal-oxide-semiconductor field-effect transistors (MOSFETs). To address this challenge, the International Technology Roadmap for Semiconductors (ITRS) suggests replacing the strained silicon MOSFET channel with an alternate material offering higher quasi-ballistic carrier velocity and mobility than strained silicon [1]. By using germanium (Ge), a semiconductor with higher carrier mobility for both holes and electrons as well as greater source injection velocity, these scaling bottlenecks can be overcome and allow for the continual advancement of device technology approaching 16 nm and beyond. In this situation, Ge substrates can provide maximum drain saturation current while providing sufficient electrostatic control so that short-channel effects can be suppressed [2]. Through the processing of MOS capacitors on Ge and Si, one can see how substrate material impacts overall device performance and how Ge devices are advantageous in terms of greater voltage output and faster device speed. This work will lead to Ge device research and education at RIT and in turn for the continuation of device scaling and ease forward progress for the semiconductor industry as a whole.

II. THEORY

A. Material Differences

The use of Ge is a logical upgrade from Si in that it is another Group IV element, meaning it has the same number of valence electrons as silicon and thus will have some of the same physical and chemical behaviors as silicon. While the two elements are comparable to a certain extent, there exist vast differences as seen in Table I below:

<table>
<thead>
<tr>
<th>Properties</th>
<th>Symbol</th>
<th>Ge</th>
<th>Si</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap at 300 K</td>
<td>$E_g$</td>
<td>0.66</td>
<td>1.12</td>
<td>eV</td>
</tr>
<tr>
<td>Breakdown E-field</td>
<td>$E_{BD}$</td>
<td>$\approx 10^4$</td>
<td>$\approx 3 \times 10^4$</td>
<td>V/cm</td>
</tr>
<tr>
<td>Drift mobility (electron)</td>
<td>$\mu_e$</td>
<td>3900</td>
<td>1500</td>
<td>cm²/V·s</td>
</tr>
<tr>
<td>Drift mobility (hole)</td>
<td>$\mu_h$</td>
<td>1900</td>
<td>450</td>
<td>cm²/V·s</td>
</tr>
<tr>
<td>Effective mass (electron long.)</td>
<td>$m_{el}$</td>
<td>1.64</td>
<td>0.98</td>
<td>—</td>
</tr>
<tr>
<td>Effective mass (electron trans.)</td>
<td>$m_{et}$</td>
<td>0.082</td>
<td>0.19</td>
<td>—</td>
</tr>
<tr>
<td>Effective mass (heavy hole)</td>
<td>$m_{hh}$</td>
<td>0.044</td>
<td>0.16</td>
<td>—</td>
</tr>
<tr>
<td>Effective mass (light hole)</td>
<td>$m_{lh}$</td>
<td>0.28</td>
<td>0.49</td>
<td>—</td>
</tr>
<tr>
<td>Intrinsic carrier concentration</td>
<td>$n_i$</td>
<td>$2.4 \times 10^{10}$</td>
<td>$9 \times 10^{10}$</td>
<td>cm⁻³</td>
</tr>
<tr>
<td>Melting point</td>
<td>—</td>
<td>937</td>
<td>1415</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal conductivity at 300 K</td>
<td>$k_d$</td>
<td>0.6</td>
<td>1.5</td>
<td>W/cm·°C</td>
</tr>
<tr>
<td>Abundance in Earth's crust</td>
<td>—</td>
<td>1.5 x 10⁶</td>
<td>27.7</td>
<td>%</td>
</tr>
</tbody>
</table>

There are numerous benefits to using Ge in the channel region of transistors, as enumerated below:

- Lower effective masses for longitudinal electrons, heavy holes, and light holes are primarily responsible for higher drift mobility values
- A smaller bandgap at room temperature is more compliant with supply voltage scaling as specified by ITRS
- The lower melting point of Ge reflects a possibility to fabricate MOSFETs with much lower thermal budget processes than are currently being utilized in industry

While Ge has many valuable properties, it also has certain characteristics that are disadvantageous when compared to Si—these are detailed below:

- The breakdown of electric-field in Ge is much lower which could be a concern for deeply scaled or high voltage Ge devices
- Higher carrier concentration and lower thermal conductivity values could be problematic with regard to
heat dissipation in integrated circuits that are already heavily tasked.

- While Si is the second-most abundant element in the Earth's crust, Ge makes up only 1.5 parts per million and is thus a much more expensive material.

B. Material Cost Analysis

As was previously mentioned, the discrepancy in abundance of Ge in comparison to Si leads to an extreme cost differential between the two elements. While hyperpure silicon (i.e., of greater than 99.99% purity) costs somewhere between $0.25 and $0.40 per gram, the cost of Ge of equivalent purity is about $3 per gram. Because of this increase, alternative methods have been explored to reduce transistor critical dimensions.

One such method is double patterning, a class of photolithography methods designed to enhance feature density. This technique has proven to be challenging, however, for several reasons. Most importantly, tool throughput is reduced when double patterning is employed because the same pattern requires multiple passes to be fully printed. Another glaring problem is that the yield of a double patterning process can be expected to be lower because the overall yield then becomes the product of the overlay yield, first mask yield, and second mask yield together.

Another option that has been explored is extreme ultraviolet lithography (EUVL), which uses a 13.5 nm wavelength as the irradiation source. The problem with this lithography technology, however, is that it is not fully developed for production; because of this, it cannot compete with 193 nm immersion lithography, an established process for industry. Intel, the largest semiconductor company in the world, has set the tone for the semiconductor industry by stating that they will not be using EUVL in their upcoming 22 nm production line due to its inadequacy at this time; instead, they will continue working with immersion lithography.

C. Oxides on Germanium

Use of silicon dioxide (SiO₂) has been common practice in the semiconductor industry for its dielectric properties. Recently, however, the negative effects of shrinking critical dimensions have been noticeably increasing. Below the 2 nm threshold for oxide thickness, one can begin to see drastic increases in tunneling effects which in turn leads to higher amounts of leakage currents. This effect can then lead to such issues as excessive power consumption in devices and reduced device reliability [7]. For this reason, new materials have been explored to allow for improved performance without the need for such small dielectric layers. These compounds, known as high-κ materials, allow for increased gate capacitance without having leakage problems seen with older products.

These materials are especially important when using a germanium substrate as the native oxide formed on germanium (GeO) is very volatile and easily desorbed, thus making it very difficult to control the dielectric/germanium interface. This instability also leads to a large amount of interface states which will hinder device performance [7]. For this reason, high-κ dielectrics are essential for use on germanium substrates as they will stabilize both interfaces of dielectric films and metals with germanium. Their addition to MOS devices should provide excellent device control and aid in the desired enhancement.

D. Simulations

Fig. 1 illustrates through simulation how the use of Ge in the channel region of a transistor impacts device performance. By modeling a PMOS transistor with SiGe in the channel region, one can alter the percentage of Ge present in order to show how drive current changes:

![Fig. 1. Id vs. Vgs curves of simulated data for increasing amounts of Ge in channel region.](image)

The figure above shows a distinct increase in drive current as the concentration of Ge is augmented, thus demonstrating how Ge can greatly enhance electrical properties when used in place of Si.

III. Procedure

As was previously mentioned, two different surface treatments for the Ge substrates were implemented. The first involved NH₃ immersion at 560°C for one minute in an LPCVD system prior to oxidation—this preparation should create an amorphous oxide layer. The second treatment, consisting of a one minute deionized (DI) water rinse, should instead lead to the formation of a crystalline dielectric.

Following their respective surface treatments, the Ge samples were loaded into the deposition tool and underwent a 15 minute reactive sputter of hafnium oxide and a 30 minute sputter of molybdenum before being patterned and tested. The full process flow can be found below in Fig. 2:
A. Atomic Force Microscopy (AFM) Results

In order to characterize the planarity of the hafnium oxide sputtered onto the Ge surfaces, AFM was utilized. Fig. 3 below shows the results obtained following the deposition – (a) represents the DI water treatment results and (b) shows the nitrogen passivation results. As can be seen from the figures, the DI water treatment had greater surface uniformity with a maximum variation of 5 nm. The nitrogen passivation, on the other hand, led to more variance in surface roughness with a maximum variation of 200 nm. This deviation suggests an undesirable non-planar interfacial layer that could negatively impact the device behavior [4]:

B. X-Ray Diffraction (XRD) Results

X-ray diffraction, the second surface analysis performed, was used to characterize the crystallographic structure of the hafnium oxide layer. Fig. 4 shows the results obtained following the deposition – (a) represents the DI water treatment results and (b) shows the nitrogen passivation results. Following testing, the hafnium oxide was reported to exist in three polymorphic phases: tetragonal, cubic and orthorhombic phase. Unlike the predicted outcome, however, the DI water surface treatment did not lead to a crystalline dielectric film. Instead, the method resulted in similar properties to the amorphous layer created with a nitrogen surface passivation as indicated by the lack of peaks throughout the curves below:

![Fig. 3. AFM results showing surface roughness of Ge samples with DI water surface treatment (a) and nitrogen passivation (b) prior to oxidation.](image)

![Fig. 4. XRD results showing amorphous state of the high-K dielectric layer on Ge samples with with DI water surface treatment (a) and nitrogen passivation (b) prior to oxidation.](image)
C. Capacitance-Voltage (CV) Results

Following analysis of the hafnium oxide surface, the CV characteristics of the Ge samples were examined through the use of mercury probing. As can be seen from Fig. 5 below, the Ge devices did not perform as expected when first tested:

\[ C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{t_{ox}} \Rightarrow t_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{C_{ox}} \quad (1) \]

\[ EOT = \frac{\varepsilon_0 \varepsilon_{SiO_2} A_{Hg}}{C_{HgO}} = \frac{(3.9)(8.854 \times 10^{-14} \frac{F}{cm})(0.0053 \frac{cm}{cm^2})}{3.5nF} = 5.23 \text{ nm} \]

As can be seen from the equation above, the effective thickness was extracted to be 5.23 nm in comparison to the 17.7 nm of hafnium oxide deposited. This shows how the high-κ dielectric serves as a better film than that of silicon oxide.

D. Further Processing

Upon further processing of the devices, various issues were encountered, particularly with etching. The wet etch chemistry used did not properly remove the molybdenum and so, upon stripping photoresist, the capacitor patterns no longer remained. Following this, the wafers had another layer of molybdenum deposited and were patterned once again. For the second test, a plasma etch was used to remove metal. Upon testing of the completed capacitors, however, the capacitance values obtained were constant. These results suggest oxide was no longer present on the wafers, possibly due to the high power used in the metal deposition step which destroyed the hafnium oxide to the point where it was an ineffective dielectric.

V. Conclusion

Upon completing experimentation, much was learned regarding MOS devices on Ge and how surface treatments affect performance. It was found that Ge surface treatments prior to oxidation do not impact the crystallographic structure of the oxide layer as expected and that nitrogen passivation increases surface roughness, thus causing greater variation across wafer surface. With this in mind, however, more extensive testing is needed to understand each processing step affects Ge performance. In particular, future work should be completed with regard to hafnium oxide deposition on Ge and what thermal treatment steps are needed to optimize Ge device performance as a whole.

ACKNOWLEDGMENT

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REFERENCES

Fabrication of an Esaki Tunneling Diode by Proximity Rapid thermal diffusion

Sankar Krishnan, Student, Rochester Institute of technology

Abstract—Tunnel diodes need degenerately doped junction to optimum performance. They are fabricated using the Molecular Beam Epitaxial method. This method yields good degenerately doped junctions. However it is not clear whether the process can be used with 300 mm wafer technology due to the demand for a high thermal budget. Proximity Rapid Thermal Diffusion (PRTD) uses the RTP tool for its thermal processing. The amount of time used for the processing is in seconds which yields to a low thermal budget. Moreover RTP tools are a common place in the industry and hence comparatively, PRTD is easy to integrate into the wafer fabrication process. Tunneling diodes are fabricated using the proximity diffusion technique where a dopant is diffused from a source wafer to a device wafer in a RTP chamber. The resulting devices yielded PVCR of 2.1 and a current density of 160 mA/cm² at 300K. The performance of this device is better than the device which was fabricated before at 850 °C. This paper discusses the process flow and the results of the fabricated devices.

Index Term - Tunneling, Tunnel diode, Peak to valley current ratio(PVCR), Spin on Glass(SOG), Proximity Rapid thermal diffusion (PRTD)

I. INTRODUCTION

Tunneling diodes employ the quantum mechanical effects of tunneling for their operation. They offer lower leakage current and faster switching speeds compared to normal diodes.

The proximity rapid thermal diffusion process is a method by which dopants are transferred from a source wafer to a device wafer at a certain temperature and ambient. The dopant, in the form of spin on glass is spun on the wafer and cured. This is placed facing the source wafer separated by a spacer usually at a distance of 300 um. Due to the heat the dopant gets transferred from the source wafer to the device wafer. The process is carried out in a Rapid thermal anneal chamber.

The rapid thermal anneal process is used commonly in the industry today. After the ion implantation process, wafers are usually undergo rapid thermal anneal to anneal the damaged lattices in the silicon structure.

Tunneling diodes are usually fabricated by Molecular beam epitaxy. This process is very efficient in providing the degenerately doped profile of the tunneling diode. But this process is not feasible with 300mm wafer technology and is very cost consuming. PRTD, on the other hand is very cost efficient, using only the RTA chamber and requires low thermal budget.

But however the PRTD is influenced by a number of factors such as heating rate, cooling rate, ambient flow rate and source preparation to name a few. There is also no technique which allows to measure the amount of dopants transferred during the process.

II. THEORY

A. Tunnel Diode

Tunnel diodes are diodes which have a negative resistance region in the forward bias mode and have very high switching speed in the GHz range. The diode works on the principle of Quantum mechanical principle of tunneling. If the doping characteristic of a diode is very high, a thin depletion region results in the flowing of the majority carriers through the thin depletion region, even if the potential barrier across is greater than the kinetic energy of the particle.

Figure 1: Tunnel diode I-V curve

Figure 1 shows the I-V characteristics of a tunnel diode. As the voltage increases, the current increases as is usual with a normal p-n junction diode. But after a point, as the voltage increases, the current starts to decrease. After a point, as the voltage increases, the current again starts to increase. The region where the current decreases as the voltage increases is called the negative differential resistance region of the tunnel diode. This is a characteristic unique to tunnel diodes.
The tunnel diode is degenerately doped so that abrupt junctions are created. An ideal junction for a tunnel diode is 10nm. Figure 2 shows the band diagram under various biasing conditions of the tunnel diode. Fig 2.2(a) shows the diode under negative potential or reverse bias. In this condition, the electrons from the occupied states from the p-side tunnel to the n-side giving a negative current. Under zero biased condition, no tunneling take place and as a result no current is present. This is shown in fig 2.2 (b). Fig 2.2(c) shows the diode under small forward bias. In this condition, the electrons from the n-side conduction band tunnel into unoccupied sites of the p-side valence band. As the conduction and valence band uncross, the tunneling decreases leading to a decrease in current as shown in fig 2.2 (d). As the applied potential exceeds the built in potential, normal diffusion current of the diode takes over and the current increases once more.

B. Proximity Diffusion

Proximity diffusion is carried out in a rapid thermal anneal chamber. Proximity diffusion is similar to the CVD process but unlike CVD, the dopants are obtained from a source wafer rather than gasses flown into the chamber. The tungsten halogen lamps emit the ultraviolet radiation which is readily absorbed by the silicon wafer. As a result the silicon wafer heats up. This heating causes the diffusion of the dopants from the source wafer to the device wafer.

This diffusion technique relies heavily on the preparation of the silicon on glass sample. The diffusion properties of the SOG are affected by the thickness, cure time and cure temperature. The SOG is spun on the source wafer and cured at a certain temperature. Studies have shown that optimum diffusion occurs with thicker SOG layers and hence it is cured at 200C. There are two methods to measure the temperature inside the chamber. The two methods are by attaching a thermocouple to the back of the silicon wafer or by a pyrometer. A thermocouple is ensures accurate readings at a cost and thermal budget while a pyrometer is cheap but does not ensure accurate reading.

III. Procedure

The Esaki diodes were fabricated on a Six inch wafer which already had a high n-doping of the 1E19 cm⁻³ and 1 milliohm resistivity. One six inch p-type wafer was used as a source wafer. Phosphorically was used as an n-type dopant source and Borofilm was used as a p-type dopant source.

At first the source wafer was prepared. The Source wafer was cleaned. At first the Phosphorically was coated on the wafer. The coating was done at 3000 rpm for 40 seconds on the manual coater. The wafer was then cured for 20 minutes inside the Blue M oven at 200C. During this time, the device wafer was cleaned with HF to remove any surface oxide.

The RTA needed to be optimized to make sure the temperature was achieved as fast as possible and at the same time it didn’t overshoot a lot. After the source wafer was taken out of the oven it was cleaved into 4 pieces. One piece of the source wafer is placed facing down on the device wafer separated by three spacers at each corner.

The RTA process was run at the desired temperature for 1 second. Following the RTA run, the source wafer was removed and the just the device wafer was run for the drive in process for 90 seconds. Following this, another source was prepared with the Borofilm dopant source. The bottle was warmed and the wafer was coated with the solution at 3000 rpm for 40 seconds, following by the curing process at 200C for 20 minutes. The device wafer was again dipped in HF for 30 seconds to remove any native oxide. The source was broken into 4 pieces and one piece was placed facing down on the device wafer, separated by spacers. The process was run for 1 sec at the desired temperature.

After the diffusion was carried out in the RTA, the wafers were cleaned with HF (50:1) in the wet bench and prepared for aluminum deposition. The CVC evaporator was the tool used for the deposition of aluminum. The source wafer was loaded with aluminum and placed inside the chamber. The wafers were placed inside the chamber and the pump down for vacuum was initiated. The pressure was allowed to go to 2.4E-7 torrs. Following this the filament was heated to melt the aluminum. 2000 Angstroms of aluminum was deposited.

The aluminum deposition was followed by photolithography. The Karl Suss 6" mask aligner was used for the photolithography step. HPR 504 wafer was coated on the wafer at 3000 rpm for 45 seconds. The wafer went through pre bake at 90C for 60 seconds. Exposure dose of 115 mj/cm² was required. The exposure was run for 16 seconds followed by post exposure bake at 115 c for 60 seconds. The photoresist was then developed with CD-26 developer followed by a bake at 120C for 120 seconds.

The wafer was placed in the Al etch bath to remove the aluminum from exposed areas. The photoresist was stripped.
of and then placed in the dry tech quad to etch into the silicon to isolate each device.

The recipe used for etch contained 4 cc flow of SF6 and 16cc flow of CHF3. The pressure was 100mT and the power was 100w. The recipe was run for 65 seconds.

Following table shows the process splits used.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Phosphorous diffusion</th>
<th>Phosphorous Drive</th>
<th>Boron Diffusion</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>850 C, 1 Sec</td>
<td>850 C, 90 Sec</td>
<td>850 C, 1 Sec</td>
</tr>
<tr>
<td>2</td>
<td>900 C, 1 Sec</td>
<td>900 C, 90 Sec</td>
<td>900 C, 1 Sec</td>
</tr>
<tr>
<td>3</td>
<td>950 C, 1 Sec</td>
<td>950 C, 90 Sec</td>
<td>950 C, 1 Sec</td>
</tr>
</tbody>
</table>

Table 1: Process splits used

IV. RESULTS AND ANALYSIS

IV Curve

![IV Curve](image)

Figure 3: 30umx30um Esaki Diode with a PVCR of 2.029

Fig. 3 shows the characteristic I-V curve of an Esaki Diode with a PVCR of 2.029. The current density of this diode was 0.113 A/cm². The peak voltage of this device is 0.06 volts.

Figure 4 shows the PVCR of the different devices measured. It is seen that as the PVCR decreases, the current density decreases.

Figure 5 shows the area where the working Esaki tunneling diodes were found. The area where the quarter source wafer placed is also shown.

Figure 6 shows the measurement of the Esaki Tunneling diodes. The metal adhesion in the area above it was not good and hence the metal came out. But it is seen that as the dies move farther away from the top, the PVCR decreases exponentially.

The variation in the PVCR of the diodes is attributed to the gas flow inside the chamber. Due to the gas flow some of the dopants, while diffusing from the source wafer to the device wafer got carried away in the ambient and got deposited elsewhere. To understand the effect of the ambient inside the chamber, few dopant studies were carried out.
Figure 9 and 10 show the RTA drive in and diffusion temperature profile. It is very important to get the temperature high as fast as possible and cool them as fast as possible. The figures show that the ramp rate of the temperatures is good but it takes a long time for them to cool down. Also this level of repeatability was attained after a number of trials before a real run. A thermocouple was used to measure the temperature of the wafer inside the chamber. But the thermocouple gives inaccurate readings below 300 C.

V. CONCLUSION

The goal of the project was to fabricate Esaki tunneling diode and to understand the tolerances involved in fabricating such a device using PRTD. Working devices with PVCR greater than 2.0 were created at 900C temperature. However the current density was small, about 160 mA/cm². Esaki diodes created three years ago had lower PVCR but greater current density of about 3 A/cm². From this project it was revealed that the process tolerances for fabrication Esaki diodes using PVTR is very small. The map of the measured dies proves this very point. There are devices with PVCR concentrated in a small region, but as the dies go away from them, the PVCR reduces exponentially.

VI. REFERENCES

[1] Michael Suster, Darrin J. Young, and Wen H. Ko,
“Micro-Power wireless transmitter for high temperature MEMS sensing and communication and applications”
Double Patterning Technique Using an Aluminum Hardmask

Brian Lindenau

Abstract—The goal of this project was to successfully demonstrate a double patterning technique using equipment available at the SMFL at RIT. Traditional methods of increasing resolution have been essentially exhausted; therefore new methods of increasing resolution are needed. One of these new methods is double patterning, which splits a dense pattern into two less dense patterns which are imaged in two steps, thereby reducing imaging constraints. Overall a proof of concept of the double patterning process was achieved. Imaging of 0.5 μm drawn features was demonstrated, resulting in 0.3 μm post-etch.

Index Terms—double patterning, hardmask, BARC

I. INTRODUCTION

Increasing resolution in a lithographic system has been a constant goal in the semiconductor industry. Feature sizes have continued to shrink, forcing lithographic systems to adapt. Minimum resolution is determined by the Raleigh Criterion. The traditional methods of increasing resolution have been to decrease the wavelength of the radiation used, thereby creating smaller diffraction angles, or to increase the NA of the system, thereby capturing larger diffraction angles. These traditional methods of increasing resolution are approaching their limit. Reducing wavelength below 193nm to 157nm has proven to be extremely problematic. The traditional fused silica lenses used in modern lithography equipment are highly absorptive at this smaller wavelength. Also, resist systems for 157nm have yet to be developed.

Increasing NA has shown more promise, but is still approaching a limit. Increasing NA past 1 has now been made possible due to immersion systems, which is essential for future minimum feature sizes. However, these systems are new and most likely will introduce new problems. A problem that has already arisen is finding a high-index immersion liquid other than water, to boost NA even further. Also, there is a practical limit on how high the index of the immersion fluid can be, as the fluid index cannot exceed the index of the photoresist, which is typically around 1.6-1.7.

These issues with traditional methods of increasing resolution have lead to other less desirable, but possible solutions. One of these methods includes double patterning. Double patterning utilizes the relationship between duty-ratios and resolution. Imaging smaller features becomes much easier when the duty ratios are large. Unfortunately, densely packed features are still required in chip designs. Double patterning allows for higher duty-ratios and still results in densely packed features. This is accomplished by splitting densely packed features with duty-ratios near 1:1 into two different mask sets, with duty ratios of 1:3. The wafers are then exposed and patterned twice, the first pattern of 1:3 features, followed by the second pattern of 1:3 features, which are placed in between the first set of features. This creates a set of densely packed features, without having to image them all at the same time, thereby effectively increasing the resolution of the system. This can be proven by utilizing Eq. 1, known as the Rayleigh Criterion. Essentially, this technique allows for $k1$ values less than 0.25.

$$h P_{min} = \frac{k_1 \lambda}{NA} \tag{1}$$

Currently, there are many different double patterning techniques, and they are generally divided into two separate categories: processes using a single etch step, and processes using two etch steps. The latter technique was used in this experiment.

The target layer for the double patterning process is the polysilicon gate layer. This layer typically has the smallest and most critical features in a CMOS process. The process uses a single hardmask of aluminum, in which the first pass pattern is transferred. Aluminum was selected for the hardmask material for several reasons. Aluminum has been a common material in semiconductor manufacturing, and deposition and etching techniques are well developed and characterized. Also, from MEMS applications, aluminum is known to have high selectivity in common silicon etch chemistries (~300:1). However, using aluminum has significant challenges. The reflectivity of the material created the first challenge that needed to be addressed, due to the standing wave effects and resist thickness sensitivity it created. A bottom anti-reflective coating (BARC) from Brewer Science, Inc. was utilized to mitigate this issue.

Another challenge arose from the fact that aluminum etch processes typically have not been developed for the critical feature sizes needed for the gate layer.
II. PROCEDURE

The general process flow is illustrated in Fig. 1. The process begins with the film stack for the polysilicon gate layer. From here, a thin layer of aluminum is deposited (1000 Å). The first pass lithography is then performed, and the resulting pattern is transferred to the underlying aluminum layer. After the aluminum is etched and the resist is removed, the second pass lithography is performed. Finally, both passes are etched into the underlying polysilicon layer to achieve the final pattern. The photoresist and aluminum are then stripped from the wafer, leaving only the poly pattern. For a detailed process flow please see the attached table.

III. RESULTS

A. BARC simulation

A BARC form Brewer Science (i-CON 16) was utilized for this process. The performance of the BARC was simulated using Prolith lithography simulation software. A basic swing curve (resist thickness v. reflectivity) was created for two scenarios: with and without 1600 Å of BARC. These simulations were completed for both passes of lithography, since both passes have reflective substrates. The results of these simulations are shown in Figs. 2 and 3. The purple lines are for no BARC, and the green lines are with the BARC. The results show a significant improvement in reflectivity in both cases. The amplitude of the swing curve for the first pass was reduced from 0.34 to 0.01, and the amplitude for the second pass was reduced significantly as well.

B. First Pass Lithography

Imaging of 0.3 µm drawn features was achieved in the first lithography step, as well as 0.5 and 1 µm drawn features. An optical image of the results is shown in Fig. 4. The primary challenge in this step was achieving the correct focus and exposure settings for the imaging step. This was done using focus/exposure arrays, which were qualitatively evaluated. The optimum settings were found to be a dose of 320 mJ, and a focus setting of +0.2 µm.
C. BARC etch

The BARC used in this process was not wet-developable, therefore an etch process was developed to etch the thin BARC layer before attempting the aluminum etch. This etch was performed in the LAM 490, using a chemistry of 10 sccm of O2 and 100 sccm of SF6. The etch rate was found to be ~50 Å/sec, with minimal resist erosion.

D. Aluminum etch

The aluminum etch for this process was adapted from an existing aluminum etch recipe meant for much thicker films (~0.75 μm). The etch rate proved to be extremely slow for the first several attempts for an unknown reason. One possibility was an increase in the thickness of the native aluminum oxide “skin” on the surface of the aluminum film, which may have been caused by exposing the aluminum surface to an oxygen ambient during the BARC etch. Another possible cause in the differing results for the thinner film could be an unknown acceleration of the etch rate during the etch process. This effect was finally compensated for by increasing the time of the first stage of the etch, which is the portion of the etch recipe meant to break through the aluminum oxide skin. Also, the etch time for the second stage of the etch was also significantly increased. This resulted in a complete aluminum etch. The 0.3 μm drawn lines were still intact after the aluminum etch. An optical image of the aluminum lines post-etch and after resist strip is shown in Fig. 5.

E. Second Pass Lithography

Optimal imaging settings were found using the same approach as the first pass, which used focus/exposure arrays and a qualitative assessment. The imaging of the 0.3 μm drawn lines was not achieved during the second pass. Possible reasons for this include optical proximity interactions with the aluminum lines in between the imaged features, topography issues, and BARC dishing in between the aluminum lines. Future process optimizations may or may not improve imaging capabilities of this step. An optical image of the 0.5 μm drawn lines are shown in Fig. 6.

The primary concern in the second pass lithography step was overlay; however, this proved to be the parameter that gave the least amount of difficulty. The results of the overlay errors were immeasurably small using 0.1 μm verniers. A high-magnification image of these alignment verniers is shown in Fig. 7.
F. Polysilicon etch

The polysilicon etch proved to be the most difficult part of the process. The etch was first attempted on the LAM 490, using an existing recipe intended for etching a 4000 Å poly film, which was the thickness of the poly used in this experiment. The results of this etch showed complete hardmask erosion, as well as resist undercutting for all feature sizes below 1 μm. The use of the LAM 490 for this etch was abandoned.

The Drytek Quad RIE system was utilized instead, as well as a poly etch recipe already adapted for a RIT factory process. The results of this etch was mixed. Most patterns showed signs of hardmask lifting, and some erosion. An example of this lifting is shown in Fig. 8. All 0.3 μm drawn patterns were completely eroded, and most 0.5 μm features were successfully transferred from the second pass imaging, however the hardmask for these patterns were shifted or completely lifted. Both passes of some 0.5 μm patterns were transferred intact. An example of these patterns is shown in Fig. 9.

G. SEM images

The pattern shown in Fig. 9 was also observed using a SEM, and is shown in Figs. 10 and 11. The images show that the 0.5 μm drawn lines became 0.3 μm poly lines after etch. The images also show a significant feature integrity difference between the lines protected with photoresist, and those protected by the aluminum hardmask. The hardmask-protected features show some damage and line edge roughness. In Fig. 11, the evidence of shifting hardmask features is clearly seen. Also, the CD error from pass-to-pass appears to be very minimal.
IV. CONCLUSION

Overall, a proof of concept of a double patterning process using aluminum as a hard mask was achieved. Imaging of 0.5 μm drawn features was achieved with little to no overlay error, with a final CD after etch of 0.3 μm. Significant improvements can still be made to this process, specifically in the etch steps. The results show that a double patterning process is achievable at RIT.

REFERENCES


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<th>Action</th>
<th>Tool</th>
<th>Process details</th>
</tr>
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<td>CVC 601</td>
<td>1000 W&lt;br&gt;450 secs&lt;br&gt;5 mT&lt;br&gt;Target thickness: 1000 A</td>
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<td>Spin on BARC</td>
<td>CEE Hand Coater</td>
<td>2500 rpm&lt;br&gt;60 sec</td>
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<td>3</td>
<td>Post-application bake</td>
<td>Hotplate</td>
<td>180&lt;br&gt;60 sec</td>
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<td>Coat with resist</td>
<td>SSI Track</td>
<td>Recipe: coat&lt;br&gt;10000 A thickness</td>
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<td>Expose 1st pass</td>
<td>Canon Stepper</td>
<td>Recipe: arandall_nwell&lt;br&gt;320 ml&lt;br&gt;+0.2 um</td>
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<td>Develop</td>
<td>SSI Track</td>
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<td>Etch BARC</td>
<td>LAM 490</td>
<td>Recipe: ash&lt;br&gt;35 secs&lt;br&gt;325 mT&lt;br&gt;140 W&lt;br&gt;10 sccm O2&lt;br&gt;100 sccm SF6</td>
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<td></td>
<td></td>
<td>LAM 4600</td>
<td>Stage 1: 15 secs&lt;br&gt;250 W&lt;br&gt;25 sccm N2&lt;br&gt;100 sccm BCI3&lt;br&gt;10 sccm Cl2&lt;br&gt;15 sccm CFORM</td>
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<td></td>
<td></td>
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<td>Stage 2: 70 secs&lt;br&gt;125 W&lt;br&gt;40 sccm N2&lt;br&gt;50 sccm BCI3&lt;br&gt;60 sccm Cl2&lt;br&gt;15 sccm CFORM</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>Stage 3: 10 secs&lt;br&gt;125 W&lt;br&gt;50 sccm N2&lt;br&gt;50 sccm BCI3&lt;br&gt;45 sccm O2&lt;br&gt;15 sccm CFORM</td>
</tr>
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<td>8</td>
<td>Etch aluminum</td>
<td>LAM 4600</td>
<td>Recipe: ash&lt;br&gt;35 secs&lt;br&gt;325 mT&lt;br&gt;140 W&lt;br&gt;10 sccm O2&lt;br&gt;100 sccm SF6</td>
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<td>9</td>
<td>SRD</td>
<td>SRD</td>
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<td>10</td>
<td>Ash resist/BARC</td>
<td>Branson Asher</td>
<td>Recipe: hardash</td>
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<td>11</td>
<td>Spin on BARC</td>
<td>CEE Hand Coater</td>
<td>2500 rpm&lt;br&gt;60 sec</td>
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<td>Post-application bake</td>
<td>Hotplate</td>
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<td>13</td>
<td>Coat with resist</td>
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<td>14</td>
<td>Expose 2nd pass</td>
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<td>Develop</td>
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<td>Recipe: develop</td>
</tr>
<tr>
<td>16</td>
<td>Etch BARC</td>
<td>LAM 490</td>
<td>Recipe: ash&lt;br&gt;35 secs&lt;br&gt;325 mT&lt;br&gt;140 W&lt;br&gt;10 sccm O2&lt;br&gt;100 sccm SF6</td>
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<td>17</td>
<td>Etch Poly</td>
<td>Drytek Quad</td>
<td>Recipe: facopoly&lt;br&gt;225 secs&lt;br&gt;190 W&lt;br&gt;40 mT&lt;br&gt;30 sccm SF6&lt;br&gt;10 sccm CHF3</td>
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<td>18</td>
<td>Ash resist/BARC</td>
<td>Branson Asher</td>
<td>Recipe: hardash</td>
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<tr>
<td>19</td>
<td>Strip aluminum</td>
<td>Aluminum etch</td>
<td>30 secs, or until visibly removed</td>
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<tr>
<td>20</td>
<td>SRD</td>
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Process Development for the Fabrication of a Double-Sided Photodiode

Kimberly E. Manser

Abstract—Given a cross-section and functionality requirements for a photodiode designed for application as the focal plane array on SNAP (SuperNova Acceleration Probe), a proposed satellite in the Joint Dark Energy Mission by NASA and the DOE, a process has been developed to fabricate the device in the most efficient and reliable manner. The photodetector is to be hybridized with a ROIC (Read-Out Integrated Circuit) that interprets the individual pixel signals and converts the electrical information into an image. After several versions of the process based on simulations, efficiency of sequence, and research, a test run of key process steps was completed to evaluate chosen process values and their final results, including well profile and I-V characteristics. The results from the test run were used to create a preliminary process flow for device wafer fabrication. The process was implemented in full on a small lot of device wafers with some monitor wafers, with the entire process (not including test) requiring about 100 hours. The results from this device run were used to create a new revised version of the process flow in order to attain better functionality from the device. After this device run was completed, the results were analyzed and used to update the process flow again to address deficiencies in the resulting devices and processing difficulties.

Index Terms—Photodetector, ROIC, Dark Current, Diode Ideality

I. INTRODUCTION

SNAP (SuperNova Acceleration Probe) is a deep space observatory that will measure the expansion of the universe by tracking supernova as markers. This information will also help scientists understand the nature of dark matter and its role in the acceleration of the expansion of the universe. It is a part of the Joint Dark Energy Mission (JDEM), included in the Beyond Einstein program: an initiative by the scientific community to better understand the universe. The photodetector described here will act as the focal plane array for this observatory in its final revision. Fig. 1 above shows a final cross-section of the device. The bump bonding sites will be the point of communication between the detector pixels and the ROIC circuit. The backside of the wafer has a metal frame to introduce a bias across the whole wafer via a heavily doped region of silicon. Fig. 2 shows the top-down views for both the front and back of the wafer. There is a metal grid that runs between the pixels which will act as a field effect gate to decrease cross-talk between the pixels by creating a slightly N-type accumulation. The design of the device stipulated that there was to be minimal shadowing (which implies that the metal layer must be tightly controlled), the implant well junctions were to be less than a micron each (more specifically, less than 0.75μm for the n-well and less than 0.5μm for the p-well), and the pixel pitch was 15μm. The surface concentration of the wells was to be also aggressively high to make a good ohmic contact between the silicon and the aluminum: 1x10^18 cm^-3 for the N+ implant and 1x10^19 cm^-3 for the P+ implant. The goal for the dark current (the limiting factor in the resolution of the resulting image) was 0.1 nA/cm² at the operating conditions for the device (200K at a 50V reverse bias), which translates to 150 nA/cm² at the testing conditions of 300K with the same bias.

II. CHALLENGES AND SOLUTIONS

A. "Backside" Contamination

In normal CMOS fabrication, the devices are made on only one side of the wafer, and while the backside of the wafer is exposed to contaminants and vulnerable to scratching, this is generally ignored (and perhaps encouraged to aid in gettering). For the fabrication of this device, however, the backside must be as device-ready as the front side. To make sure that both sides of the wafer remain pristine as possible, protective coatings, proximity bakes, and careful sequencing were used so that neither side the wafer was ever subjected to the contamination usually seen by a standard CMOS process wafer.
B. Limited Thermal Budget

Due to the need for shallow junctions (to decrease surface recombination velocity, a parasitic that decreases the signal to noise ratio in a photodiode), little to no diffusion of the implanted species could occur. Since this diffusion occurs at high temperature (like temperatures seen during thermal oxide growth steps), these high temperature steps were eliminated as much as possible. Since the final device requires an anti-reflective layer (silicon dioxide) 5000Å thick, the decision was made to use LTO for the majority of the film thickness, but still grow 100Å of thermal oxide for a good interface between the oxide and the silicon. These oxide growths also served to activate the implanted species since they occur after each implant step in the process flow. Rapid thermal anneals were also done after the implants to anneal out damage due to implant.

C. Front to Back Alignment

Double-sided alignment is a challenge at RIT due to the availability of tools only designed for single-sided alignment. A process needed to be found that would facilitate the alignment of the front die and the back die to within a reasonable shift. Alignment was done by first aligning the side that would not be exposed to a mask, then affixing the wafer to the mask by using water droplets to create adhesion. The wafer and mask were then flipped, and the second mask was aligned to the first mask by use of marks outside the design area and the backside of the wafer was exposed, now aligned to the front side.

D. Selectivity / Over-Etching

Because the implanted wells are so shallow, selectivity and over-etching became an issue. Dry etching is more anisotropic, which leads to better contact etching, but has poorer selectivity, meaning that the etching gases will not stop on the desired layer. Instead, they will continue into the silicon layer after etching the oxide layer and consume the highest doped portion (the surface) of the doped well. End point detection can be used to gauge the transition from oxide to silicon by monitoring the spectra emitted in the chamber, but slight over-etching would result in dopant loss and poorer contacts, which result in more parasitic resistance and poorer device performance. For these reasons, wet etches, though isotropic in nature, were chosen for their selectivity (ratio of more than 500:1) and therefore reliability.

III. SIMULATIONS

Once a preliminary process flow had been completed, simulations were done using Silvaco Athena to ensure that assumptions that were made incurred good results (as per the goals listed previously). The entire process was simulated save for the passive steps (such as RCA cleans) and then the final well profiles were analyzed to determine the defining characteristics. Fig. 3 shows the front and back-side well profiles (P+ and N+, respectively).

As seen in the figure, the surface concentrations are correctly obtained, but the junction depths are about 0.25µm too deep. Since all of the thermal steps had already been reduced and the P+ implant species changed from B11 to BF2 (for shallower initial junction), these values were deemed acceptable and the project moved forward, knowing that the goals were aggressive to begin with. Should the simulations prove correct at the end of fabrication, more steps would be taken to decrease them.

IV. TESTING RUN

A truncated version of the full process (which excluded photolithography steps and metal layers) was run to verify that the designed process parameters would result in the desired junction depths and sheet resistance of the implanted areas.

Blanket implants were used for ease of testing, and all of the thermal steps were included to achieve the most accurate profiles. The testing wafers were characterized using a groove and stain method to record junction depth and a four-point probe measurement was used to procure the sheet resistance of the implants. After completion of the truncated fabrication, some of the process values needed adjustment, and so changes were made to the process and then verified. These changes included phosphorus implant dose, boron implant screening oxide thickness, and deposition time for the LTO steps based on a newly calculated deposition rate. Fig. 4 to the left shows a generalized process flow for the device fabrication.
V. Device Fabrication and Results

A. Fabrication

The device run was done with three device wafers and two monitors (one for implant measurements and one to monitor metal deposition). There were 55 steps total in the last version of the process, requiring approximately 96 tool hours. During the course of fabrication, there was a problem with LTO uniformity, even though the testing run had much better quality of oxide with the same settings. This led to difficulties in etching the films, which then led to a degradation of the surface (scratches and plasma damage), which would then affect device performance.

B. Results

A series of tests were done on the implant wafer and device wafers to ascertain well profile characteristics and I-V characteristics (both reverse and forward biased). Table 1 shows the well characteristics from the implant monitor wafer. The sheet resistance and junction depth were taken as measurements, with the surface concentration derived from those two values using Irvin’s Curves.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Ideality Factor (n)</th>
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<tr>
<td>D1</td>
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</tr>
<tr>
<td>D2</td>
<td>1.26</td>
</tr>
<tr>
<td>D3</td>
<td>1.31</td>
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where \( I_D \) is the diode current, \( I_S \) is the leakage current (or dark current for a photodiode), \( V_D \) is the voltage placed on the diode, and \( V_T \) is the turn-on or threshold voltage for the device. Table 1 to the right shows the ideality factors for all three device wafers, the average being 1.31.

A reverse bias curve was also obtained from the device wafers and the data is reported below in the graph in Fig. 7.

![I-V Characteristic Curve, Reverse Bias](image)

The average dark current at a 50V reverse bias is on the order of \( 1 \times 10^{-6} \text{A/cm}^2 \), three orders of magnitude higher than the goal. This is likely due to insufficient anneals and the surface damage described earlier. There is one curve that represents one device wafer (D2) with the light on, showing that the diode functions as a photodetector.

Figures 8 and 9 show the top down views for the frontside and backside (in comparison with Fig. 2), respectively. It may be seen that while the wet etching worked sufficiently on the backside patterning (due to the relatively large and isolated features), the wet etch was not sufficient for the frontside due to the dense features and therefore resulted in over-etching of the oxide contact cuts (note the round shape as opposed to the on-mask square shape). The metal was also under-etched due to the dense features as well, resulting in larger than desired contact pads, encroaching on the metal grid pad.
VI. CONCLUSIONS AND FUTURE WORK

The process was an overall success, with the exception being the contact etching parameters. Based on results from the full process run, changes were made to increase the total tool time to 100 hours and 59 steps.

For future work, dry etches will be looked into for the contact etches. Etch rates, possible changes to the gas flows, and endpoint detection will be investigated to provide the optimum etch with minimal over-etching.

In addition to the dry etch experiments, the anneals will be optimized to decrease the damage remaining from the implant, resulting in lower dark current. Also, since the area of the test die is much larger than that of the individual pixels, the perimeter parasitics will be larger in theory. Characterization of perimeter to area ratios and the resulting dark current (for the same implants that will have the same bulk dark current) will help to eliminate the parasitics’ contribution to the dark current.

APPENDIX

Final full process flow below: (DW = Device Wafers, IMP = implant monitor, ET = metal monitor)

<table>
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<td>1</td>
<td>RCA Clean</td>
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<td>Protective Oxide Growth</td>
<td>Bruce Furnace, Tube 1, Recipe #311</td>
<td>DW</td>
<td>Oxide Thickness</td>
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<td>Coat Frontside with Photoresist</td>
<td>CEE Hand Coater, 120C for 60s</td>
<td>DW</td>
<td>-</td>
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<td>4</td>
<td>Etch Backside Oxide</td>
<td>10:1 BOE, 2 minutes (586 A/min) (be sure it pulls dry)</td>
<td>DW</td>
<td>-</td>
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<td>5</td>
<td>Remove Photoresist</td>
<td>PRS-2000 Bench</td>
<td>DW</td>
<td>-</td>
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<td>6</td>
<td>Photo 1 - Backside Alignment marks</td>
<td>Coat HMDS on CEE Hand Coater Bake at 90C for 30s Coat Resist on CEE Hand Coater Bake at 90C for 60s Expose on KarlSuss MA56 Bake at 140C for 90s Develop on CEE Hand Developer</td>
<td>DW</td>
<td>-</td>
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<td>Varian 350D Implanter, Dose = 5e14, Energy = 33keV, P31</td>
<td>DW + IMP</td>
<td>-</td>
</tr>
<tr>
<td>13</td>
<td>Strip Oxide, BOE Chemical Bench</td>
<td>HF Wetbench, 10:1 BOE, 1 minute (586 A/min)</td>
<td>DW + IMP</td>
<td>Junction Depth</td>
</tr>
<tr>
<td>14</td>
<td>Anneal</td>
<td>AG610A/B RTA, 1000C, 3 minutes</td>
<td>DW + IMP</td>
<td>-</td>
</tr>
<tr>
<td>15</td>
<td>RCA Clean</td>
<td>RCA Wetbench</td>
<td>DW + IMP</td>
<td>-</td>
</tr>
<tr>
<td>16</td>
<td>Backside Oxide Growth</td>
<td>Bruce Furnace, Tube 4, Recipe #450</td>
<td>DW + IMP + ET</td>
<td>Oxide Thickness</td>
</tr>
<tr>
<td>17</td>
<td>Backside LTO Deposition</td>
<td>LPCVD Upper Tube, 425C LTO recipe, 53 min.</td>
<td>DW + IMP + ET</td>
<td>Oxide Thickness</td>
</tr>
<tr>
<td>18</td>
<td>Backside Protection Silicon Nitride Growth</td>
<td>LPCVD Tube #2, Factory Nitride Recipe, 23 minutes</td>
<td>DW + IMP + ET</td>
<td>Nitride Thickness</td>
</tr>
<tr>
<td>19</td>
<td>Backside Photoresist Protective Coating</td>
<td>Coat Resist on CEE Hand Coater Bake at 120C for 90s</td>
<td>DW + IMP + ET</td>
<td>-</td>
</tr>
<tr>
<td>20</td>
<td>Dry Etch of Nitride on the frontside of the wafer</td>
<td>DryTech Quad, Nitride Recipe, 2.5min (stop on LTO)</td>
<td>DW + IMP + ET</td>
<td>-</td>
</tr>
<tr>
<td>21</td>
<td>Oxide Etch frontside oxide</td>
<td>HF Wetbench, 10:1 BOE, 4 min (1600 A/min, 586 A/min-Th)</td>
<td>DW + IMP + ET</td>
<td>-</td>
</tr>
<tr>
<td>22</td>
<td>Strip Photoresist</td>
<td>Branson Asher, 4&quot; Normal Ash</td>
<td>DW + IMP + ET</td>
<td>-</td>
</tr>
<tr>
<td>23</td>
<td>Photo 2 - Frontside Alignment marks</td>
<td>Coat HMDS on CEE Hand Coater Bake at 90C for 30s Coat Resist on CEE Hand Coater Bake at 90C for 60s Expose on KarlSuss MA56 Bake at 140C for 90s Develop on CEE Hand Developer</td>
<td>DW</td>
<td>-</td>
</tr>
<tr>
<td>24</td>
<td>Etch Silicon alignment marks</td>
<td>DryTech Quad, use carrier wafer, recipe &quot;polysilicon&quot;, 1.5 min</td>
<td>DW</td>
<td>-</td>
</tr>
<tr>
<td>25</td>
<td>Strip Photoresist</td>
<td>Branson Asher, 4&quot; Normal Ash</td>
<td>DW</td>
<td>-</td>
</tr>
<tr>
<td>26</td>
<td>RCA Clean</td>
<td>RCA Wetbench</td>
<td>DW + IMP</td>
<td>-</td>
</tr>
<tr>
<td>27</td>
<td>Frontside Screening Oxide Growth</td>
<td>Bruce Furnace, Tube 4, Recipe #456</td>
<td>DW + IMP</td>
<td>Oxide Thickness</td>
</tr>
<tr>
<td>28</td>
<td>Photo 3 - Frontside Well Definition</td>
<td>Coat HMDS on CEE Hand Coater</td>
<td>DW</td>
<td>-</td>
</tr>
<tr>
<td>Step</td>
<td>Process Description</td>
<td>Details</td>
<td>Notes</td>
<td></td>
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<td>------</td>
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<td>-------------------------------------------------------------------------</td>
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</tr>
<tr>
<td>29</td>
<td>Frontside Boron Well Implant</td>
<td>Varian 350D Implanter, Dose = 1e15, Energy = 33keV, BF2</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Strip Photoresist</td>
<td>Branson Asher, 4&quot; Normal Ash</td>
<td>DW</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Etch Oxide (damaged from implant) Frontside</td>
<td>HF Wetbench, 10:1 BOE, 2 minutes (586 A/min)</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Anneal</td>
<td>AG610A/B RTA, 1000C, 3 minutes</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>RCA Clean, RCA Wetbench</td>
<td>RCA Wetbench</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Frontside Oxide Growth</td>
<td>Bruce Furnace, Tube 4, Recipe #450</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>Frontside LTO Deposition</td>
<td>LPCVD Upper Tube, 425C LTO recipe, 53 min.</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>Coat Frontside with Photoresist</td>
<td>CEE Handspinner, 120C for 60s</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>Backside Oxide Etch (remove any oxide on the nitride)</td>
<td>10:1 BOE Cup Etch, 5 minute (586 A/min)</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>Strip Photoresist</td>
<td>Branson Asher, 4&quot; Normal Ash</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>Strip Backside Silicon Nitride</td>
<td>Hot Phosphorus Bench, 45 min</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>Coat Frontside with Photoresist</td>
<td>CEE Hand Coater, 120C for 60s</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>Photo 4 - Backside Contact Etch</td>
<td>Coat HMDS on CEE Hand Coater</td>
<td>DW</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bake at 90C for 30s (Proximity Bake)</td>
<td></td>
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<td></td>
<td></td>
<td>Coat Resist on CEE Hand Coater</td>
<td></td>
<td></td>
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<td></td>
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<td>Bake at 90C for 60s (Proximity Bake)</td>
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<td></td>
<td>Expose on KarlSuss MA56</td>
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<td></td>
<td>Bake at 140C for 90s (Proximity Bake)</td>
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<tr>
<td></td>
<td></td>
<td>Develop on CEE Hand Developer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>Etch Oxide (backsides contacts)</td>
<td>10:1 BOE Etch, 3.5 minutes (1600 A/min, 586 A/min)</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>Strip Photoresist</td>
<td>PRS-2000 Bench</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>Backside Aluminum Deposit</td>
<td>CVC601 Sputter, 15sccm Argon, Power = 1500W, 5mT, 930s</td>
<td>DW + ET</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>Photo 5 - Backside Aluminum Etch</td>
<td>Coat HMDS on CEE Hand Coater</td>
<td>DW</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bake at 90C for 30s (Proximity Bake)</td>
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<td></td>
<td>Coat Resist on CEE Hand Coater</td>
<td></td>
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<td>Bake at 90C for 60s (Proximity Bake)</td>
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<td>Expose on KarlSuss MA56</td>
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<td>Bake at 140C for 90s (Proximity Bake)</td>
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<tr>
<td></td>
<td></td>
<td>Develop on CEE Hand Developer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>Wet Etch of Backside Aluminum</td>
<td>Aluminum Etch Bench, 1 minute 20 seconds</td>
<td>DW + ET</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>Strip Photoresist</td>
<td>PRS-2000 Bench</td>
<td>DW</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>Backside Photoresist Protective Coating</td>
<td>CEE Hand Coater, 120C for 60s</td>
<td>DW</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>Photo 6 - Frontside Well Contact</td>
<td>Coat HMDS on CEE Hand Coater</td>
<td>DW</td>
<td></td>
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<td></td>
<td></td>
<td>Bake at 90C for 30s (Proximity Bake)</td>
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<td></td>
<td></td>
<td>Coat Resist on CEE Hand Coater</td>
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<td>Bake at 90C for 60s (Proximity Bake)</td>
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<td>Expose on KarlSuss MA56</td>
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<td>Bake at 140C for 90s (Proximity Bake)</td>
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<td>Develop on CEE Hand Developer</td>
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<tr>
<td>50</td>
<td>Etch Oxide - Frontside Contacts</td>
<td>10:1 BOE, 3.5 minutes (1600 A/min, 586 A/min)</td>
<td>DW + IMP</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>Strip Photoresist</td>
<td>PRS-2000 Bench</td>
<td>DW</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>Frontside Aluminum Deposition</td>
<td>CVC601 Sputter, 15sccm Argon, Power = 1500W, 5mT, 930s</td>
<td>DW + ET</td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>Photo 7 - Frontside Contact Etch</td>
<td>Coat HMDS on CEE Hand Coater</td>
<td>DW</td>
<td></td>
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<td></td>
<td>Bake at 90C for 30s (Proximity Bake)</td>
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<td>Coat Resist on CEE Hand Coater</td>
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<td></td>
<td>Bake at 90C for 60s (Proximity Bake)</td>
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<td></td>
<td>Expose on KarlSuss MA56</td>
<td></td>
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<tr>
<td>Step</td>
<td>Process Description</td>
<td>Equipment</td>
<td>Conditions</td>
<td>Notes</td>
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<td>------</td>
<td>---------------------------------------------------------</td>
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</tr>
<tr>
<td>54</td>
<td>Wet Etch of Frontside Aluminum</td>
<td>Aluminum Etch Bench</td>
<td>1 minute 20 seconds</td>
<td>DW + ET</td>
</tr>
<tr>
<td>55</td>
<td>Strip Photoresist, PRS 2000</td>
<td>PRS-2000 Bench</td>
<td></td>
<td>DW</td>
</tr>
<tr>
<td>56</td>
<td>Frontside Passivation Layer Deposition of LTO</td>
<td>LPCVD Upper Tube</td>
<td>425C LTO recipe, 4 min.</td>
<td>DW + ET</td>
</tr>
<tr>
<td>57</td>
<td>Photo 8 - Passivation Layer Trim</td>
<td>Coat HMDS on CEE Hand Coater</td>
<td></td>
<td>DW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Coat Resist on CEE Hand Coater</td>
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<td></td>
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<td>Bake at 90C for 60s</td>
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<td>Expose on KarlSuss MA56</td>
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<td></td>
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<td>Bake at 120C for 60s</td>
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<td></td>
<td></td>
<td>Develop on CEE Hand Developer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Etch Passivation Layer, BOE Chemical Bench</td>
<td>&quot;Pad Etch&quot;, 15 minutes (38 A/min)</td>
<td></td>
<td>DW + ET</td>
</tr>
<tr>
<td>59</td>
<td>Strip Photoresist, PRS 2000</td>
<td>PRS-2000 Bench</td>
<td></td>
<td>DW</td>
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</tbody>
</table>

**ACKNOWLEDGMENT**

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**REFERENCES**

Three Dimensional Nanochannel Formation by Reflective Interference Lithography

Michael Many

Abstract—An imaging technique using TM polarized illumination at 45 degree incidence to a highly reflective surface has been demonstrated possible. The imaging technique was able to produce a single row of over exposed nanochannels. Further experimentation will be required to develop a stable process where multiple rows of channels can be formed. Once the optimal process is determined, experimentation can be designed to create either or both photonic crystal structures and a pitch doubling technique.

Index Terms— lithography, immersion, interferometry, transverse-electric, transverse-magnetic

I. INTRODUCTION

In an effort to enhance lithography as hyper-NA with oblique angle imaging is approached, a novel method of imaging is investigated and tested. The imaging technique employs two-beam interferometry immersion lithography. The imaging makes use of a frequency doubling phenomena when transverse-magnetic (TM) polarized 193nm wavelength irradiation illuminates a photo-sensitive polymer (photoresist) over a highly reflective substrate at a specific interference angle. As the two beams of the interferometry system interfere at 45 degree incidence or 90 degrees to each other the intensity of the interference drops to zero. Although no intensity remains from the interference, the beams are able to reflect off the substrate. The reflected beam leaves the surface on a parallel trajectory to the other incoming beam. This causes an interference pattern with the reflected beam along the 45 degree trajectory. The resulting reflected interference creates a standing wave pattern along the 45 degree diagonal, where the node and anti-nodes are both intensity maximums, resulting in a frequency doubled pattern of channels transverse to the substrates surface.

II. THEORY

Highly temporal coherent illumination source, as used in 193nm lithography, create a standing wave effect from interference between incoming and reflected beams. Most lithography applications require the suppression of reflected beams to reduce this standing wave effect. As will be seen in later sections, imaging conditions will be chosen such that the standing wave pattern created will be along a 45 degree diagonal, which will result in a frequency doubling of intensity maximums.

Lithography use interference from a diffracted pattern of irradiation to create an image in photoresist. As incident angles of interference increases the intensity of the interfering beams begins to decrease. This decrease of intensity is a result of the interference of the magnetic field component of irradiation. The intensity of illumination for polarized illumination is defined as;

\[ I_{TE} \propto 2|E|^2 [1 + \cos(2kx\sin \theta)] \] \hspace{1cm} (1)

For transverse electric (TE) polarization

\[ I_{TM} \propto 2|E|^2 [1 + \cos(2kx\sin \theta)\cos(2\theta)] \] \hspace{1cm} (2)

For transverse magnetic (TM) polarization

The contrast of the formed image is defined as;

\[ C = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \] \hspace{1cm} (3)

For TE polarization the image contrast is always 1, which is why it is often used to enhance contrast in hyper-NA lithography.

\[ C_{TE} = 1 \] \hspace{1cm} (4)

While for TM polarization the contrast has an incident angle dependence define as

\[ C_{TM} = \cos(2\theta) \] \hspace{1cm} (5)

As the angle of incident light approaches 45 degrees, the contrast is decreasing until it falls to zero at 45 degrees and then becomes negative at angles above 45 degrees. At 45 degrees there can be no interference of TM polarized...
illumination.

Using TM polarized illumination at 45 degree incident angles should result in no imaging. If this illumination is combined with a highly reflective substrate, the reflected illumination leaves the surface parallel to the incoming illumination as seen in Figure 1. This creates a standing wave pattern. Since the incoming and outgoing waves are at 45 degree incident angles, the standing wave pattern created is on the 45 degree diagonal. Combined with the two beam fringe effect across the substrate's surface, the resulting intensity pattern in the vertical direction is an alternating stack of intensity maximums and minimums. The simulation tool ILSim[4] was employed to create this intensity simulation in Figure 2. The simulation uses 193nm illumination, water immersion lithography at 1.2NA, JSR ARX2829 JN-09 photoresist on a silicon substrate.

Figure 1. An illustration of the required illumination. The incoming beams are TM polarized

Figure 2. An exposure intensity simulation using ILSim.

Figure 3 is the intensity simulation of figure 2 with a threshold filter applied. The threshold filter would be equitant to the photoresist detector. This is the ideal illustration of the resulting nanochannels that should be created. In order to produce a frequency doubling, 20nm channels need to be created in the resist.

III. PROCEDURE

To create the nanochannels, a 193nm immersion lithography microstepper research tool by Amphibian Technologies[3] is used. The tool employs a 193nm coherent ArF eximer laser, chromeless phase-shift mask and a Smith Talbot prism setup to allow for NA up to 1.65 with advanced immersion fluids. For this experiment the incident angle of the beams must be at 45 degrees in the resist. The NA is defined as;

\[ NA = n \sin(\theta) \]  

(6)

Where \( n \) is the index of refraction of the media. In this case there need to be a 45 degree angle of incidence in the photoresist. The JSR ARX2928 JN-09 has a complex index of refraction of 1.6895-0.041i. The required NA for this experiment can be calculated as

\[ NA = 1.6895 \sin(45^\circ) \]

(7)

With the prisms available a 1.2NA prism was chosen to carry out the experiments.

The Amphibian XIS uses a chromeless phase-shift mask to act as a beam splitter, creating ideal only a +1 and -1
diffraction orders. These orders are then sent through the Smith Talbot prism. The Smith Talbot prism's design uses total internal reflection (TIR) off angled faces to recombine the diffraction orders. The unique design of the prism is such that translation alignment need not be perfect, as the diffraction order always travel the same distance before recombining.

![Diagram of Smith Talbot prism]

From the simulations, it was desired to create two layers of channel in the photoresist. The photoresist needed to be 80nm to accomplish this. At 193nm the silicon substrate had sufficiently large reflectivity to use it as the reflective surface beneath the photoresist, eliminating the need for additional processing.

Most immersion systems also employ a topcoat for protecting the lens from contamination caused by resist leaching. This experiment would also use a topcoat for protecting the prism. The topcoat should also be able to provide additional advantages. Photoresist is easily contaminated by amines and bases in the air. This neutralizes the top of the exposed regions and creates a condition called t-topping. A topcoat will eliminate the possibility of t-topping. Topcoats come in a multitude of varieties. For this experiment a developer insoluble topcoat was chosen to help maintain the top surface from collapsing. TOK TSP-3A was selected for the topcoat.

The substrate with photoresist and topcoat are then exposed on the Amphibian system. A post exposure bake is required to chemically amplify the photoresist. Since the channels in the photoresist are completely contained, the substrates need to be cleaved prior to development to expose the channels from the side. A standard Tetramethylammonium Hydroxide (TMAH) developer is used. Rohm and Haas CD-26 developer was selected.

After development the substrates can be baked if desired to harden the photoresist by causing cross-linking of the polymer chains. Hardbakes are often desirable in preventing samples from charging in scanning electron microscopes (SEM).

The samples are then prepared for mounting and SEM imaging. Cross-sections which have been coated with gold are investigated to see the formation of the channels.

IV. RESULTS AND DISCUSSION

Prior to beginning any experimentation on the proposed imaging technique, the Amphibian XIS had just been upgraded to provide better vibration isolation. Baseline wafers were run to prove the tool could operate at 1.2NA in a TE polarized state, with substrates prepared to suppress all standing waves. The upgrade to the tool performed exceptionally well.

Initial experiments were performed to create a reliable process for uniformly coating the photoresist. Using spin-speed curves from previous experiments on this photoresist, 2000RPM spin speeds were used as the starting point. 5 wafers were coated from 1900-2100RPM in steps of 50RPM to determine a process window for coating. The substrates were measured on a variable angle spectroscopic ellipsometer (VASE, by J. A. Woollam Co., Inc. U.S.A). The VASE revealed previous experiments were still accurate and 2000RPM was the optimal spin-speed. To measure across-wafer uniformity, the Cauchy coefficients of the photoresist were determined to be used in the Tencor SpectraMap. Two SpectraMap tools were available, so both were used with identical recipes to determine which was best calibrated to the VASE. After many attempts to tweak the recipes on the SpectraMap, the tool was not able to accurately measure the thin layer of photoresist. The VASE measurements were used for the remainder of the experiment.

The first run of experiments consisted of two wafers with 80nm of ARX2928 photoresist and 40nm of TSP-3A topcoat. The photoresist was coated at 2000RPM and baked at 110C for 90 seconds according to the manufacturer’s instructions. The topcoat was coated at 4000RPM to provide 40nm thickness. The topcoat was baked for 60 seconds at 90C according to the manufacturer’s instructions. They were both exposed using a dose meander recipe to provide multiple doses on a single exposure pass. The wafers were cleaved and developed in CD-26 which had been mixed with equal parts developer and DI water to reduce the normality to 0.13N. The pieces were further cleaved where needed to fit onto the SEM mounts, and then coated for 6 seconds in a gold desktop sputter system.

The samples were loaded into the ARAY 1830 SEM. The SEM images for all the samples (6 fields) all showed signs of edge cleave problems. The samples clearly showed what appeared to be a tearing of the topcoat, rather than a clean break. This tearing left the entire edge of the photoresist with defects many microns in size. This completely covered and/or destroyed any channels that would have formed.

A second set of experiment were design to eliminate the topcoat problem. It was decided to run the experiment without the topcoat. The problems with running without a topcoat is the possibility of the developer creating pattern collapse if any of the top most portion of the resist is
developed away. To prevent pattern collapse it was necessary to take advantage of the t-topping phenomena of the resist to neutralize some of the top of the resist creating a capping layer on the top of the photoresist. The other concern was the possibility of photoresist leaching contaminating the lens. The risk was acceptable, and the prism would be monitored after every exposure. All other parameters were held constant as the first experiment. There was a fluctuation in the gold sputter tool, it was left at a high current setting, which may have caused an over deposition of gold.

Upon inspection in the AMRAY SEM there was no longer a significant amount of debris and damage to the edge of the samples. A bigger issue however unfolded. THE AMRAY 1830 was not designed to image 20nm features and was at the time using a tungsten filament. The University of Rochester Optics and Biomedical program was kind enough to donate some time on their field emission Carl Zeiss. There SEM was able to produce great high resolution images of the samples. With the Zeiss SEM it quickly became apparent that the samples had too much gold deposited on them. One good sample was discovered. Figure 6 is the first and only image that showed signs of nano channels. The image shows channels which are approximately 30nm in width, which is overexposed for the intended dimension. Only one layer of channels is seen. The photoresist may have been left to t-top too long.

In order to reproduce these result, a third set of identically processed wafers were run to attempt to get better images with a properly applied gold coating. In order to get a finer gain size, the samples were coated with a gold alloy at the University of Rochester. None of the samples for the third experiment showed any signs of channels forming. All the samples appeared unexposed. Due to time constraints another set of samples could not be processed.

V. FUTURE WORK

There are two potential applications for this imaging technique. The first application is in the production of interference bandgap photonic crystals. Photonic crystals are used to alter the path of light. They contain repetitive patterns of two different dielectrics with high and low dielectric constants, where certain wavelengths are able to pass through the dielectrics. The application of this imaging technique would require a photosensitive dielectric capable of changing dielectric constant upon exposure. This method of photonic crystal creation is much simpler than the method of beam splitting and recombining currently practiced.

The second application of this imaging technique is as a single lithography method for pitch doubling. A novel method of pattern transfer has already been theorized. The process adapted from Dr. Bruce Smith of Rochester Institute of Technology is shown below. Two photoresist layers are alternately layered with a dielectric that has a matched complex index of refraction with the photoresist to minimize reflection between the layers. The process results in a single pass lithography pitched doubled image. At the parameters used in modern lithography and this experiment, 193nm water immersion lithography with 1.2 NA can produce 20nm half-pitch features.

VI. CONCLUSIONS

An imaging technique using TM polarized illumination at 45 degree incidence to a highly reflective surface has been demonstrated possible at the Rochester Institute of Technology. The imaging technique was able to produce a single row of nano channels. Further experimentation will require the development of a stable process where multiple rows of channels can be formed. Once the optimal process is determined, experimentation can be designed to create either or both photonic crystal structure and a pitch doubling technique as described.
Experimentation into developing a process for creating a pitch doubling technique would have major benefits to the semiconductor industry. The current generation of immersion lithography systems can be extended down to 20nm half-pitch.

ACKNOWLEDGMENT

The author would like to thank his advisor Dr. Bruce Smith for his guidance and inspiration. Neal Lafferty and Peng Xie of the Rochester Institute of Technology’s Nanolithography Research Center offered a great deal of support and assistance. He would like to give a special thanks to Brian McIntyre of the University of Rochester’s Optics and Biomedical Department for donating the use of their SEM and donating a large portion of his own time to SEM imaging. Jianming Zhou a PhD graduate of the Rochester Institute of Technology for his assistance with the project. The author would also like to thank all of the SMFL staff for their continued efforts to keep the FAB operating smoothly.

REFERENCES

Germanium Esaki Diodes by N-type In-Situ Doping

Amy Miller

Abstract—A rapid melt growth process is performed in the formation of Esaki tunnel junctions on in-situ n-doped germanium on silicon substrates. An aluminum-silicon alloy is used as the p-dopant for the junctions as well as an ohmic contact for testing. The rapid thermal anneal (RTA), used for the incorporation of the aluminum-silicon, is characterized by varying ramp rate and peak anneal temperatures. It is found that peak anneal temperature is the dominant factor affecting the current density through the devices. The maximum current density recorded is 2098 mA/cm² at a peak anneal temperature of 620°C.

Index Terms—alloy, in-situ doping, rapid thermal anneal (RTA), tunnel junction

I. INTRODUCTION

Recent interest has been taken in the area of germanium technologies specifically for its high current density tunneling capabilities. These properties are essential for the fabrication of low-power dissipation field-effect tunneling transistors as well as combining tunnel diodes with transistors in low-power circuits. The ITRS currently lists the tunnel transistor as an emerging research device to be used as an alternative to MOSFETs.

To create the Esaki tunneling effect, degenerately doped abrupt p and n junctions must be formed to maximize direct interband tunneling. A rapid melt growth process has recently been demonstrated by Zhao et al. at the University of Notre Dame for the realization germanium tunnel junctions. This process uses an RTA step to heat the devices above the eutectic temperature of Al-Ge. During the ramp up the aluminum and germanium react allowing aluminum donor atoms to incorporate into the germanium substrate. Upon cooling the germanium re-crystallizes forming the degenerately doped p-junction.

Aluminum has the highest solid solubility as a p-type dopant in germanium with concentrations possible to about 2x10²⁰ cm⁻³. Figure 1 shows the phase diagram for Al-Ge. The eutectic temperature of Al-Ge is Tₑ=420°C. Peak anneal temperatures above this value should theoretically result in 51.6% weight percent germanium or greater.

II. APPROACH

A. Simulations

To build the devices an n-type in-situ doped germanium on silicon substrate was used. The substrate had a known doping of 1x10¹⁹ cm⁻³. Using a rapid melt growth process the maximum doping concentration theoretically should be around 1x10²⁰ cm⁻³. Band gap simulations using Silvaco Atlas show the Fermi Level on the n-side at or slightly below the conduction band edge. Based on this information it was expected that the devices would have large depletion regions and act similar to a backwards diode. Negative differential resistance (NDR) is not likely since the n-type doping concentration is not high enough.

B. Process

This process was adapted from an existing process at Rochester Institute of Technology to create tunnel junctions. Fig. 3 outlines the steps in the original process and the new
process used in this study. The original process used a spin-on-glass (SOG) dopant source to dope the substrate. Since the substrates were already uniformly highly doped, this step was omitted. The substrates were patterned using contact photolithography with a LOR layer for use in a later lift-off process. The aluminum was DC sputter deposited on the patterned substrate. Substrates were then placed in a heated bath of Nanoremove PG to complete the lift-off process. The lift-off process was also a modification to the original process. The original process used a wet aluminum etch bath to pattern the aluminum, but it was found that the aluminum etch bath was attacking the germanium and an alternate method to pattern the aluminum was preferred.

<table>
<thead>
<tr>
<th>Step</th>
<th>Old Process</th>
<th>New Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SOG</td>
<td>Lithography using LOR and Resist</td>
</tr>
<tr>
<td>2</td>
<td>DC Sputter Aluminum Deposition</td>
<td>DC Sputter Aluminum Deposition</td>
</tr>
<tr>
<td>3</td>
<td>Lithography</td>
<td>Lift-off in Nanoremove PG</td>
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<tr>
<td>4</td>
<td>Wet aluminum etch</td>
<td>Alloy</td>
</tr>
<tr>
<td>5</td>
<td>Resist strip</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Alloy</td>
<td></td>
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</tbody>
</table>

Fig. 3. Old Process vs. New Process. This table outlines the changes made to the existing process at the Rochester Institute of Technology to form tunnel junctions in germanium.

III. P-DOPING EXPERIMENT

Although the substrates were not doped sufficiently to cause NDR, the factors of the RTA process to form the p-junction could be isolated because of the uniform substrate doping. Both ramp rate and peak anneal temperature were varied to characterize the anneal process. Ramp rates varied from 50°C/s to 150°C/s and peak anneal temperatures ranged from 550°C to 820°C. Fig. 5 shows the current voltage characteristics from this experiment. All data shown has a ramp rate of 100°C/s since this value showed the most consistent results and showed the most prominent inflection points. The current density had an obvious response to the peak anneal temperature.

Fig. 4 shows a representative cross section of the finished device. After the RTA process a p-type doped region is formed just below the patterned aluminum.

Fig. 6 shows how the current density of the devices responded to the peak anneal temperatures. There is an obvious decreasing exponential trend as the temperature increases. The hotter temperatures of the anneal process allowed the reaction between the aluminum and the germanium to take place for a longer period of time. Since the reaction takes place horizontally as well as vertically, the resulting junction had a less abrupt doping profile. This inhibited the tunneling current through the devices greatly limiting the current density at higher temperatures.

Fig. 7 shows the surface morphology of two separate samples after the anneal process. The image on the left shows a sample with a peak anneal temperature of 620°C. The reaction between the aluminum and the germanium was mostly confined to the areas right below the metal lines. The image on the right is a sample with a peak anneal temperature of 720°C. The reaction in this case has spread well beyond the metal lines and could actually be shorting out adjacent devices.

Ideality factor also showed a strong response to peak anneal temperature. Ideality factor vs. peak anneal temperature is shown in Fig. 8. At temperatures above 720°C and below 650°C there is an obvious degradation in device performance. Devices with peak anneal temperatures between these temperatures showed similar results with the 700°C anneal
temperatures showing the best ideality factor at 1.39. Devices using lower peak anneal temperatures probably did not see enough of a reaction between the aluminum and germanium, while the hotter temperatures could not contain the reaction. Both of these factors could contribute to the degradation in performance.

Fig. 7. Surface morphology of a sample annealed at 620°C (left) and a sample annealed at 720°C. The hotter temperatures allowed for a longer time for the reaction to take place resulting in the junction spreading well beyond the aluminum lines.

CONCLUSIONS

This study has shown that peak anneal temperature is the dominant factor affecting device performance of germanium Esaki diodes. Although dopant concentrations in the substrate were not high enough to promote enough direct tunneling to cause negative differential resistance, these same findings can be applied to other substrates to optimize tunnel junction devices. Lower peak anneal temperatures showed the highest current densities, but the ideality factor was degraded. Best device performance was seen using a peak anneal temperature between 650°C and 700°C.

ACKNOWLEDGMENT

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REFERENCES

Abstract—Polymer cholesteric liquid crystal display technology has been demonstrated previously on single pixel monolithic displays at the University of Rochester's Lab for Laser Energetics. Mass reorientation of PCLC flakes in a variety of host fluids has been modeled and observed. However, a pixilated PCLC display has never been demonstrated. The motive of the project was to create a prototype pixilated PCLC display in order to demonstrate the commercial viability of the technology. An active matrix back plane was designed, fabricated, tested, and incorporated with the existing PCLC display technology. The resulting display showed strong isolation between pixels with negligible cross talk.

Index Terms—Polymer Cholesteric Liquid Crystals, Active Matrix Displays

I. INTRODUCTION

Research and investment in particle based displays has expanded recently as flexible substrate technology has become more appealing and manufacturable. Using an electric field to control the motion of particles has been explored since the early 1970s. Electrophoretic displays were one of the primary contenders to replace cathode-ray tube displays until liquid-crystal technology became dominant in the 1980s. Particle displays are now regaining attention as flexible low power display development gains momentum.

The University of Rochester's Lab for Laser Energetics (LLE) has developed a unique display technology based on polymer cholesteric liquid crystals (PCLCs) flakes. [1] PCLCs have been traditionally used in passive applications for their reflection of specific wavelengths and polarization characteristics. At LLE the rotation of PCLCs suspended in a host fluid has been explored. A vertical electric field induces a dipole moment on the flake due to Maxwell-Wagner polarization, which causes the flakes to reorient its longest axis parallel to the electric field.[2] It has been shown that flakes suspended in a host fluid will reorient in as short as hundreds of milliseconds under an applied bias as small as 5 mV/μm.

All previous demonstrations of PCLC display technology have been on monolithic 'single pixel' devices. The motive of the project is to pair a custom active matrix backplane and the current PCLC technology to create a functional prototype PCLC display that has an array of pixel units that can be individually addressed. The first generation devices have been processed on silicon with the intention of moving the technology to a glass or flexible substrate platform for future iterations.

II. POLYMER CHOLESTERIC LIQUID CRYSTAL FUNDAMENTALS

A. Cholesteric Liquid Crystals

Cholesteric liquid crystals (CLCs) are a unique type of liquid crystal that can selectively reflect a specific bandwidth of light. The long range order of the molecules is defined by the director. The director lies in the plane of the LCs and twists in a helical fashion around the vector normal to the plane of the LCs. The distance it takes for the director to rotate 360° is defined as the pitch length (p) of the material and determines what wavelengths the CLC reflects. The direction of rotation of the director determines the handedness of the material. Fig 1.1 shows a diagram of a Cholesteric LC. PCLC flakes are made by heating the polymer CLC to its cholesteric state and then cooling it below its glass transition temperature, (T_g) fixing the internal orientation of the molecules.

Fig 2.1 A diagram of a left-handed cholesteric LC of pitch p. The director, n, is illustrated by the red arrows.

B. PCLC Flake Reorientation

PCLC flakes can be suspended in a moderately conductive host fluid such as propylene carbonate. A vertical field is applied to the suspended flakes causing them to reorient to the plane of the electric field. Fig 1.3 shows the change in orientation. Rotation is due to the vertical field, which induces a dipole moment on the flake. The dipole is
brought about by the difference in the conductivity and
dielectric constant of the flakes and host fluid. [3]

The rotation of the PCLC flakes cause dramatic drop in
reflectivity. Fig 1.4 shows a patterned ITO substrate before
and after the rotation of the flakes.

![Figure 1.4 Example of the rotation of PCLC flakes suspended in a host
fluid when a vertical field in applied. The vertical field is created by applying
a bias to one plate of the indium tin oxide (ITO) substrate and grounding the
second.](image)

III. DISPLAY ADDRESSING SCHEMES

In a pixilated display there are 3 main ways of
addressing individual pixels: direct, passive matrix, and active
matrix addressing.

A. Direct Addressing

In a direct addressing scheme each pixel is controlled by
its own individual control signal. In a display with \( m \times n \)
pixels, the display would require \( m \times n \) control signals. For
anything but the smallest displays this scheme is considered to
be inefficient use of I/O and physical space.

B. Passive Matrix Addressing

Passive matrix addressing can address \( m \times n \) pixels with
only \( m + n \) control signals. The scheme divides the incoming
signal into a select (row) signal and a video (column) signal.
Each row is addressed one at a time by raising the select signal
voltage. Each pixel in that row is then individually addressed
with a video signal. Passive matrices have no active elements and
therefore each pixel element needs bi-stability in order for it to maintain its image.

C. Active Matrix Addressing

Active matrix addressing uses the same number of
control signals as a passive matrix display. The main
difference is that each pixel is isolated individually through an
active component. The active component is usually a thin film
transistor in display devices. The addressing is done one row
at a time and starts by raising the signal voltage on the
address. The signal voltage is connected to the gate of each
transistor and turns the device on. Each pixel in the row is
then addressed by its individual video signal. The signal
voltage is then dropped low again isolating each pixel. Each
element has a built in capacitance that can maintain the
voltage applied by the video signal until it is addressed again.
The speed at which each row can be addressed and the number
of rows determines the total scanning period of the display.
The inverse of the scanning period is the maximum refresh
rate of the display. The scanning period must be less than the
time it takes for the capacitance on each device to decay in
traditional LC Displays. The quasi-bistability of PCLC
displays allows for moderately long delay (<1 min) between
addressing.

IV. NMOS ACTIVE MATRIX BACKPLANE

A. Active Matrix Design

The active matrix back plane design is based off of a
donut gate DRAM cell. Similar to DRAM, the basic cell is a
parallel plate capacitor with one plate being an aluminum pad
that is addressable through an active device and the second
plate is common ground to all of the pixels. The donut gate
transistor maximizes the effective device width and also
allows for square or rectangular pixels that can easily be tiled
to create displays of various sizes. The technology and
process flow for the devices is loosely based on the NMOS
portion of the SMFL CMOS technology, which uses lambda
of 5 μm. Fig 4.1 shows both an aerial and cross-sectional
diagram of a single pixel. The dimensions drawn are for a 635
μm square pixel. A variety of other pixel sizes where also
included in the design ranging from 250 μm to 5 mm. Fig 4.2
shows an array of 250 μm pixels prior to aluminum
deposition.

A unique feature of the device is the SU-8 3050 well
layer. It is designed to be 100 μm thick and have a minimum
dimension width of 20 μm. It is the last processing step before
dicing the wafer and is critical because the high aspect ratio
4.5:1 "wells" are difficult to resolve and the epoxy based SU8
resist cannot be reworked. The SU-8 wells serve a dual
purpose in the device. First, it determines the gap height
between the aluminum and the ITO glass which must be thick
enough to allow the flakes to rotate, but thin enough to allow
for minimum field strength of 50 mV/μm. Secondly, the wells
physically isolate the fluid and flakes in each pixel. This is
crucial because both the fluidic motion of the pixels during
rotation and the fringing electric fields during addressing can
cause the flakes to laterally migrate out of "on" regions, which
effectively destroys the device. Metrology of the SU-8 layer
was done using a Zygo white light interferometer and
measured the SU-8 well to be 89.6 μm thick.
B. Active Matrix Electrical Testing

The devices were electrically tested prior to the SU-8 well layer being patterned. Fig 4.3 shows a threshold voltage of 0.6 V. An $I_{DS}$ versus $V_{DS}$ plot with 0.5 V increments of $V_{GS}$ is shown in Fig 5.4. The $I_{on} / I_{off}$ of the device is greater than 5 decades, with a peak drive current of about 25 mA. The donut gate device has a gate length of 20 μm and an effective width of 2300 μm, which gives roughly 10.9 μA per micron of device width.

V. DISPLAY ASSEMBLY AND RESULTS

A. Display Assembly and Packaging

Final devices were assembled by dicing the wafers into their individual display components. The display itself is assembled by filling the SU8 wells with propylene carbonate and a 1-5% concentration by weight of commercial freeze fractured flakes. The display is then sealed by bonding glass with an ITO film onto the top of the display using a UV curing epoxy. The device is sealed with epoxy along the edge to prevent contamination and leaking of the fluid. A 64 x 64 array of 635 μm pixels at this point is shown in Fig 6.1. The voids in the display are caused by air bubbles being trapped in the SU-8 wells when the display is sealed.

The bottom image in Fig. 6.1 shows the same display without a circular polarizer. PCLC technology is designed not to need a polarizer however limitation of the active matrix technology requires one as discussed in Section 7.

Final devices were mounted to custom PCBs that include simple drive circuitry capable of addressing sections of the display. They are attached to the board using two-part epoxy and then electrically connected using colloidal silver paint. The driver boards are not capable of addressing individual pixels, however sections of the display can be addressed and
checkerboard patterns can be displayed. Fig 6.2 shows the same display mounted on a custom PCB board.

B. Display Results

Using weak biasing signals of $2.5 - 4$ $V_{pp}$ 100Hz AC, videos of flake rotation were recorded under different magnifications. Fig 6.3 shows the center 635 µm pixel being biased with a $2.5 V_{pp}$ 100 Hz signal under 30x magnification. The flakes rotated in approximately 6 seconds. Much faster response times can be obtained by using larger drive voltages (<1 second). The 3.5% PCLC flake density by weight produces an image with strong contrast.

Fig 6.4 shows the border of two 635 µm pixels under 100x magnification. The flake density is very low in this display and allows for each flake to be seen rotating individually. The right side of the image shows the majority of the flakes rotating while the left side remains unchanged. This demonstrates very strong isolation between pixels. Meaning that cross talk between adjacent pixels is not a problem in the display. The unrotated pixels on the right side are due to flakes sticking to the ITO surface.

Fig 6.5 demonstrates the change in reflectivity that can easily be seen with the naked eye. The entire array 8 x 32 array of 1270 x 423 µm pixels is addressed with a $2.5 V_{pp}$ 100 Hz AC signal in order to turn ‘off’ all of the pixels. The before and after pictures demonstrate an easily visibly change in brightness between the on and off states. The remaining unrotated pixels shown in the bottom picture can be attributed to either poor contact to the aluminum pads or defective pixels.

VI. CURRENT PROBLEMS AND FUTURE WORK

A. Active Matrix Issues

One of the attractions to PCLC technology is its ability to produce high contrast images of any color without polarizers or color filters. Unfortunately when the flakes are above a reflective substrate, like aluminum, it is difficult to differentiate between the reflectance of the PCLC flakes versus the light reflected by the substrate. This problem is clearly illustrated in the difference in color and brightness between the top and bottom images in Fig 6.1, which shows a 64 x 64 device both with and without the polarizer. Some grain can be seen without the polarizer, however the contrast is so low that it is practically negligible. The aluminum reflects nearly the entire spectrum of incident light, defeating the purpose of having a selectively reflective material above it. This known fault of the first generation technology is remedied by adding a circular polarizer to the display, which significantly increases the display contrast.

Future iterations of the active matrix need to substitute the aluminum for an alternate non-reflective conductive material. This would allow the device to operate without a polarizer and significantly reduce the price and complexity of any commercial application. Possible materials include moving to a completely transparent device and using ITO to substitute for the aluminum. Alternatively, a dark or black metal such as Titanium Nitride could be used. Other materials should be investigated with the primary qualifications being low resistance, low reflectance, and patternability.
Other problems with active matrix display to address include: routing, isolation, scalability and both response and relaxation times. Routing and isolation of signals is the next most significant problem in the displays. Routing in diffused silicon should be avoided and a multi-level metal system needs to be incorporate into future iterations.

B. PCLC Issues

A combination of PCLC specific issues need to be addressed. The most important problem is the inability of the display to reorient themselves back to their reflecting state without waiting for gravity to naturally relax them. This is most limiting aspect of the technology and is of primary concern. Several solutions are being researched including the development of a unique waveform to ‘shock’ the flakes back into their horizontal position. Secondly, a novel device structure could be used to apply a horizontal field to a pixel.

Secondly, the response time and variation of the displays can also be significantly enhanced (<100 ms) using LLE’s unique shaped flake technology. This allows for uniform PCLC flakes to be used that have identical response and relaxation times. Also, using layered shaped flakes which are made of two materials that reflect left and right handed polarization states respectively will allow for displays with near 100% reflectance at the designed wavelength.

VII. Conclusion

A custom active matrix back pane was design, fabricated, and packaged for use with PCLC flake display
technology. The fabricated displays demonstrated the ability to individually address pixels inside of an array.

Future iterations of the technology need to incorporate non reflective materials and advanced PCLC technology such as shaped and layered flakes. With these changes PCLC flake displays represent a real and viable technology for low power and low cost display applications.

VIII. ACKNOWLEDGEMENTS

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LLE: Gerald Cox, Ken Marshall, Dr. Steven Jacobs, Dr. Tanya Kosc, Catherine Fromen

IX. REFERENCES


Abstract— Single crystal silicon photoactive devices using a low-temperature thin-film transistor (TFT) compatible process were designed and manufactured on bulk silicon and silicon-on-insulator (SOI) substrates at the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT. Photodiodes and phototransistors designed with transparent indium-tin oxide (ITO) gates, along with n-type and p-type ITO Schottky test devices were manufactured and investigated. Possible applications for devices investigated here include on-display photodetectors, on-display digital logic and possible integration into touchscreen or lightpen sensitive liquid crystal TFT displays.

The photoactive devices were integrated in active pixel sensor (APS) arrangements to determine feasibility of integration into large-field SOI or Silicon on Glass (SiOG) applications. Currently most APS sensors fabricated using standard bulk silicon processes are incompatible with TFT processing due to temperature constraints; standard TFT processing does not exceed ~660°C. Device sizes were varied in order to quantify sensitivity due to junction size. Elements of the APS circuit were scaled to enable the acquisition of a transient response.

Index Terms—Active pixel sensor, photodiode, silicon-on-insulator, silicon-on-Glass.

I. INTRODUCTION

CLASSICALLY, Thin-film transistors have been built using amorphous silicon on glass substrates. This has provided working devices with the lowest cost for the display industry. The performance of these TFT devices is inferior to crystalline silicon, in that carrier mobility in amorphous silicon is two orders of magnitude lower. This paper will attempt to demonstrate the advantages of crystalline silicon over amorphous silicon using TFTs, and will also provide an overview of a manufacturable process for TFTs on crystalline silicon using SOI or SiOG.

Recently, a step has been made by certain corporations (e.g. Corning, Inc.) to produce a new substrate which incorporates crystalline silicon with glass. This process, when it meets fruition may provide near-SOI quality semiconductor on a large glass substrate. This would facilitate the manufacture of not only higher quality flat panel displays, but also allow for integration of amplifiers and digital logic on the display itself, where currently these devices are integrated off-display, linked by wirebond. Using the process outlined in this paper it is possible to obtain working CMOS logic on glass, using a TFT compatible process.

Photoactive devices will be investigated, along with silicon photodiodes, in an APS arrangement. ITO gate transistors and photodiodes were integrated on the same design. Much like standard TFTs, photoactive devices benefit greatly from a move to crystalline silicon. Photoresponse should scale with the differences in carrier mobility, providing the ability to not only have a display, but also have a detector on the same piece of glass. However, there is an inherent tradeoff in junction area if the device region is confined within a thin-film crystalline silicon layer.

II. DEVICE DESIGN

Standard TFTs and photodiodes were constructed using a molybdenum gate, self-aligned process with aluminum as the metal on both SOI and bulk.

Fig. 1. Cross-sectional diagram of ITO gated phototransistor. ITO is contacted to a Mo bridge and Al is contacted to Mo. Done to prevent HF contact with ITO, the results of which are uncharacterized.

Fig. 1. shows a representative ITO gate phototransistor. The ITO gate phototransistors were constructed with a non-self-aligned process, and contacted to metal via a molybdenum bridge. This design alleviates the need for an HF contact cut through silicon dioxide down to ITO, and instead cuts down to molybdenum; the interaction between HF and Mo is better characterized than that of HF and ITO, and this was done to remove uncertainty from the process.

Other than acting as a transparent, conductive gate, the ITO layer was utilized to investigate phototransistor and possible Schottky effects due to workfunction difference when contacted directly to silicon.

Silicon photodiodes investigated were of the P-I-N variety,
with a 12-micron long junction length. Widths of the photodiodes were varied to examine photocurrent response to junction size. The lengths investigated were 116μm, 216μm, 280μm, 344μm and 408μm.

Fig. 2. Layouts of 5 photodiode sizes investigated in this paper, increasing in size from left to right, these devices have junction widths of 116, 216, 280, 344 and 408μm.

Fig. 3. Cross-sectional diagram of P-I-N photodiode. Photoactive area is centered around the intrinsic silicon (lightly doped p-body) between the two Al contacts.

Fig. 4. Schematic of active pixel sensor circuit. Photodiodes or phototransistors can take the place of the photodiode in the schematic.

Figure 4 shows the generic schematic of an active pixel sensor circuit. The photoactive components were integrated as part of an APS circuit[2]. The APS circuit is comprised of 4 or more transistors arranged to provide clocked output for digital imaging applications. These are most commonly utilized in modern digital cameras and some forms of medical diagnostic digital imaging.

In order to utilize an APS circuit[1], proper timing and clocking must be implemented. Before the photoactive device can be used, a voltage must be set, or more correctly, a charge accumulated on the gate of Msf; this is done by turning the RST signal high, causing Mrst to turn on. To read out, RST goes low, turning off Mrst, and the charge accumulated on Msf is dissipated by the photoactive component. The charge on the gate of Msf will determine the conductance of the transistor, and the amount of current passing through the readout rail, or the voltage drop over Msf and Msel is utilized by the readout circuit. The current or voltage is read off the COL, and the ROW signal going high will cause the pixel to be read.

Due to the importance of the capacitance of the integration node Msf, its sizes were varied as part of the design. In order to obtain a transient response as opposed to a high-speed clocked response from the APS, the integration node must be made very large. Msf sizes were designed as 12x4, 100x100 and 320x320 micron.

Lightblock was added to prevent stray light from affecting the performance of the non-photoactive transistors in the active pixel sensor array. It is a metal layer over a passivating ILD. It is not present over photoactive devices and testpads.

III. DEVICE FABRICATION

Processing was done on 100mm bulk p-type wafers and n-type SOI wafers. Only Bulk NMOS will function without VT adjust implant. NMOS and PMOS will function on SOI.

A ten level mask set was designed for use on quad reticles (4 layers per plate) with a 5x reduction stepper. Normal TFT processing only uses six lithography levels, however this process included two non-standard layers, ITO and Lightblock metal. All lithography was done using an SVG 100mm coat and develop track, and a GCA 6700 g-line 5x reduction stepper. Exposure was found to be optimal at 1.9 seconds with a focus setting of 100. HPR 504-10 resist was used with CD-26 as a developer.

Deposition of layers was done in a myriad of tools. Low pressure Chemical vapor deposition of oxide was done in an ASM 150mm LPCVD system, using a 425C LTO recipe. Molybdenum was deposited using a CVC 601 sputter tool. ITO was also sputtered using the same tool, using the following parameters: 180W pulsed DC, 1600ns pulse width at 250KHz, sputter at 5mT with a 10-20 minute pre-sputter. A 1-hour sputter yielded approximately 2400 angstroms of ITO, or approximately 40 angstroms per minute. The resulting film was translucent and conductive, measuring 180 ohms/square.

Ion implantation was done in a Varian 350D Implanter. Four implants were done, backside 2E15 boron at 35KeV,
4E15 phosphorus at 110KeV, 3E15 fluorine pre-amorphization at 60KeV, and 4E15 boron at 35KeV.

Etching processes were done using a LAM490 silicon plasma etcher, along with a Drytek Quad which dry-etched molybdenum. A specialized wet etchant, formulated 10:10:1, water : hydrochloric acid : nitric acid was used for ITO. This etchant was noted to be extremely sensitive to temperature and etch rate repeatability was only obtainable at 17-20°C.

IV. DISCUSSION

Fabrication of devices is still being investigated. The patterned ITO gates and other ITO devices suffered undercutting during etch and are non-working.

Fig.5. Optical micrograph of ITO gate device. ITO is present on the wafer, as can be seen in the ITO contact cut.

Fig.5. is an image of a representative device with ITO deposited before lithography. Directly after this step, a lithographic pattern was applied to form a gate. When that gate was wet etched, the ITO began to lift-off and undercut along major lines of topography.

Fig.6. shows the result of a wet etch on an ITO gate device. The speckling and rough appearance are indicative of lift-off and undercutting. Undercutting this severe will result in open-circuits and therefore lead to non-working transistors.

The silicon mesa etch done on the SOI wafers early in the process suffered a non-uniformity problem and this was not discovered until later processing. At that point it was impossible to correct the mesa etch problem, so the fabrication of devices was continued despite the non-uniformity which may short some mesas on the SOI device wafers.

V. CONTINUING INVESTIGATION

Work is being done to engineer solutions to the undercutting observed when wet-etching ITO over major topography. This work is being done in the design of a modification of the layout of the mesa/active area with respect to topography and specifically the positioning of ITO gates. By redesigning the gate topography to be mostly planar, it should alleviate the undercutting and lift-off problems observed.

Fig.7. Diagram of proposed layout design change to combat ITO undercutting along topography.

Fig.7. shows a proposed change in the layout of the active mesa which may solve the problem of undercutting. The device on the right is the current design which is in manufacturing. The ITO (the vertical part of "T") intersects with the edges of the active (the horizontal part of the "T"). In the device on the right is the changed layout, with the ITO completely surrounded by mesa on all sides with an overlap. While not an elegant solution it is a possibility.

Another possibility is the use of a dry-etch process incorporating methane or halogens. Both of these are, however, covered under intellectual property of several organizations and also pose very real risks of contamination of the chamber, along with hazardous byproducts.

Fabrication also continues on devices which suffered the ITO problems. The photodiodes and active pixel sensor devices remain unaffected and may prove functional.

VI. CONCLUSION

A process for manufacturing crystalline silicon TFTs on SOI and glass was investigated. Setbacks due to ITO wet etch problems were encountered. Solutions for correcting the problems are being engineered and fabrication continues with electrical results forthcoming.
ACKNOWLEDGMENT

I.J. Onigman would like to thank Dr. Karl Hirschman, Dr. Sean Rommel, Ms. Patricia Meller, Mr. Christopher Shea and the staff of the Semiconductor and Microsystems Fabrication Laboratory.

REFERENCES


Isaac J Onigman is a graduate of the Rochester Institute of Technology in Microelectronic Engineering with a minor in Criminal Justice. He was born in Manchester, New Hampshire, and has co-oped at the General Electric Global Research Center in Niskayuna, NY on the wet/dry etch group working in digital mammography production.
Abstract—Fully processed CMOS Si wafers were reclaimed to make solar cells, while ensuring an acceptable efficiency loss of 15%. This project successfully developed a wafer reclaim process coupled with a solar cell fabrication process. The optimum efficiency obtained was 12.4% using prime wafers and surface texturing, while comparably processed reclaimed wafers were able to achieve 10.5% efficiency.

I. INTRODUCTION

Demand for electricity is increasing at an exponential rate, our consumption of coal is harmful to the environment and solar cells seem to be a promising alternative. One key factor for future implementation of solar cells is cost per watt, reclaiming scrapped silicon wafers into solar cells may be a viable option. This project is aimed towards the use of reclaimed silicon wafers for reducing cost while ensuring acceptable efficiencies.

Fully processed CMOS Si wafers were reclaimed to make solar cells. The reclaim process removes 100μm of the top surface by grinding, this was done to ensure all deposited and diffused layers have been removed. After the front grind process, wafers were polished using chemical mechanical polishing (CMP), followed by a clean using wet processes.

II. THEORY

A. Wafer Reclaim

Wafers that have undergone CMOS processing may have many deposited layers as well as diffused layers that need to be removed before subsequent processing. 100μm of the top surface ensures the removal of all deposited and diffused layers. The wafers were then polished in order to be of the same surface roughness of prime wafers, this step may be skipped in future work. Once polished, a modified RCA clean was used to ensure the removal of contaminants.

A modified SC2 is used initially to remove metal contaminates. The higher concentration of hydrochloric acid etches off residual metals that may have adhered to the substrate during the wafer grind process. The SC1 bath is used to ensure the removal of organic contaminates, the wafers are then etched in HF to remove the native oxide. Once the native oxide is removed a subsequent metal contaminant clean is utilized to further ensure the removal of metals. Between cleans is an assumed 5min DI water rinse clean undergone at room temperature. Fig. 1 shows the entire clean process.

B. Solar Cell

Figure 2 shows a typical solar cell with an n-type emitter on a p-type wafer. An if the hv of the incoming light is greater than the bandgap of silicon, an electron hole pair is generated. A fraction of the generated electron hole pairs are collected by the depletion region and internal electric field. If the carriers are not recombined, they are collected by the metal fingers and grid.

![Figure 1 Wafer Cleaning Process](image.png)

![Figure 2 Typical Silicon Solar Cell](image.png)
Figure 3 shows a single diode with simulated parasitic series and shunt resistances. To obtain the maximum amount of power from the solar generated current \(I_R\) to the load, the series resistances should be minimized and the shunt resistance should be maximized. Two key parameters when considering solar cells are the short circuit current and the open circuit voltage, these parameters are highly dependant on series and shunt resistances as shown in equation 1 and equation 2.

\[
I_{sc} = I_R - I_0 \left[ \exp \left( \frac{q}{nkT} \left( I_{sc} R_s - 1 \right) \right) \right] - \frac{I_{sc} R_s}{R_{sh}}
\]

Equation 1 Solar cell short circuit current

\[
V_{oc} = \frac{n k T}{q} \ln \left( I_R + 1 - \frac{V_{oc}}{I_0 R_{sh}} \right)
\]

Equation 2 Solar cell open circuit voltage

III. EXPERIMENTS

A. Experiment I

The goal of the first experiment was to fabricate working solar cells using different simulated diffusion profiles as well as oxide thicknesses. Table 1 shows all the treatment combinations.

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>X_e (nm)</th>
<th>OXIDE (nm)</th>
<th>INTEGRATED DOSE</th>
<th>AVERAGE DOPING</th>
</tr>
</thead>
<tbody>
<tr>
<td>900°C FOR 20MIN</td>
<td>200</td>
<td>100</td>
<td>4.2E+012</td>
<td>2.1E+17</td>
</tr>
<tr>
<td>1000°C FOR 20MIN</td>
<td>421</td>
<td>400</td>
<td>4.13E+012</td>
<td>9.2E+16</td>
</tr>
<tr>
<td>1100°C FOR 20MIN</td>
<td>950</td>
<td>553</td>
<td>4.06E+012</td>
<td>4.3E+16</td>
</tr>
</tbody>
</table>

The top metal finger grid design was also varied for all experiments to determine what the optimum spacing between fingers and the optimum metal thickness is. Figure 5 shows this top level metal mask, which also includes TLM structures and test diodes to be able to extract contact resistance and diode idealities. The nomenclature for the mask is line width/spacing and all numbers are in microns.

B. Experiment II

Using the optimum diffusion profile found in experiment 1, fully processed CMOS wafers were reclaimed and were processed into solar cells. Using the tools and process parameters shown in figure 6 coupled with the wet processes shown in figure 1, reclaimed wafers had 100um of their top layer removed were chemical-mechanically polished and then wet cleaned.
Experiment III's goal was to increase efficiency by increasing the surface area of the solar cell and also attempting to reduce reflection loss. This was done by surface texturing as seen in figure 7.

Inverted pyramids by KOH etching in the configuration shown in figure 7 were achieved as well as top and back surface fields for enhanced carrier collection.

IV. RESULTS

A. Experiment I

Figure 6 Wafer reclaim process

Figure 7 Cross-section of modified PERL design[1]

Figure 8 100nm Oxide spectral response and simulated absorption

Figure 9 400nm Oxide spectral response and simulated absorption

Figure 10 500nm Oxide spectral response and simulated absorption

Figure 11 Experiment 1 Spectral Response
Figure 12: Solar cell IV characteristic

B. Experiment II

Figure 13: Reclalm wafer spectral response

Figure 14: Reclalm wafer IV characteristic

C. Experiment III

Figure 15A: SEM image of textured fabricated solar cell

Figure 15B: SEM image of textured fabricated solar cell

Figure 15C: SEM image of textured fabricated solar cell
V. DISCUSSION

Figures 8-10 show the spectral response plotted with the simulated absorption. Figure 8 shows the 100nm oxide device performance not being hindered by its reflection loss, whereas the other figures 9 and 10 show significant device performance decreases at the reflection peaks or the absorption valleys. These were proof of concept measurements to accurately indicate that reflection was truly hindering the performance of the device and using an optimum oxide thickness increases device performance. This conclusion is clearly shown in figure 11 where the spectral response of all three devices are plotted together. It shows that the 100nm oxide has the best device performance, which is also reflected in figure 12’s current-voltage characteristic. The 100nm device generates more current as expected from its spectral response.

Experiment II’s results are shown in figures 13 and 14, where it could be shown that the reclaim wafer has a shifted spectral response and does not perform as well as the prime wafer. At 600nm the reclaim wafer has a decrease in response as shown in figure 13, this may be attributed to gettering sites in the CMOS process the reclaim wafers had undergone previously. In future work, it is possible to cleave the reclaim wafer and wet etch the gettered sites preferentially and under a scanning electron microscope it will be easy to see where the gettered sites are located. As expected the generated current for the reclaim wafers is not as high as the current generated by the prime wafers. This is can be attributed to a lower carrier lifetime, the carriers are being recombined before they are collected by the metal finger scheme.

Figure 15A-C show the fabricated textured cell’s cross-section which is similar to the simulated desired cross-section shown in figure 7. The pyramid mask design was 30μmX30μm squares, but after undercutting they were fabricated at 37.5μmX37.5μm squares as shown in the scanning electron microscope pictures. This increased the surface area of the device by 50%, although the irradiance through the increased surface area is constant. Another advantage of the inverted pyramid design is its decrease in reflection as shown in figure 2. A measurement that can be taken as future work is scatterometry measurements, by shining light incident to the sample and collecting reflected light at various angles, an experimental reflection value can be obtained by adding all of the individual angle’s reflection measurement. Figure 16 shows the reclaim wafer performance as compared to a prime wafer’s performance, and as expected the reclaim wafer has a decrease in spectral response as shown in table 2 as well.

VI. CONCLUSION

The goal of developing a process to reclaim wafers into solar cells has successfully completed. An acceptable efficiency loss of 15% has been demonstrated comparing prime and reclaimed silicon as shown in table 2. This experiment has shown that using reclaimed silicon can be a viable option to meet the future electricity demands.

ACKNOWLEDGMENT

The author would like to acknowledge all of those who have helped along the way, including, but not limited to SMFL, NPRL and μE. If it weren’t for the people around us, we would be nothing.

REFERENCES

Surface Micro-Machined Capacitive Pressure Sensor

Scott Raguse

Abstract—This project entailed the design, fabrication, and testing of a surface micro-machined electret pressure sensor with the possible use as a microphone. The design is based on a capacitance electret microphone. This type of microphone uses a plate that has a built in charge to provide the bias of the system. This eliminates any external bias directly attached to the sensor. The surface micro-machining means that no backside etch is required to form the membrane. Without the backside etch the process can be integrated with a CMOS process much more easily. This electret pressure sensor uses a poly-silicon floating gate that has a fixed charge \( Q \) place on it to create an internal bias between the floating gate and the upper aluminum diaphragm. This means that the device can run without a sustained external bias, instead of the constant bias that a condenser pressure sensor/microphone requires. The device can run without a sustained external bias, instead of the constant bias that a condenser pressure sensor/microphone requires. The diaphragms were completely released from the sacrificial resist, and were shown to hold their shape.

Index Terms—CMOS compatible, electret, floating gate, surface micro-machined

I. INTRODUCTION

The MEMS industry is one of the fastest growing sectors of the semiconductor industry. To make the devices compatible with CMOS technology, the use of a backside etch to form a diaphragm needs to be discontinued. If a device can be created using only surface techniques, then the CMOS circuitry can be integrated on chip with the MEMS device. This saves cost and results in a smaller package. Small microphones are needed in many applications such as hearing aids, cell phones, and even in some car systems. MEMS microphones are ideal for these applications due to their low cost small package.

Electret microphones lend themselves for such MEMS manufacturing and small scale microphones. The microphone does not require an external bias. An amplification circuit does require power, but this would be required in a condenser microphone also.

II. THEORY

Capacitive Microphones

Capacitive microphones work on the concept of voltage changes from a variable capacitor. One of the plates of a capacitor is a diaphragm that is sensitive to sound pressure waves. The two plates are biased with a fixed charge \( Q \). Since the capacitance equation states \( C = \frac{Q}{V} \), and \( Q \) is held constant, that mean the voltage \( V \) must change when the capacitance \( C \) changes due to the diaphragm deflection [1]. This change in \( V \) is measured and the fluctuations are the electrical representation of the sound waves. In a condenser microphone \( Q \) is produced by a constant DC bias or from a RF voltage. An amplification circuit, which also has to be powered, is usually also required to produce a usable signal [2].

An electret microphone works on the same principle as a condenser microphone; however, in an electret microphone \( Q \) is built into the device. The term "electret" is used to describe a material that has been permanently electrically charged. Since the electret plate of capacitor already has a fixed charge \( Q \), there is no need for and external bias for the device. Power is still needed to run the amplification circuitry that produces a useable electrical signal from the small voltage changes from the diaphragm deflections [1].

Diaphragm Calculations

The diaphragm for a pressure sensor or a microphone needs to be ridged enough to easily support itself, but also flexible enough react to desired pressure changes. Aluminum is a easy material to work with when performing MEMS surface processing. The thickness of the material and the capable size of a circular diaphragm can be calculated by using Equation 1.

\[
y = \frac{3PR}{16E(\frac{1}{\nu})^2} - 1
\]

Equation 1: Maximum deflection of a circular diaphragm

Where \( P \) is pressure, \( R \) is the radius, \( \delta \) is the thickness, \( \nu \) is Poisson’s Ratio, and \( E \) is Young’s Modulus. This equation give the maximum deflection at the center of the diaphragm at a given pressure [3].

III. PROCEDURE

Design

To form the electret pressure sensor a chargeable electret material needed to be chosen. A charging mechanism also needed to be determined. Poly-silicon was chosen to be the electret material. The poly-silicon would be isolated by \( \text{SiO}_2 \) and become a floating gate. The floating gate would then be charged using Fowler Nordheim tunneling through a thin gate oxide separating the poly-silicon from the silicon substrate. This would then require a control gate. The Al diaphragm was first considered for this task, but an air gap of 1\( \mu m \), the desired separation, would be too great to produce tunneling. It was decided then to use a two metal process, in which metal 1 would be used as the control gate and metal 2 as the diaphragm.

The diaphragm was determined to require a 2\( \mu m \) thickness
in order to support itself. The ideal diameter of the device was then determined to be about 100μm. It was then determined to have diaphragms of 50, 100, 150, and 200μm in diameter. This would provide different sensitivities, and provide some data on the durability of the Al diaphragms. Fig. 1 shows design of the sensor. The dimensions were then just scaled for the other sizes.

Process
For these devices it was decided to use 6 inch wafer and the corresponding toolset. The starting substrates were 10Ω-cm P-type wafers. A 500Å pad oxide was then thermally grown on the substrate. Next 1500Å of nitride was deposited using LPCVD process. This would be used to for a LOCOS process in order to produce alignment marks on the wafer. Photo 1 was then performed on the Cannon i-line stepper to defined the N-well regions and the alignment marks. A dry etch was used next to remove the nitride from the exposed areas. The wafers were then ion implanted with P31 at a dose of 2x10¹⁵. The photo resist was then removed and an RCA clean was performed on the wafers. The wafers were then placed in the furnace to grow a 4000Å wet oxide. The nitride and oxide were then removed using wet chemistry. In order to provide a uniform gate oxide growth, a 1000Å Kooi oxide was grown next. This was stripped and a 150Å dry gate oxide was grown on the wafers. LPCVD poly-silicon was then deposited to a thickness of 5000Å. The poly was then doped using an ion implant of P31 at 60keV at 4x10¹⁵ to form an N⁺ poly floating gate. During the furnace activation, a 500Å oxide was grown on top of the poly to form the control gate oxide. To protect this oxide, a 1500Å LPCVD nitride was deposited.

Photo 2 was next defining the floating gates. Dry etch was then used to etch through the entire gate stack. Once the resist was removed and the wafers cleaned, a 3000Å SiO₂ was deposited using a PECVD TEOS process. Photo 3 then defined the contact cuts and the control gate opening. The oxide was etched in BOE. The exposed nitride layer protecting the control gate oxide was then etched away using a hot phosphoric etch. This provided a very good selectivity between the nitride and the SiO₂. A 5000Å Al layer was then deposited using the CVC 601 Sputter. Photo 4 then defined the metal 1, which was etch using the wet Al etch. Another 3000Å ILD was deposited and photo 5 was performed to define the via’s and also to open up the region that will be the air gap under the diaphragm. The oxide was etched away using a BOE bath. Photo 6 was then performed to apply a 1μm photo resist layer that would act as the sacrificial layer to form the air gap under the metal 2 diaphragm. The 2μm metal 2 was then deposited using the CVC 601. Photo 7 then defined metal 2 and the Al etch bath was used to remove the unprotected Al. An O₂ plasma ash was then used to remove both the metal 2 definition resist, and the underlying sacrificial resist. The plasma had access to this resist through opening in the metal 2 layer. Fig. 2 shows a cross-section of the completed process, and Fig. 3 shows a top down view of a fully processed device.

IV. RESULTS AND DISCUSSION
Testing
The devices were initially tested using a probe station to characterize the tunneling and view any changes in the voltage drop across the N-well and the diaphragm. It was determined at this point that the control gate was shorted to the N-well. This meant that the floating gate could not be charged. In order for the device to work the floating gate needs to have a fixed charge Q placed on it. Since the floating gate was designed to be isolated there was also no chance of testing the diaphragm as a condenser microphone. All three of the fully processed wafers were found to have this same short.

The cause of the short is believed to be a combination of factors. The floating gate dry etch etched to far and went into the substrate. This caused the exposed surface to become rough and pitted. This pitting was translated into the ILD layer. This could have cause some unexpected etching during the contact etch, thus opening a path for the control gate to short to the substrate or the floating gate.
**Diaphragm Integrity**

The diaphragms were found to hold up and keep their shape very well. There were some issues with the diaphragms lifting off. This most likely happened in the spin rinse dryer after the Al etch. The edge of the sacrificial resist provided a stress point for the metal to break off. Once the structure was weekend my etching away some of the metal, the stress of the water jets and spinning could have proved too much for some of the diaphragms to handle.

Fig. 4-6 show images of the finished devices taken using the Veeko Wyko profiler. This tool uses white light interferometry to map surface heights and produce a 3D image of water structures. The images show the diaphragms to be very flat. In fact these two devices showed only on 500nm variance in height across the entire 150μm diaphragm.

![Fig. 4: Wyko image of a 200μm device](image1)

![Fig. 5: Wyko image of a 150μm device](image2)

![Fig. 6: Wyko image of a 150μm device](image3)

V. CONCLUSION

A surface micro-machined pressure sensor was manufactured. The devices could not be tested due to a short between the control gate and the substrate, but a process of producing a surface process diaphragm was demonstrated. The diaphragms were shown to hold good structure and be very flat across the entire diaphragm. The resist was completely removed from under these devices by using an O₂ plasma. With a few process changes to remove the shorting issue a working pressure sensor should be able to be manufactured. If amplification circuitry was then added to the chip, these devices even have the capability of being microphones.

REFERENCES


By imaging one of the devices that lost the diaphragm, Fig. 7, a profile of the air gap could be taken. This profile shows that from the remaining metal 2 layer down to the nitride layer above the floating gate, there is a 3μm difference. The metal 2 layer was almost exactly 2μm, so this shows an extra 1μm left for the air gap; however, the air gap under actual diaphragms is closer to 2μm. The sacrificial resist layer had some overlap over the unetched ILD. This would bring the overlying metal 2 an extra 1μm above the rest. Some tension in the Al layer would then pull the center of the diaphragm to the same height as the highest metal 2 when the resist was removed and the metal weekend from the openings.
Thermal SiO$_2$ Growth Rate Enhancement at Low Temperatures using an NF$_3$ Additive

Ryan D. Rettmann

Abstract—Thermally grown silicon oxide growth enhancement using small amounts of NF$_3$ was investigated, examining both growth rate and interface quality. Low temperature results showed noted growth rate enhancement at temperatures above 700°C. Interface quality showed significant improvement. Further enhancement is expected through modified chamber and equipment design.

Index Terms—Thermal Oxide, NF$_3$, Gate Dielectric, Thin Film Transistors

I. INTRODUCTION

The introduction of a viable thermal oxide process could remedy several current challenges facing high-mobility TFT applications. Studies have shown potential for enhanced oxide growth and interface state reduction using both NF$_3$ and F$_2$ additives in an oxidizing ambient [1], [4]. This research project revives this study in a new context where a high-temperature rapid thermal process is not applicable.

II. EQUIPMENT SETUP

The test setup was constructed as follows; a horizontal hot-walled furnace with an 800°C torch (for pyrogenic steam) was outfitted with a direct injection NF$_3$ inlet. Figure 1 shows a diagram of the furnace. A mass flow controller rated at 2-8 sccm was used to control NF$_3$ flow. The experiment used 4” p-type bare Si wafers. Flow rates of O$_2$ and NF$_3$ were varied from 2-8 sccm and 2.5-10 lpm, respectively. A temperature range from 600-800°C was investigated. Thickness measurements were performed using a Woollam VASE ellipsometer, a Rudolph ellipsometer, and a Tencor SM300 SpectraMap. Oxide quality was investigated using C-V characteristics measured using an MDC mercury probing station.

III. GROWTH RATE RESULTS

Initial results on screening experiments done at 600°C were inconsistent and non-uniform, and thus further runs were shifted to higher temperatures. Figure 2 shows the dependence of growth rate on NF$_3$ concentration found from oxide test runs performed at 700°C and 800°C. The greatest enhancement in oxidation growth rate was found at a maximum NF$_3$ flow condition of 8 sccm; the O$_2$ flow setpoint at either 5 lpm or 10 lpm showed little effect. Results generally indicated a 2x increase in growth rate. Longer soak runs were performed at 5 lpm O$_2$ and 8 sccm NF$_3$, with results shown in Figure 3. These results along with literature [2-5] suggest that further rate enhancement may be possible using a different gas mixture configuration, and/or a different chamber design.

![Fig. 2. Growth rate dependence on NF$_3$ concentration at 800°C and 700°C for 1 hour.](image-url)

R. D Rettmann is a 5th-year student in the Microelectronic Engineering Department at the Rochester Institute of Technology.
IV. C-V MEASUREMENT RESULTS

Initial electrical measurements were performed using an MDC mercury probe capacitance voltage station. Figure 4 shows a sample of C-V measurement sweep using the Hg probe station. No significant shift in oxide quality was observed between dry and NF3 enhanced growth runs. Derived electrical thickness showed some deviation from optically measured results.

Aluminum capacitors were then fabricated to verify results. Sample wafers were coated with aluminum using a CVC evaporator, patterned, and etched using wet etch chemistry. The wafers were then sintered at 450°C in an N2/H2 ambient.

Measurements were performed on an MDC probing station. Figure 5 shows a sampling of the C-V results.

### Table 1: Electrical Oxide Surface State Thickness Density

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Oxidation Method</th>
<th>Electrical Oxide Thickness</th>
<th>Surface State Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>800°C, 2 hour, 1600 ppm NF3</td>
<td>194 Å</td>
<td>4.51e10 cm^2-2</td>
<td></td>
</tr>
<tr>
<td>800°C, 4 hour, Dry Oxidation</td>
<td>203 Å</td>
<td>1.33e11 cm^2-2</td>
<td></td>
</tr>
<tr>
<td>700°C, 4 Hour, 1600 ppm NF3</td>
<td>209 Å</td>
<td>5.18e10 cm^2-2</td>
<td></td>
</tr>
<tr>
<td>700°C, 12 hour, Dry Oxidation</td>
<td>227 Å</td>
<td>1.32e11 cm^2-2</td>
<td></td>
</tr>
</tbody>
</table>

Significant interface state reduction is observed in the NF3 enhanced growth runs. This is thought to be caused by the influence of fluorine during the growth process; F atoms are suspected to tie up Si dangling bonds as a placeholder for O2 molecules [4].

V. CONCLUSIONS/FUTURE WORK

Growth rate enhancement was observed for temperatures greater than 700°C. However, results from less than 700°C runs were inconclusive. C-V measurement data shows a substantial improvement in oxide quality through the use of NF3. This has significant importance to proposed TFT applications. For this work to be applicable, oxide quality must match or exceed currently available techniques.

Optimizations to chamber design based on previous studies and data from this study are expected to further improve growth rate. By plumbing the NF3 source through the torch, the molecules are expected to dissociate, freeing up the fluorine to interact with the oxide growth.

REFERENCES

Fabrication of Thermally Actuated Micromirror using CMOS Compatible Surface MEMs Process with XeF₂ Release etch

Christopher G. Shea

Abstract—Thermally actuated micromirrors were fabricated to demonstrate a CMOS compatible surface micromachined MEMs process that was developed. A key step in the process was the use of a XeF₂ etch to release the structures. A design was created that varied key factors including mirror pad size and number of anchors. For the smallest pads attached by a single anchor, the length and width was varied. The release etch was found to require a sacrificial layer of greater than one micron for fast lateral undercutting. Mirrors with the longest and narrowest necks were found to display the greatest deflection.

Index Terms—Thermal Actuation, Micromirror, Surface MEMs, XeF₂

I. INTRODUCTION

Micromachined mirrors on silicon substrates have been fabricated for quite some time. Their most notable use is the digital micromirror device (DMD) commercialized by Texas Instruments for television and projectors. The demand for optics-lab-on-chip devices has increased as integrated microsystems become more prevalent. While the DMD works well for its specialized application, its binary nature limits the scope of its use. A thermally actuated micromirror offers analog positioning allowing a much broader range of applications. With this technology optical switching matrices or optical multiplexers are conceivable.

II. THEORY

A. Review Stage

A surface micromachined MEMs fabrication sequence compatible with fully processed CMOS wafers was developed. The design was based upon previous work done at the RIT using bulk fabrication methods [1]. The updated process is constrained to low temperatures (T < 400°C) and makes use of only deposited layers. The devices were formed using a 2 μm layer of tetraethyl orthosilicate (TEOS) deposited above a sacrificial silicon layer with the mirrors defined using reactive ion etch (RIE) to create a trench in the structural oxide. Using a DC magnetron sputtering system, tantalum and aluminum layers were deposited for the formation of heater elements and contact regions, respectively. Polyimide was applied as the actuating mechanism, with a XeF₂ silicon etch used to release the structures. An image of a typical mirror as created by Clever 3D process simulation is shown in Fig. 1.

A mask layout was created to incorporate as many variations of the micromirror design as possible. Varied design parameters included the length, width and number of anchors, as well as the width of the trench etch. Serpentine and ladder resistor designs were used that scaled to the size of the anchors. The polyimide pad placed over the anchors induced a tensile stress when cured, pulling the mirror out of the wafer plane. When heated by the underlying resistor, the large thermal expansion of the polyimide allows the position of the mirror to be controlled. This technique provides analog positioning of the mirror as opposed to the digital versions that are in commercial production today.

III. DESIGN

The design was created in Mentor Graphics Expert layout software. All of the mirrors were created within the 12 pin test probe pad for ease of testing. Three different mirror sizes were created, the largest (1000 x 500 μm) fills the entire pad and had either 1, 2, or 4 anchors. The middle sized mirrors were 500 x 250 μm and had either 1 or 2 anchors. For the smallest mirrors with a square pad 250 μm on a side, the length and width of the single anchors was varied. Six of the single mirrors fit within the test pad with anchor lengths of 0, 50, 100 (x2), 150, and 200 μm. This pad was replicated with anchors widths of 250, 150, 100, and 50 μm. All of the designs were created with the width of the trench defining the mirror as 2 μm, 5 μm and everywhere the mirror structure is not. Mirrors were fabricated with both ladder and serpentine type heater elements. Test structures were included to determine the intrinsic stress of the heater and metal layers as well as their resistivities. Microhotplates were also included in the design as they were compatible with the process sequence. The final cell layout can be seen in Fig. 2. This cell was scaled across multiple form factors (¼X, ½X, 1X, 2X, 4X) to create the final die.
IV. Fabrication

The starting substrates for the process serve only as mechanical supports for the devices. Heavily arsenic doped 6" 100 silicon wafers were used due to their abundance. Onto this 1 μm of oxide was deposited from TEOS in an Applied Materials P5000 at 390° with 500 W. The sacrificial silicon layer was deposited using e-beam evaporation in the CHA. The source for the silicon was a ground up 2" wafer placed into a carbon crucible. The silicon layer was patterned and plasma etched to leave only select release areas. An additional 2 μm of oxide was deposited to form the structure of the mirror. This layer was patterned with the trench layer outlining the mirrors, and the oxide was etched anisotropically in the P5000 RIE chamber.

First attempts to etch the trench caused arcing events in the chamber around the edge of the wafer. It was initially thought that the secondary flats on the wafers were exposing part of the seal. New substrates were acquired that did not have a secondary flat, but were SOI wafers. These wafers were carried through the same fabrication as previously described. Upon attempts to perform the oxide trench etch, the same arcing events were observed. These created large variations in the DC bias of the chamber which caused unpredictable etch rates. The cause was eventually determined to be poor electrical contact with the electrostatic chuck due to the presence of a backside oxide. This was removed by applying a blanket coat of photoresist to the wafers and submerging them in BOE (10:1 DI:HF) for 20 min. Pinholes in the resist coat did allow some HF to attack the oxide, although this did not have a significant effect on yield.

A thin layer of tantalum was deposited using DC magnetron sputtering in the CVC 601. A 4" target was used at a pressure of 5 mTorr with 250 W. The deposition rate was found to be ~100 Å/min. Tantalum was chosen for it high etch resistance and melting point. The etch resistance was required as the heater elements would be exposed during the etching of the contacts. Once patterned the tantalum was etched in a LAM4600 Chlorine etcher. A low power (125 W) recipe was used, and 1500 Å was found to etch completely in 45 sec. Aluminum was deposited in the same DC sputter system using the standard RIT metal process for electrical contacts to the heaters. A power of 2000 W was used for the 8" target at 5 mTorr. The use of an ILD was avoided as the use of vias had caused problems in previous work. The patterned aluminum contacts were wet etched at 50° for 2 min with agitation. The
polyimide used was Durimide 112A, a non-photosensitive film that could be etched by positive developer. The polyimide was applied with a static dispense followed by a 15 sec spread at 600 RPM. Spinning at 2000 RPM for 45 sec resulted in a 4 μm thick polyimide film with relatively good uniformity. Following a stepped softbake at 100° C and 120° C the wafers were coated with photoresist. The develop time had to be reduced to 30 sec due to significant undercutting or the resist. The resist was removed by a simple spray with acetone, followed by IPA and a DI water rinse and spin dry. The polyimide was cured in the Heraus Vacuum oven at atmospheric pressure in a N₂ ambient. The oven was set to 400° C though typically only reached ~350 – 370° C. The thickness of the polyimide layer was measured to decrease from 3.4 μm to 2.4 μm due to the cure. While significant this is not the 50% volumetric contraction the material is capable of.

The devices were released using the Xactix XeF₂ etcher. The system consisted of a XeF₂ source connected to an expansion chamber that allowed the material to sublimate up to its vapor pressure. The expansion chamber is isolated before being opened to a sealed vacuum chamber containing the samples. The system simply pump –purges the chamber with XeF₂ gas, and soaks for a set period of time and cycles.

Due to issues with the initial process runs, a revised process was proposed. A significantly thicker sacrificial silicon layer was deposited to reduce the effects of mass-transport limitations. This was also deposited as polysilicon in an LPCVD system. To further investigate effects of the release etch devices were fabricated on bulk silicon in addition to un-patterned and patterned sacrificial layers, To prevent etching of the heater elements devices were created with aluminum heater elements. This required a slight change to the process sequence as the heater elements were exposed during the etch to form the contacts. To address this 2 μm of aluminum was deposited immediately after the structural layer. Slightly thicker contacts were used here due to concerns about connectivity over the topology from the thick silicon layer. After the contacts were patterned a thin (~2000 Å) layer of aluminum was deposited that served not only as the heater elements but also a hard mask for the trench etch. The rest of the process followed as described above.

V. DISCUSSION OF RESULTS

The arcing events during the trench etch proved to one of the main challenges of fabrication. The arcing appeared to be stemming from the edge of the wafer at the location of the secondary flat. When the SOI substrate wafers were used the same arcing events were observed, however from random location. The oxide on the back of the wafers was causing a charge to build that found the most favorable location on the chuck to arc. Upon removal the system provided a very consistent isotropic etch with a rate of 30 Å/sec. Unfortunately selectivity to resist was only 2:1, however the use of aluminum as a hardmask worked well.

During the release of first lot, the lateral undercutting of devices was observed to self-limit when encroaching etch planes met, leaving a connecting ridge. Figure 3 shows an optical image enhanced by a Nomarski polarizer where the underlying ridge can be seen. This effect was observed to be independent of device area and was present in all form factors.
As it was also seen for all trench widths the effect was determined to be caused by mass transport limitations. A cross section of one of the devices is shown in Fig. 4, where the gap resulting from etched silicon can be seen to decrease towards the center of the device. A small number of devices were released by subjecting them to extremely prolonged etching cycles. These devices were analyzed with the Veeko Wyko NT1100 Optical profiler. An angle of \(-10^\circ\) was determined for the mirrors shown in Fig 5.

Tantalum was also found to be etched by the XeF₂ process, compromising the heater elements. The design allowed the sides of the ladder elements to be exposed, and the tantalum was corroded out from under the polyimide pads. The serpentine resistors all failed due to step height opens over the patterned silicon pads.

In the revised process the lateral undercutting of the release etch increased significantly. Device fabricated on unpatterned silicon fully released from only 60 cycles. An optical image is shown in Figure 6 where the sacrificial silicon can be seen to have almost completely removed.

In order to verify device release, SEM images were taken. Figure 7 shows that all single anchor mirrors fully released and stiction was not an issue. Figure 8 is a close up of the mirrors with the largest anchor aspect ratio. These exhibited the largest degree of deflection. In testing the mirrors were visually verified to move. Additional device testing is ongoing.

VI. CONCLUSION

A CMOS compatible surface MEMs process using a XeF₂ release etch was successfully developed. Thermally actuated micromirrors were fabricated to demonstrate the process. It was determined that during the trench etch, the presence of a backside oxide on the substrates was the cause of arcing events that lead to severe etch rate variability. Lateral undercutting of devices in the XeF₂ release etch was observed to self-limit when encroaching etch planes met, and was independent of device area or trench width. Tantalum was also found to be etched by the XeF₂ process, compromising the heater elements.

In a revised process, a significantly thicker sacrificial silicon layer was deposited to reduce the effects of mass-transport limitations. To prevent etching of the heater elements devices were created with aluminum heaters, though alternate materials could be implemented with refined process rules. An optical profiler was used to determine the angle of the mirrors. Additional process refinements are still under investigation.

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REFERENCES

Process Characterization for Integration of Esaki Diodes into Aspect Ratio Trapping Material

Stuart A. Sieg

Abstract—A process for forming Esaki Diodes in Germanium bulk material was characterized. In doing so its processing characteristics were studied to determine whether it could be transferred into Aspect Ratio Trapping, ART, material. It was determined that transfer was feasible with the optimization of the spin on dopant process and strict control of the wet etching of the spin on dopant and Aluminum. Following process characterization electrical data was collected for a range of devices with varying process parameters. The maximum peak to valley current ratio was 1.5 and maximum peak current density was 5kA/cm². The PVCR value was very close to data collected by a group at Notre Dame who’s process was the basis for the one used in this project. However, the maximum peak current density was much lower, most likely due the decreased dopant concentration of the spin on dopant. Upon completion of the project a process, which could be transferred to ART, was obtained and baseline data was collected for comparison to future devices.

Index Terms—Aspect Ratio Trapping, Esaki Diode, spin on dopant, peak to valley ratio, current density

I. INTRODUCTION

With semiconductor technology continuing to advance into smaller and smaller dimensions it has become increasingly important for new/rekindled areas of device development to progress and lead to new innovation which can lessen the constraints. One such area of interest is in the development of devices in non-silicon material which can lead to different if not better electrical characteristics for new devices. This paper discusses the integration of a process for Esaki Diodes into bulk Germanium and then the difficulties in implementation into Aspect Ratio Trapping (ART) material. By doing so it will allow the confirmation of device operation in non standard material as compared to an already developed process with a more common material base. The process undertaken was adapted from the work done by a group out of Notre Dame.  

II. THEORY

A. Electrical Properties

The Esaki Diode is a device which has its basis as a standard diode, however, during processing the cathode and anode regions of the device are heavily doped leading to degeneracy. The impact of this is to create a junction which allows for electron penetration through the barrier, known as electron tunneling, since the states on both the n side of the junction and p side of the junction will line up over some finite region of applied voltage.

During Esaki operation there are a few regions of interest which are distinctive to a tunneling device and thus the Esaki diode. These states will be shown in two ways, the first through the band diagram and how it is manipulated during biasing, Figure 2, and the voltage-current curve shown in Figure 3.

Figure 1: Band Diagrams at Various Bias Conditions
Initially during non-biased conditions, as seen in (a) of both Figures 1 and 2, there is no current flow since there is no external electric field to drive the tunneling, there can be seen in Figure 1 that there are, however, allowed/occupiable states on both sides of the junction. By beginning the biasing of the junction the condition of (b) is met, where maximum tunneling current is achieved due to the high bias and available states. The current at this point is known as the peak current and is a crucial characteristic of any tunneling device. Biasing the device after the peak current leads to a subsequent valley which is caused by the fact that the states on the cathode and anode side of the device are offset with no overlapping of the states, as seen in (c) of both Figures 1 and 2. With no overlapping of the states there should be, in theory, no current, however, it can be seen at this point that there is some current flow. This is caused by trap states which allow for some electron flow through the barrier. This valley current is necessary for device characterization since it will yield how optimally the device works to inhibit current. The peak current and valley current are often presented as a ratio known as the peak to valley current ratio, PVCR, which allows the determination of the quality of the device. Past the valley the device is highly biased and thus begins to operate as a standard diode, (d) in both Figures 1 and 2.

B. Aspect Ratio Trapping

Aspect Ratio Trapping material, ART, was developed by Amberwave Systems in Salem, NH. In this method a base material, such as Germanium or III-V materials, can be placed onto a host material, such as Silicon with a surface that is free of lattice and thus suitable for device fabrication. In standard methods for placement of one material onto another, without any surface modification, the lattice constants of the material must be taken into consideration. This is due to the fact that since they do not have the same distance between bonding atoms at some point, a thickness, for the deposited material, will be reached which will cause stress induced lattice errors to propagate through the material. This thickness is known as the critical thickness and is of concern since it can be very small for certain material systems which are of interest for unique device fabrication. To alleviate this problem Amberwave Systems uses high aspect ratio trenches, made in Silicon Dioxide on Silicon, to trap lattice errors above which a clean surface is created, as seen in Figure 3, which can then be used for device fabrication.

![Figure 3: Aspect Ratio Trapping side profile](image)

There are many different applications for such material, however, in this case the most notable benefit is for use as a basis for devices which do not use silicon as a bulk material. This is important since it will provide the alternative material for less cost, since it is on Silicon and not in bulk form, and also allow the continued use of semiconductor toolsets which were designed for use with standard Silicon substrates.

C. Process and Material Considerations

The operation of the Esaki Diode is based upon tunneling current through a PN junction. Since this is the case it is necessary that the doped regions are degenerate such that there are available states for electrons to occupy, thus providing for a high tunneling probability. On the same note the doped regions must also form a sharp junction since any grade between them will only act to reduce tunneling probability and thus the peak current to valley current ratio, yielding a non-optimized device. Although the quantum operation of this device is complicated the needs for device fabrication are not.

For development of such a device the needs as laid out above are obtainable through a number of methods. For high doping it is initially expected that an ion implantation method would be instituted for both p and n regions, however, with the need for a sharp junction, ion implantation would not yield a optimum interface due to ion diffusion. The alternative method to this is to use a rapid melt growth technique.

Initially a spin on dopant with a high concentration is used to n-type dope the substrate for creation of the cathode. Following this Aluminum can be deposited onto the surface. When this Aluminum is then heated above the eutectic temperature of 420°C the Germanium and Aluminum will incorporate into one another and upon cooling create a degenerately doped p-type Germanium area. In addition to this is the fact that it is expected that very little of the dopant, Aluminum in this case, will diffuse past the highly doped area.
and thus allow for a very sharp junction. Another benefit to this process is that the doping concentration and depth vs. anneal temperature is well known for Aluminum in Germanium as seen in Figure 4 below, which allows for the optimization of the devices. Also since not all of the Aluminum is incorporated in Germanium as a dopant the remaining layer can be used as a top contact to the device.4

Figure 4: Doping depth and concentration vs. anneal temperature

To undertake testing of the devices it is necessary to make back contact to them as well. This can be done in a multitude of novel methods but the easiest is to recognize the fact that the devices are already serially “wired” across the surface of the bulk germanium. This makes it very easy for testing since top side contacts between adjacent devices is all that is necessary for testing. With this accomplished there are two main parameters which are of particular interest in device operation and characterization. Those two being peak to valley current ratio, PVCR, and current density. PVCR, as stated above, is the ratio between the peak current which propagates through the device during tunneling and then the subsequent minimum current when the tunneling is diminished and normal diode operation begins. This parameter is crucial for tunneling devices such as Esaki Diodes, Resonant Tunnel Diodes, etc since it represents how effectively the devices promote electron propagation through the barrier and then how effectively they prohibit it, thus the quality of the devices. It must be recognized that this device property is dominated by material properties and peak to valley current ratios in the fifties have been obtained which dwarf the 1.5 value seen in many Esaki Diodes. However, the Esaki Diode has a very simple fabrication process as compared to the better performing, but more complicated devices, and was thus the better selection for proof of tunneling device feasibility in Aspect Ratio Trapping material. The second device criterion that is collected for these devices is current density. This parameter is crucial for understanding the ability of the material to promote current flow, thus determining how well it can drive larger circuits, and is especially intriguing to study in Aspect Ratio Trapping material since there is an interest in seeing the effect of confinement based upon the ART’s surface.

III. PROCESS

Initially when undertaking fabrication there were a few departures from the process laid out by the group at Notre Dame. First was that the bulk germanium sample used was not an optimized sample for the process since it was not specifically obtained for this project. It was of unknown doping and the orientation was not specified, meaning the diffusion of the n-type dopant may or may not have been optimized to create the highest doping or sharpest junction. This was not a roadblock as much as a nuisance since the Esaki fabrication was highly robust as will be seen later. With that said the first step was to introduce the n-type dopant. This was performed using an Emulsitone Phosphosilica film with a dopant concentration of $5 \times 10^{20}$ atoms/cm$^3$, which deviated from the model process that implemented a much higher concentration spin on dopant.4 Before applying the film the surface of the germanium was prepared using a DI rinse followed by a rinse in isopropyl alcohol. The spin on dopant was then applied using a coater for 60 seconds at 3000 rpm followed by a high temperature bake at 200°C for 15 minutes to drive out solvent and densify the film. The film underwent the drive in step using an AG 410 Rapid Thermal Processor at 800°C for 5 minutes, it was at this step that the first experiments were conducted to determine the impact of temperature on diffusion and thus electrical characteristics. The film was then stripped in 10:1 BOE. Following the strip it was clear that the film was not being fully removed from the surface and led to what looked to be cracking on the germanium surface. This problem was alleviated using a decreased spin time, 8 seconds, to increase the thickness of the film and a two step bake, 100°C for 15 minutes, followed by the 200°C bake for 15 minutes. Implementing this process led to the clearing of the surface properly after the BOE strip.

With the n-type doping region created in the germanium the next step was to create the aluminum contact and p-type region. The aluminum was deposited as Aluminum with 12% Silicon using a CVC601 DC Sputtering system at a thickness of roughly 1000Å. The Aluminum was then patterned using a contact lithography system and wet etched using a solution containing acetic acid, phosphoric acid and nitric acid. The patterned Aluminum then underwent a spike anneal at around 550°C for 1 second. This temperature was varied to determine effect on electrical characteristics. This completed device fabrication and thus led to device testing.

IV. RESULTS

Since the main purpose of undertaking this process was to prove the feasibility of instituting the process developed by Notre Dame4 and to understand its nuances in regards to processing in ART based material, much of the information gained was not for electrical purposes but material characterization. In terms of material characterization the largest challenge was in implementation of spin on dopant.
A small experiment was undertaken to show the effect of each as seen in Figure 6 and 7, it can be seen that until both were implemented the surface was not optimized, Figure 8. It has been postulated that this cracking effect occurred due to dopant suspension solvent interaction with the surface.

Another issue which needed to be understood was that dealing with the etching chemistries. Since ART material is based upon a grating of alternating Silicon Dioxide and structure material, in this case Germanium, the BOE will undoubtedly attack the Silicon Dioxide during dopant strip. This means that extra care must be taken during this step such that the Silicon Dioxide isn’t overly exposed thus weakening the structure and possibly causing shorts. On the same note it was determined that the Germanium was etched by the Aluminum etching chemistries thus yielding the same concerns as with the dopant etch. The Germanium etching can be seen in Figure 9 with the large slope beneath the aluminum areas. In the future these two issues may be resolved by implementation of dry etch and lift off resist processes.

During implementation it was found that under the initial process conditions for application, 60 second spin at 3000rpm and then subsequent 200C bake and 800C drive-in, the surface would appear cracked as in Figure 5. To alleviate the issue both a two step densification, 100C and 200C, and a decreased spin time, 8 seconds, were implemented.
In undertaking electrical testing two separate designs of experiment were conducted to determine the effect of anneal temperature, aluminum-silicon thickness and drive-in temperature on the electrical characteristics of the devices. The first experiments specifically targeted how the diodes responded with varying anneal temperatures of 530°C, 550°C and 570°C with no other variations in processing conditions. Under these circumstances there appeared to be a change in the maximum peak current density and the max peak to valley current ratio as seen in Figures 10 and 11, however, the data is skewed since so many data points showed a very low PVCR for all temperatures and such a wide variation in peak current density.

The second experiment dealt with all three of the aforementioned process conditions with settings as seen in table 1. It was found that although tunneling was found in each case there was not enough data gathered to provide any distinct difference between any process condition set since the range of values was so high and thus the standard deviation, as seen in Figures 12, 13 and 14. This did not result in a failure of the experiment since it showed that the process was very robust and thus suitable for implementation in ART material. The data did show that maximum values for PVCR of roughly 1.5 were obtainable which was what was reported at Notre Dame for peak to valley current ratios. Figure 15 below shows much of the data collected during this project vs. anneal temperature and Figure 16 shows the IV characteristic of the device with the highest PVCR. All of this information is crucial for comparison to ART devices to determine the impact of the alternative material.

Table 1: Experimental Design Matrix

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<th>Set</th>
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<th>Anneal Temperature</th>
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V. CONCLUSION

By undertaking the implementation of a process to fabricate Esaki diodes in bulk germanium a process for implementation in non standard material has been obtained. Initially concerns of etching in BOE were examined and it was determined the best option was to ensure correct timing in the etch. At the same time it was found that the Germanium was being etched at a very high rate by the chemistries of the Aluminum etch. This was unexpected and therefore yielded important knowledge for implementation into ART based material, where it is imperative to have the least amount of unnecessary surface manipulation as possible. To alleviate this issue timed etches were instituted, however, another method for counteracting this effect would be the institution of a lift off resist process for removal of the patterned Aluminum. Material characterization also yielded knowledge into the processing conditions of the spin on dopant where a more satisfactory process was necessary to correct for inferior surface quality seen with basic processing conditions. For electrical testing two designed experiments were performed on a variety of process conditions to determine effect on peak to valley current ratio and current density. In both experiments a few trends were seen on the surface, but due to the range of variation, in both PVCR and peak current density, there were no trends that could be considered statistically significant. What could be said was that the process was very robust since most devices across a sample exhibited tunneling characteristics and that the maximum PVCRs were the same as those seen in other studies. Future research into this process should yield a more optimized method, however, at the moment this process could be implemented into ART material and provide operational devices for characterization.

ACKNOWLEDGMENT

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REFERENCES

Biomedical Lance Ion Sensitive System

Charles D. Sturdevant, RIT Microelectronic Engineering

Abstract—The fabrication of a pH sensor which can be used in practical applications in biological and medical fields was designed and manufactured using a new lance style ion sensitive field effect transistor. The lance can be used to measure pH levels in micro biological cultures without disruption of the culture and can be a powerful tool in real time Invitro medical diagnostics tool.

The reference electrode can be placed onto the chip by depositing a noble metal contact in the field region. This is referred as a Pseudo Reference Electrode, PRE. By bringing the PRE design closer to the membrane, the active test area for the ISFET will then be contained to the small perimeter of the gate. Also, with the PRE being very close to the gate membrane, a larger percentage of charged ions will interact with the membrane which can allow for a smaller gate membrane and still have strong sensitivity. The combination of these two benefits can create a very compact Perimeters PRE ISFET design.

With this compact design, it can be implemented on a MEMS cantilever for new testing methods in the medical and biological fields. By combining the ISFET device at the tip of a cantilever, the device can be put into use to test with minimum impact.

Deep silicon etching was attempted using a protective front side coat and a hot KOH bath to etch a patterned backside. Complications in preserving sensitive ISFET components needs to be resolved before completion of freestanding cantilever lance MEMS probe with ISFET sensor.

I. INTRODUCTION

Ion sensitive field effect transistors, ISFET, are traditionally to large and impractical for bio probe applications. An ISFET device has 5 main components. Figure 1 shows a basic ISFET design. ‘A’ is a reference electrode that is suspended in the solution. The reference electrode is traditionally off chip. The charge increase Ion activity, increasing the sensitivity to the solution pH. ‘B’ is the ion sensitive gate. The gate traditionally is very large, so as to be exposed to as many ions in the solution as possible. It is usually comprised of a dielectric and a sensitive membrane. The membrane is an important aspect that shows different sensitivity characteristics. ‘C’ is an ion filled solution that has to large enough to cover both the reference electrode and the gate membrane. ‘D’ is a thick protective oxide needed to protect the source and drain from the ion solution and reduce ion contamination. ‘E’ is the source and drain components of the ISFET and are the means of sensing the Vt adjust cause during the ion interaction with the gate membrane.

The ISFET is a relatively large device. The reference electrode can be placed onto the chip by depositing a noble metal surface contact in the field region. This is referred as a Pseudo reference electrode, PRE. Figure 2 shows a type of PRE design.

The problem with this type of PRE design, a very broad testing area is needed and the sample solution must carry the charged electrons laterally instead of near the gate membrane. By bringing the PRE design closer and membrane, the active test area for the ISFET will then be contained to the width of the gate. Also, with the PRE being very close to the gate membrane, a larger percent of charged ions will interact with the membrane which can allow for a small membrane. The combination of these two benefits can create a very compact ISFET. Figure 3 shows a Perimeters PRE ISFET design.
With this compact design, new applications can open for the sensor. Previously, with the need for an exterior electrode, the solution needed to be fairly large. With the PRE, the solution needed to be placed onto a chip. With the new smaller design, the ISFET can be more flexible in its applications. One application that was not viable with the previous designs is the opportunity to be manufactured at the end of a MEMS probe lance. With a very fine probe, medical testing and biological applications expand greatly. The ability to test acidic level in burn wounds, damaged tissue, and the ability to detect body chemistry changes instantly during surgery can be crucial information for medical professionals. This can be done using a compact ISFET design that can be manufactured on the end of a MEMS lance.

II. Procedure

Four inch n-type wafers are used to create the PMOS ISFET device. The wafers are thinned using a wafer grinder on the backside of the wafer and a CMP tool to reduce the thickness to approximately 330um. The wafers are cleaned in a RCA clean cycle. Oxide is grown in a wet furnace to create a mask for the active regions device. The oxide is patterned using a contact aligner and is etched in the active areas. A p-type spin on glass is used to dope the PMOS source and drain. The oxide is removed. A pad oxide is grown for a nitride backside pattern. The nitride is removed from the front of the wafer using a SF6 plasma and the pad ox is removed in a BOE 10:1 bath. The backside is patterned using the front side active mask to align in the contact aligner. The patterned nitride is etched using a SF6 plasma and the oxide pad is removed in a BOE 10:1 bath.

A 140nm wet oxide is grown in a furnace. Contact cuts to the active area are patterned using a 5x g-line stepper and etched in a BOE 10:1 bath. A 600nm LPCVD Poly silicon layer is grown over the oxide and is doped with a p-type spin on glass. The poly silicon is patterned using a 5x g-line stepper and etched in SF6 plasma. A thick 1um oxide is deposited using a TEOS deposition tool to protect the source, drain, and poly silicon from the electrolyte solution.

The gate is patterned using the 5x g-line stepper and is etched using a BOE 10:1 bath. The photo resist is removed before a dry 25nm gate oxide is grown. A lift off process is used to deposit the Al2O3 so to limit acid contamination to the gate membrane. The 5x g-line stepper patterns the Al2O3 membrane before deposition. An electron beam evaporation tool is used to deposit 40nm of Al2O3 onto the wafer. The photo resist is removed in an ultrasonic acetone bath.

Poly silicon to pad contacts are patterned using the 5x g-line stepper and etched in a BCl3 10:1 bath. The gold perimeter PRE pattern is also a lift off process. The PRE is patterned using the 5x g-line stepper before metal deposition. An electron beam evaporation tool is used to deposit a 50nm chrome layer followed by a 150nm gold metal contact. The photo resist is removed in an ultrasonic acetone bath.

The front side of the wafer is etched to define the thickness and edges of the lances. The front side etch is patterned on a 5x g-line stepper and is etched using an SF6 plasma. The etch recess is approximately 30um. The wafer is then etched from the backside with the nitride pattern. The front side of the wafer is protected with a Brewer Science Protek B3 product. A Protek primer is spun and baked on the front and edges of the wafer, followed by the Protek B3. The wafer is etched in a 75°C KOH bath for 3 hours. The wafers are cleaned in a KOH decontamination bath. The Protek is removed using a solvent strip and the front side is cleaned using an acetone ultra sonic bath to remove residue.

III. Results

The first wafer was observed after the KOH three hour etch. The front side of the wafer showed signs of partially etched regions. The Protek product is optimized to adhere to a SiO2 surface. The top etched region was largely bare silicon. The Protek did not properly adhere to the bulk silicon or the Al2O3 gate. Only the thick oxide and gold coated regions were protected with the Protek. The front side etched silicon increased from 30um to 90um, suggesting that the KOH only etched for approximately one hour on the front side. Figure 4 shows a SEM image of the front side of the devices.
The **Protek** is a stackable film that can be layered. The bulk of the device was properly protected. Using the **Protek** to adhere to itself in multiple layers can be used to bridge the gate and protect the membrane during the etch.

If the **Protek** cannot protect the gate membrane due to adhesion, a deep silicon etch can be used to release the lances. Using a thick photo resist such as SU-8, a long SF6 plasma etch can be used to remove the bulk of silicon under the lance using the backside lithography step at the end of the process.

**IV. CONCLUSION**

The perimeter PRE ISFET design was successfully designed and manufactured. The integration of the design onto a lance cantilever MEMS was unsuccessful due to complications in deep silicon etching processes. Further work can produce a freestanding lance with an ion sensitive field effect probe.

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Dr. Lynn Fuller, Ivan Puchades, Sean O’Brien, Victor Prajapati,

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Characterization of P-N Junctions for Variation in Dose and Annealing Temperatures (May 2008)

Ryan Sweeney, Microelectronic Engineering, Rochester Institute of Technology

Abstract—The following experiment was completely in order to analyze and quantify the influence implantation dose and post implant anneal conditions have on the source and drain regions of a typical transistor. A DOE experiment was designed to investigate three different variations in each the implantation dose and post implant anneal temperatures of the source and drain regions of the advanced CMOS process transistor at RIT. Electrical characterization was used to obtain quantifiable results for each experimental variation. The experiment was successful in manufacturing a complete analysis for variations in the source and drain doping profile.

I. INTRODUCTION/THEORY

Device characterizations of basic building block structures of the CMOS transistor are necessary in designing improvements in overall functioning of the transistor. The source and drain regions of a typical transistor can be profiled and experimentally improved by researching variables related to basic PN junction diodes. In this experiment, P/N junction diodes were made to simulate the source and drain regions of a typical PMOS transistor. The experiment was designed to examine the influence that P+ implantation dose and post implant anneal temperatures have on the source and drain electrical characteristics and physical profile. Electrical analysis was accomplished by measuring data for I-V curves for each processing split. Characteristics of the diode, such as series resistance, breakdown voltage and ideality factor, can be extrapolated from the measured curve. Series resistance is related to the slope of the log(I)-V curve at the point in which it deviates from linearity[1]. The breakdown voltage is the point on the I-V curve in which current begins to flow at reverse bias conditions.

Fig. 1 consists of a table that outlines the different DOE splits for each wafer in the experiment. The P+ implant was varied from 1x10^{13} to 1x10^{15} cm^{-2}. Also, the anneal temperatures were varied from 900 to 1100°C. It is important to note that the 900°C anneal was done by a rapid thermal process. The 1000°C anneal was performed by a 20 min soak in a furnace with oxide growth present. The 1100°C anneal was processed by a 20 min soak in N_{2}. Fig. 2 shows the theoretical cross-section of the desired device in the experiment. The desired device includes an N+ implant to make improved contact to the well.

II. RESULTS/ANALYSIS

Devices were successfully created for each process variation step. The devices manufactured were simple P/N junction diodes, which are representative of the source and drain structures of a typical transistor. A top-down picture of the manufactured devices can be seen in Fig. 3. The P+ implant was done in the small 8x8 μm² structure viewable in Fig.3. The U-shaped structure in the figure is where the N+ implant was implanted and the white area is the metal layer overlaying both implants.
In Fig. 4 breakdown voltage was extracted from the I-V curves for each process split in the experiment. The table shows a sizeable increase in breakdown voltage for the 1100°C anneal. Higher breakdown voltage for PN junctions within the transistor is desirable to limit current leakage. Based on the results, an increase in anneal temperature is ideal to improve breakdown voltage, although temperature increases in transistor manufacturing is not always possible dependent upon material properties throughout the transistor. Also, there is an apparent increase in breakdown voltage dependent upon P⁺ implant dose. This increase is significant between 1x10¹³ cm⁻² dose and the two higher implants.

<table>
<thead>
<tr>
<th>W1</th>
<th>Breakdown Voltage (V)</th>
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<tbody>
<tr>
<td></td>
<td>-6.35</td>
</tr>
<tr>
<td>W2</td>
<td>-6.42</td>
</tr>
<tr>
<td>W3</td>
<td>-7.61</td>
</tr>
<tr>
<td>W4</td>
<td>-8.96</td>
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<td>W5</td>
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<tr>
<td>W6</td>
<td>-13.09</td>
</tr>
<tr>
<td>W7</td>
<td>-8.37</td>
</tr>
<tr>
<td>W8</td>
<td>-8.61</td>
</tr>
<tr>
<td>W9</td>
<td>-11.32</td>
</tr>
</tbody>
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Fig. 4. Breakdown Voltage for each wafer and DOE split measured in volts.

<table>
<thead>
<tr>
<th>W1</th>
<th>Leakage Current at -5V (µA)</th>
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<tbody>
<tr>
<td></td>
<td>511.91</td>
</tr>
<tr>
<td>W2</td>
<td>449.55</td>
</tr>
<tr>
<td>W3</td>
<td>356.75</td>
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<tr>
<td>W4</td>
<td>0.0061</td>
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<tr>
<td>W5</td>
<td>122.1</td>
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<tr>
<td>W6</td>
<td>45.59</td>
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<tr>
<td>W7</td>
<td>98.3E-6</td>
</tr>
<tr>
<td>W8</td>
<td>60.21</td>
</tr>
<tr>
<td>W9</td>
<td>241.4</td>
</tr>
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</table>

Fig. 5. Leakage current at -5V reverse bias for P⁺n diode for each wafer and DOE split.

The ideality factor of the P⁺N junction diodes can be extracted from the forward bias I-V curves in Fig. 7. The slope of the quasi neutral recombination region of the curve is related to the ideality factor by the following expression:

\[ n = \frac{1}{2.3 \times \text{Slope} \left( \frac{kT}{q} \right)} \]

The ideality factor is a measure of how 'ideal' a diode is behaving from theoretical expectations. Fig. 8 shows a table of the extracted ideality factors of the devices manufactured. The devices that received the lowest implant dose functioned more ideally than those at higher implant doses.

Fig. 6. Log(I)-V Curve. Reverse bias conditions are highlighted for each set of doping variations.
ACKNOWLEDGMENT

A special thanks is extended to the SMFL staff, RIT Microelectronics Department faculty and students and everyone else whom helped make this project a success.

REFERENCES


Fig. 7. Log(I)-V Curve. Forward bias conditions are highlighted for each set of doping variations.

<table>
<thead>
<tr>
<th></th>
<th>Ideality Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1</td>
<td>1.175</td>
</tr>
<tr>
<td>W2</td>
<td>1.141</td>
</tr>
<tr>
<td>W3</td>
<td>1.172</td>
</tr>
<tr>
<td>W4</td>
<td>1.544</td>
</tr>
<tr>
<td>W5</td>
<td>1.503</td>
</tr>
<tr>
<td>W6</td>
<td>1.302</td>
</tr>
<tr>
<td>W7</td>
<td>1.406</td>
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<tr>
<td>W8</td>
<td>---</td>
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<td>W9</td>
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</table>

Fig. 8. Extracted Ideality Factors from slope of quasi neutral recombination region of the forward bias I-V curves.

III. CONCLUSION

Overall, there were significant effects on device characteristics due to variations in implant dose and post implant anneal conditions. These effects were able to be quantified using electrical testing to produce I-V plots. The plots were then used to extract desired data to further characterize the devices. These results demonstrate the ability to improve transistor performance by experimenting with process conditions on basic components of the transistor.
Fabrication of aligned metallic structures based on block copolymer lithography

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Abstract—The objective of this project is to fabricate linear metallic patterns based on block copolymer lithography. As the semiconductor industry continue to seek scaling methods, the next breakthroughs in the electronics size barrier are likely to come from devices created out of novel material. Block copolymers have gained considerable potential for nanoelectronics applications such as lithography templates due to its incompatible components self-assemble into well-ordered structures with the scale of 10 to 100nm. In this project, creation of nano-scale structures was attempted via graphoepitaxy, a process where topographically patterned substrate is utilized to control crystallographic orientations. Linear structures of diblock copolymer, Polystyrene-block-poly(2-vinylpyridine) (PS-b-P2VP) were assembled within micro trenches, followed by chemical etching and decoration with gold nano-particles to form metal wires.

Index Terms—Nanofabrication, Block copolymer lithography, Self-assembly, Nanostructures

I. INTRODUCTION

In the past decades, diblock copolymer have gained considerable potential for nanoelectronics and nanotechnological applications due to its amphiphilic macromolecules self-assemble into well-ordered structures [1]. Among these applications, several researchers have demonstrated used of block copolymer for lithography process with the scale of 10 to 100nm [1-3]. Nanoscale patterns based on self-assembly have been considered as alternative to replace high-resolution lithographic technologies such as X-ray, electron beam and interference lithography to enable continuation of device scaling [1]. International Technology Roadmap for Semiconductors (ITRS) identified directed self-assemblies of molecular structures as a next emerging patterning technology for 16nm half pitch or beyond [4]. The phase segregating block copolymer represents a promising evolutionary step forward in resist technology. These high information content resist materials are designed to make use of additional nanoscale chemical processes that can be tuned to enhance dimensional control [4]. In the case of implementation to traditional IC fabrication processing, minimum changes will be required because a specific copolymer automatically self-assemble into desired nanoscale structures such as parallel lines for buses or nanoparticles for floating gates. The possibilities for these materials are numerous because of their potential for parallel processing of features along with the simplicity of handling [2].

Many potentials of diblock copolymer for different nanoelectronic applications have been proposed based on their ability to form organized pattern. However, the main challenge of using block copolymer is controlling of nanostructure. Block copolymer alignment has been explored using electric field, shear stress, imprinting, and other methods [6-7]. In this paper, a particular emphasis is made on one processing approach: graphoepitaxy. Graphoepitaxy is a process where topographically patterned substrate is utilized to control crystallographic orientations [1]. As a polymer solution is coated on a substrate with surface relief, block copolymer cylinders forms aligned structures due to controlled confinement. Smith et al originally developed this method in 1978, but it was not until 2001 that graphoepitaxy was utilized to control orientation of block copolymer [1, 8]. This is a prime example of the combined top-down and bottom-up approaches to pattern nanostructures, where both photolithography and molecular self-assembly are utilized. In this experiment, to create aligned linear metallic structures, diblock copolymer, polystyrene-block-poly(2-vinylpyridine) (PS-b-P2VP), was assembled within photolithographically patterned trenches, followed by decoration with gold nanoparticles and chemical etching. The potential application of this method includes nanoscale interconnects; yet it is highly versatile because the user has the control of choosing substrate materials.

II. THEORY

A. Diblock copolymer

A copolymer is any polymer that is built from more than one monomer type. The family of copolymers made from two
monomer types, A and B, can exist as one of three forms: Random, alternating or block. A random copolymer is characterized by a random ordering of the A and B monomer units in the polymeric chain, such as BBABAAABBBBABB. Alternating copolymers exhibit a regular alternating pattern of monomer units in the polymeric chain, such as ABABABABABAB. Block copolymers represent an unusual class of polymers that are synthesized from two or more distinct homogeneous polymeric blocks. For the case of a diblock copolymer, the structure might correspond to AAAAAAAAAAAAAA-BBBBBBBBBBBB and be represented by the blue and red sections of the polymer chain in Figure 1. Diblock copolymers consist of two chemically different polymer chains jointed by a covalent bond. Because of connectivity constraints and the incompatibility between the two blocks, diblock copolymer spontaneously self-assemble into microphase-separated nanometer-sized domains that exhibit ordered morphologies at equilibrium [9]. The chain lengths of the blocks determine the resulting morphology. The size and periods of these microdomain structures are governed by the chain dimensions. Selective processing of one block relative to the other is possible by use of chemical or physical dissimilarities between the two blocks.

Asymmetric PS-b-P2VP diblock copolymer was used in this study as shown in Figure 1. The polydispersity index of copolymer is about 1.05 and molecular weights are 32,000 g/mol and 12,500 g/mol for the SP and P2VP respectively. The glass transition temperatures of PS and P2VP are about 100 °C and 140 °C. The P2VP block has a proton acceptor owing to the 2-pyridyl groups, in which nitrogen is not bonded with adjacent carbons, as well as the potential to act as a metal ligand to combine with metal complexes [10]. As the polymer contact with acidic solution ($\text{pH} < 4.5$), a protonation of P2VP occurs, and it alters the polymer structures, swelling of the P2VP block. The protonated P2VP block carries a net positive charge, and thus anionic metallic particles are required for metal loading.

C. Metal deposition

A monolayer of spin coated PS-b-P2VP does not exhibits clear topography due to its polymer structure where P2VP cylinders are embedded in PS layer. The PS block forms a hydrophobic barrier between the P2VP and the aqueous solution, preventing efficient contact between P2VP and the ionic metals [2]. To induce protonation of P2VP, the polymer-coated substrate is immersed in the HCl (aq.) solution. Upon exposure to acid the P2VP cylinders are swelled up to the surface due to expansion of polymer structures, making direct contact with the ionic metal solution. The negative charge on the anionic metal, AuCl₄⁻, leads to an electrostatic bonding with the cationic P2VP surrounded by PS matrix. The hybrid structure is then reduced and PS is removed with a brief chemical treatment using toluene.

Fig. 3. Schematic diagram of the metal decoration on P2VP of diblock copolymer, PS-b-P2VP. The protonation of P2VP causes swelling to the polymer surface, and the ionic metal salt AuCl₄⁻ become electrostatically bonded to the protonated P2VP surrounded by the PS matrix. The hybrid structure is then reduced and PS is removed in toluene solution.
III. MATERIALS

A. Diblock copolymer solution and ionic metal solution

The asymmetric diblock copolymer PS-b-P2VP (Sigma Aldrich) was obtained with polydispersity index $= 1.05$ and molecular weights of 32,000 g/mol and 12,500 g/mol for the PS and P2VP respectively. The PS-b-P2VP was diluted with chloroform to make 1% solution. HAuCl₄ (99.999%) was purchased from Sigma-Aldrich.

B. Substrates

A silicon wafer (100) was patterned with a series of 10mm long, 40nm deep channels via photolithography and etching in inductively coupled CHF₃ plasma. Channel widths of 400 and 500nm were produced. Prior to copolymer coating, the substrate was cleaned thoroughly in O₂ plasma to remove photoresist and etch residues. Substrates without surface topographies were also prepared and cleaned in acetone and methanol baths.

IV. EXPERIMENT

All the experiments were performed under ambient conditions at room temperature unless specified. To obtain conformal monolayer of block copolymer solution on the substrates, spin speeds were carefully modified. Polymer film thicknesses were measured using Tencor P2 profilometer, and a spin speed vs. thickness curve obtained. The degrees of polymer spreading were characterized via atomic force microscopy (AFM) for different spin speeds. The spin speed was optimized at 1500 rpm.

The effect of micro-trenches on block copolymer alignment was studied by spin coating polymer solution on the topographically patterned substrate, followed by AFM measurement.

Annealing temperatures and time were investigated to obtain block copolymer self-assembly within the trenches. The patterned substrates coated with polymer solution went through various annealing conditions, altering temperatures and time. A polymer alignment was observed after the annealing at 220 °C for 24 hours.

The chemical etching of polymers was studied by immersing three substrates coated with polymer solution into toluene bath for 1, 3, and 10 minutes. AFM measurements were taken to compare etching effects on each sample.

To decorate P2VP with gold nanoparticles, the polymer-coated substrate was immersed in the gold aqueous metal salt solution for 10 minutes. The metal salt/acid solutions were prepared by mixing 1mL of 20mM HAuCl₄ and 9mL of 1% HCl (aq.). The samples were rinsed with DI water and dried under a nitrogen stream. Toluene etch was performed for 30 seconds to remove PS form polymer matrix.

V. RESULTS AND DISCUSSION

Figure 4 shows the spin speed vs. polymer film thickness curve obtained for 1% PS-b-P2VP dissolved in chloroform, and Figure 5 shows AFM images of block copolymer coated on substrate with 800 rpm and 3000 rpm. A slow spin speed leads to concentrated polymer orientations and overlapping of polymer structures can be observed. A high spin speed causes high degree of spreading of polymer structures, and spacing between polymers is wider. Modifying the spin speeds as 1500 rpm controlled the thickness of the polymer films to be 60 to 80nm, and a conformal monolayer of copolymer was obtained.

![Fig. 4. Spin speeds vs. polymer film thickness curve obtained for 1% PS-b-P2VP in chloroform. The spin speed was optimized to obtain a uniform monolayer at 1500 rpm.](image)

**Fig. 4.** Spin speeds vs. polymer film thickness curve obtained for 1% PS-b-P2VP in chloroform. The spin speed was optimized to obtain a uniform monolayer at 1500 rpm.

![Fig. 5. AFM images of block copolymer PS-b-P2VP coated on substrate with (a) 800 rpm, and (b) 3000rpm. A slow spin speeds causes overlapping of copolymers, and a high spin speeds leads to more spreading polymer structures.](image)

**Fig. 5.** AFM images of block copolymer PS-b-P2VP coated on substrate with (a) 800 rpm, and (b) 3000rpm. A slow spin speeds causes overlapping of copolymers, and a high spin speeds leads to more spreading polymer structures.

Figure 6 shows AFM images of 400nm wide and 40nm deep micro-trenches created via optical lithography and deep RIE, and block copolymers spin coated on the topographically patterned substrate. The fingerprint self-assembly of block copolymers was still observed, and self-alignment does not occur in the absence of proper annealing process.
Fig. 6. AFM images of (a) 400nm wide and 40nm deep micro-trenches created on substrates, and (b) block copolymer coated on substrate with micro-channels. The self-assembly of block copolymer does not occur in absence of the annealing.

Figure 7 shows AFM images of block copolymers self-assembled within the micro-channels after an annealing at 220 °C for 24 hours under atmospheric pressure. In the three dimensional picture, the green lines indicate edges of micro-trench, and the red lines indicate self-aligned P2VP polymer structures. The width of P2VP was measured as 40nm. Annealing above the glass transition temperature of copolymers and gradually cooling down create a reflow of the polymer networks into the trenches, organizing self-aligned structures.

Figure 8 shows AFM images of block copolymer spin coated on substrates and etched in toluene solutions for 1, 3, and 10 minutes. A high degree of P2VP concentration was observed after 1 minute etching because PS was removed from the top surface, and 3 minutes etching removes most of P2VP, creating wider spacing between polymers. After 10 minutes of toluene etching, no structure was observed, removing all the copolymers. It has been cleared that toluene etches two polymers at dissimilar etch rates. To remove all the PS and retain a high concentration of the P2VP, the etch time was optimized as 30 seconds.

VI. CONCLUSION

It was the purpose of this investigation to fabricate aligned metallic structures via block copolymer self-assembly. Alignments of polymer structures within photolithographically patterned trenches have been demonstrated using graphoepitaxy. Spin coating was modified to obtain a monolayer of copolymer film. The effects of annealing process on polymer alignment and the optimal annealing conditions were studied. The chemical etching of block copolymer was investigated to selectively remove one kind of polymers from a mixed polymer matrix. Additional studies need to be performed regarding same copolymers with smaller molecular weight, and different conductive materials such as aluminum, capper, or CNTs.
Fig. 8. AFM images of block copolymer PS-b-P2VP spin coated on substrates and etched in toluene solution for (a) 1 min, (b) 3 min, and (c) 10 min. Toluene etches PS faster than P2VP, but 10 min etch removed all the copolymers.

ACKNOWLEDGMENT

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REFERENCES


Yusuke Takahashi is originally from Chiba, Japan, received a B.S. degree in Microelectronic Engineering from Rochester Institute of Technology in 2008. He obtained co-op work experience at Infotronics Technology Center in Canandaigua, NY, and also worked as a research assistant at Micro and Nano Manufacturing laboratory at RIT.
Electrolysis-Bubble-Actuated Micropump

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Abstract—An electrolysis-bubble-actuated micropump is created. The pump is created with a top surface gradient across the channel. This changing gradient will help to propel the bubble, created by electrolysis, forward. This micropump is implemented by taking advantage of both surface tension effect and the electrolysis actuation. The surface tension effect is controlled via the periodic generation of electrolytic bubbles and the roughness gradient design of the microchannel surface. The fabrication of the device was completed following the processes outlined in the design phase. Adhesion problems between the top surface and the silicon substrate were encountered during testing. As result, new layer for better adhesion needs to be implemented in future designs.

Index Terms—Bubble, electrolysis, microelectromechanical systems (MEMS) micropump, roughness gradient, surface tension.

I. INTRODUCTION

MICROPUMPS have been the subject of extensive research in both academia and the private sector. In addition, they have been produced in a variety of designs that use different actuation mechanisms. Diaphragm micropumps [1] for example, achieve a high volume through a large chamber by using a membrane: however, most techniques for fabricating such diaphragm-based pumps are complicated and involve many photolithographic steps. Another technique [2, 3] drives fluid by applying a high voltage to it. Among such approaches, bubble-actuated valveless micropumps are attractive for their simple operation, miniaturized size, large actuation force, and the ability to physically comply to different types of microchannels with a wide range of cross-sections. Although demonstrated successfully in [4-6], these valveless pumps require a complex time-sequenced power control on many electrodes pairs and a large or long nozzle-diffuser structure. Moreover, further disadvantages include the need for a sealed reservoir inside the fluidic chip.

To overcome the problems presented by other pumps, the top surface of this micropump will have a simple patterned surface with different roughness across in order to propel the bubble that is created forward. This micropump is implemented by taking advantage of both surface tension effect and the electrolysis actuation. The surface tension effect is controlled via the periodic generation of electrolytic bubbles and the roughness gradient design of the microchannel surface.

Compared with other actuation mechanisms, the electrolysis bubble actuator has the features of simple structure, low-power consumption, room temperature operation, and being easy to be integrated into a lab chip. The advantage of this design is the low power consumption and room temperature operation.

II. DEVICE OPERATION PRINCIPLE AND MICROFABRICATION PROCESS

A. Operation Principle

Figure 1 illustrates the design concept. The device consists of polysilicon electrodes, a hydrophilic microchannel, and a hydrophobic lateral breather connected to air for the elimination of bubbles. The pumping principle—shown schematically from the side in Figure 1(b)—relies on surface tension and multiple bubble-actuation cycles. The actuation mechanism is divided into three phases: bubble generation, degassing, and liquid movement. First, the bubble is generated by electrolysis to push the liquid in whichever direction is required. Next, the bubble is vented out through the lateral breather. At the sides of the microchannel, surface tension exerts a pull on the liquid that creates a characteristic concave shape called a meniscus. Due to the roughness gradient design, the apparent contact angle of the leading meniscus (right) is larger than that of the trailing meniscus (left): \( \theta_L > \theta_R > 90^\circ \). Thus, the pressure on the left is larger than that on the right: \( P_L > P_R \). As a result, the menisci respond with different velocities, and a net pumping flow along the x direction is achieved. Displacement of the liquid occurs through repetition of these cycles.
Then the volumetric displacement of liquid and the pumping rate are dominated by the geometry design of the microchannel, the design of the roughness gradient surface, the frequency and amplitude of the applied voltage, and the design of the electrodes. All details will be described with the experimental results later in this paper.

B. Microfabrication

The microfabrication process for our micropump is illustrated in Fig. 1(a). First, a standard n-type 100 silicon substrate is grown with the thermal oxide of 500Å. Then 1500Å of Silicon nitride are deposit. These are lithographically patterned with the channel. Then, the substrate is etched by the wet etching process in KOH solution to define the microchannel. A BOE etch of one minute is perform to remove the 500Å of oxide. Then the substrate is grown with another 6500Å thermal oxide. This thermal oxide is only deposit in the channel surface to form the hydrophilic layer. The Silicon nitride is then removed so the silicon substrate is the exposed. Poly silicon is deposit, 6000Å for the formation of the electrodes. Next, Positive photoresist is spin coated on the wafer and cured at in a high-temperature oven. The photoresist is lithographically patterned and etched as hydrophobic regions by the O2 plasma process to serve as the bottom part of the hydrophobic lateral breather. The top cover with the roughness gradient structure is fabricated by using a dry film negative photoresist. A first layer is exposed first and then a second layer with the pattern is mounted.

III. THEORETICAL ANALYSIS

A. Roughness Gradient Design of Hydrophobic Surface

The contact angle has been commonly used to represent surface wettability. Surface wettability is a function of surface roughness. The latest experimental results confirm that wettability can be tuned by surface roughness [25], [26]. The earliest literatures reported that the contact angle of a droplet on a rough surface could be predicted by two main theories relating the surface structure to the apparent contact angle. The first theory was proposed by Wenzel [27], which assumes that the liquid completely wets the solid structure, as illustrated in Fig. 2(a). The second theory was proposed by Cassie and Baxter [28], which assumes that the liquid does not wet the valleys of the structure and forms a composite surface on the rough substrate, as illustrated in Fig. 2(b). Afterwards, Bico et al. [26] fabricated the substrates with specific roughness and compared the measured contact angles with the prediction results. They claimed good agreement and proposed that Wenzel’s formula is valid for the hydrophilic surface and that Cassie and Baxter’s formula is valid for the hydrophobic surface.
The structural design of the surface roughness gradient in our device is illustrated in Figure 3. The surface roughness varies with the pillar patterns on the dry film resist cover. For our roughness gradient design, pillar decreases along the x-direction of the microchannel.

![Decreasing gradient](image)

**Fig. 3. Illustration of the roughness gradient design on the hydrophobic surface of the top dry film resist cover that is made of square pillars.**

The roughness gradient surface of our micropump is hydrophobic, which leads to the formation of a composite surface. Besides, previous report from Shirtcliffe et al. has also shown that the dimension variation of square pillars allows the length of the contact perimeter per unit area to be varied without varying the contact area per unit area [30]. As a result, there is no change on the contact angles.

**B. Electrolysis**

When an electric current is sent through the two noble metal electrodes (such as platinum) in water, electrolysis takes place. The minimum equilibrium potential of hydrogen–oxygen electrolysis $E^\circ$ is 1.23 V. In the electrolysis reaction, the oxygen gas is produced at the anode, and the hydrogen gas is produced at the cathode, i.e.

**anode**: $2H_2O \rightarrow 4H^+ + 4e^- + O_2$

**cathode**: $2H_2O + 2e^- \rightarrow 2OH^- + H_2$

Under the assumption that all generated gases ($O_2$ and $H_2$) evolve in the form of gas bubbles, the total gas volume linearly depends on the input electrical charge [17]. The total gas volume generated by the electrolysis in the process of bubble nucleation could be estimated according to Faraday's law of electrolysis and the ideal gas law [31].

$$N = \frac{It}{zF}$$

$$PV = NRT$$

where $N$ is the moles of produced gas, $I$ is the applied current, $z$ is the number of excess electrons, $F$ is Faraday's constant (9.649x10^4 C/mol), $t$ is the period of electrolysis, $T$ is temperature, $P$ is the ambient pressure, $V$ is the volume of the bubble, and $R$ is the gas constant (8.314 J K^-1/mol). Under the assumption of constant temperature and atmospheric pressure, the volume of produced gases is proportional to the supplied electric current [32].

**D. Applied Voltage**

The pumping flow rate relies on many factors, such as the applied voltage, the duty cycle, and the driving frequency. These imply that the actuation pulses play a dominant role for the maximum pumping flow rate. Besides, the expansion period and the venting period of the bubble in one pumping cycle are also critical parameters to regulate the square-wave actuation pulses. The operation frequency $f$ and the duty ratio $d$ are defined as

$$f = \frac{1}{t_{\text{expand}} + t_{\text{vent}}}$$

$$d = \frac{t_{\text{expand}}}{t_{\text{expand}} + t_{\text{vent}}}$$

where $t_{\text{expand}}$ and $t_{\text{vent}}$ are the expansion period and the venting period of the electrolytic bubble in one pumping cycle. The expansion period $t_{\text{expand}}$ is dominated by the period of the applied voltage in one pumping cycle. The venting period $t_{\text{vent}}$ is dominated by the bubble volume and the pressure magnitudes on both meniscuses.

**IV. EXPERIMENTAL SETUP**

To characterize the performance of the micropump with different depths were fabricated. The test was done by using low-power oscillators to create the square waveforms required by each poly-electro to generate the bubble.

**V. EXPERIMENTAL RESULTS AND DISCUSSION**
VI. CONCLUSION

A electrolysis-bubble-actuated micropump with the design of the roughness gradient on the microchannel hydrophobic surface and the lateral breather was successfully fabricated. Further work to optimize the adhesion between the dry film resist and the silicon surface is needed. The features of micropumps on compact size, simple microfabrication, low-power consumption, and room temperature operation make it promising to be integrated with other multiple components to form microfluidic systems.

REFERENCES

Development of a Linear-Source, Atmospheric-Pressure RF Glow Discharge Plasma

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Abstract—A linear-source, atmospheric-pressure RF glow discharge plasma has been designed, fabricated, and analyzed. The RIT atmospheric-pressure plasma (RITAPP) consists of two parallel-plate electrodes separated by a 1.2 mm gap. Helium is flown through the gap, exiting the slit and impinging a substrate. 13.56 MHz RF power is applied to one electrode, resulting in a non-thermal plasma with a gas temperature (T_g) between 50 and 150 °C. Optical emission spectroscopy was used to determine spectral radiation in the UV-Vis region of helium and helium/oxygen plasmas. Singlet and triplet helium emissions as well as numerous O, H, and OH peaks are observed. Surface treatment of bare 2” (100) p-type silicon wafers was performed by short exposure to a He/O_2 plasma exposure increased surface energy, creating a hydrophilic surface. 20-minute exposures of bare and RCA-cleaned silicon substrates to a He/O_2 plasma were analyzed using ellipsometry and mercury probe C-V measurements. Optical thickness was determined to be 3.4 nm while C-V measurements revealed that both the plasma-grown oxide and the chemical oxides exhibited enhanced dielectric properties following treatment. Work is ongoing to expand upon oxidation experiments as well as I-V diagnostics of the plasma. In addition, investigation of low-temperature carbon nanotube growth is underway.

Index Terms—Atmospheric, Glow Discharge, Oxide, Plasma, Radio Frequency, Surface Treatment

I. INTRODUCTION

Low-pressure plasmas have long been utilized in materials processing. These plasmas offer high concentrations of chemically reactive species at low gas temperatures while maintaining a uniform gradient of reactive species over a large area. This makes them ideal for etching, deposition, and surface treatment [1]. Unfortunately, low-pressure plasmas are limited by their requirement for expensive vacuum systems which require continued maintenance, and limit the size and throughput of treated substrates. High-pressure (e.g. atmospheric) plasmas pose an impressive advantage over their low-pressure counterparts, as the need for vacuum systems is eliminated. This opens the door for the exploration of new processing environments, including open air.

Atmospheric-pressure, high-temperature plasmas (e.g. torches and plasma spray [2]) are common in applications where substrates are not thermally sensitive or the exposure time is kept very short. Low-temperature, atmospheric-pressure plasmas, such as the corona discharge and the dielectric barrier discharge (DBD), have been utilized in recent decades for surface treatment applications. A major limitation of these systems is that they are not uniform throughout the discharge volume (non-homogeneous) and have relatively low electron densities when averaged over time and space. This can make them useful for surface treatment, but etching and thin film deposition capabilities are limited.

Recently, homogeneous atmospheric-pressure plasmas (APP), also called atmospheric-pressure glow discharges (APGD), operating at low temperature have been realized [3-6]. These offer many of the benefits of low-pressure plasmas without the drawbacks of a vacuum environment or the uniformity issues of other atmospheric-pressure plasmas. Compared to low-pressure plasma deposition tools, APP offers reduced up front costs through elimination of vacuum, reduced cost of ownership through reduced maintenance, improved throughput, and can potentially be applied to any size substrate. In this paper RIT’s proof of concept atmospheric-pressure plasma deposition tool is described. Development of the RIT atmospheric-pressure plasma (RITAPP) system is discussed. Plasma diagnostics are then examined using optical and thermal spectroscopic analysis. Finally, preliminary application studies for surface treatment and silicon dioxide growth explored.

II. THEORY

A. What is plasma?

Plasmas are ionized gases, often referred to as the fourth state of matter, which constitute an estimated 99% of the matter in the universe. They contain positive and negative ions, neutral species, and electrons. Plasma is generally electrically neutral; however, it contains free charge carriers and is electrically conductive. Plasmas are often referred to as partially- or fully-ionized, which refers to the degree of ionization in the gas. The RITAPP is a weakly ionized plasma, where only a small fraction of the atoms are ionized [3, 5].

B. Creation of Plasma

Plasma is created when energy is provided to a gas. This energy can be either thermal or supplied by an electric field or
emergence of powerful electromagnetic radiation. Under an applied electric field, electrons in the gas are accelerated. The electrons collide with neutral species, modifying the electronic structure of the neutral species, creating excited species, ions and more electrons [3, 7, 8].

C. Thermal versus Non-Thermal Plasmas

Atmospheric-pressure plasmas, such as welders and torches, are thermal in nature. These plasmas are at or near equilibrium where the electrons, ions, and neutrals have the same temperature. As pressure is reduced, the number of elastic collisions between heavy particles decrease, creating a disparity between the temperatures of the electrons and the gas and giving rise to a non-thermal plasma, as seen in Figure 1. For a low-temperature plasma at high pressure, methods must be implemented to force a non-equilibrium condition between the electron and gas temperatures [1, 3, 7, 8].

D. Non-Thermal Atmospheric Plasmas

1) Dielectric Barrier Discharge

The DBD makes use of a dielectric barrier on one or more of the electrodes, preventing charges created in the gas from reaching the electrodes. Due to the dielectric barrier, no DC current can be passed and an AC bias must be applied. When the applied AC bias exceeds a breakdown voltage, narrow discharge filaments conduct electrons through the gap and towards the more positive electrode. As charge buildup occurs on the dielectric barrier, the voltage drop across the filament is reduced until it can no longer be sustained and the discharge is extinguished. These microdischarges last on the nanosecond time scale while heavy particle reactions require a duration orders of magnitude higher to reach equilibrium.

While the DBD has been used for over a century in various applications, the filamentary nature of the plasma limits its application. The non-homogeneous nature in both space and time creates non-uniformities on a scale too large for materials processing requiring uniform treatment such as in microelectronics [3, 9].

2) RF Glow Discharge

Glow discharge plasmas at atmospheric pressure make use of an RF bias applied to one of two capacitively coupled, bare-metal electrodes spaced a few millimeters apart, as shown in Figure 2. The RF bias results in an electric field capable of accelerating electrons on each half cycle and giving them enough kinetic energy to, upon collision with a heavy particle, cause ionization. The resultant ions under the same bias are unable to gain enough kinetic energy to equilibrate gas.

Unlike the DBD, the discharge maintained under an applied bias is homogeneous and free of filaments or arcs. The gas temperature remains on the order of 300-500 K while the electron temperature can exceed 10000 K [3, 6, 9, 10].

III. DEVELOPMENT OF THE RIT ATMOSPHERIC-PRESSURE PLASMA

A. Plasma Head

A linear-source plasma is ideal for potential scaling to large areas. Such a design requires a wide, thin gap contained between a powered and a grounded electrode across which an electric potential is applied. In this gap, an easily ionized gas is flown. When the electric field is applied, the gas between the electrodes ionizes, forming a capacitively coupled plasma. Helium (Airgas, 99.999% purity) was chosen for initial study due to its low breakdown voltage and electrical stability under moderate power [11]. A sufficiently small gap is required in order to allow a high enough electric field for breakdown of the working gas. Prior work has shown that a gap on the order of 1 – 2 mm is appropriate [10]. All work herein uses a 1.2 mm gap.

The RITAPP plasma head, Figure 3, was designed so that the gap may be changed by using different spacers. Powered electrode area was limited to keep power requirements to a minimum while still realizing a useful plasma size. The electrode material has negligible effect on the plasma properties due to the weak ion bombardment in the atmospheric pressure [12]. Aluminum was chosen as the electrode material for its high conductivity and ease of machining. A two-inch wide slit was chosen for complete coverage of a two-inch silicon wafer, resulting in a powered electrode 50.8 mm wide by 50.8 mm long.

In addition to plasma size considerations, a uniform treatment of a substrate requires that gas flow exiting the plasma head be homogeneous across the width of the slit. For this, computational fluid dynamics (CFD) simulations were performed using COSMOSFloWorks, as seen in Figure 4,
Fig. 3. 3-D Schematic of the RITAPP plasma head. (a) Looking into bottom of plasma head. (b) and (c) Isometric views. Electrodes are made of aluminum and encapsulated on all sides not facing gap by Teflon for electrical insulation. A gas diffusion box is placed at entrance of slit to provide area for mixing of gases.

assuming a 50 sLm flow of helium and oxygen, to confirm uniform velocity exiting the slit. High flows, correlating to velocities between 5 and 12 m/s, ensure that no outside air enters the plasma slit. The large “diffusion” gas box prior to entry of gas into the slit allows for mixing of gases and room to add diffusion barriers for gas mixing if needed.

The final plasma head design can be seen in Figure 5. Two aluminum plates were used to compress the insulators, spacers, and electrodes together. These plates were then attached to the diffuser box to seal the plasma head. The powered electrode was attached to a Type N connector while the grounded electrode was connected to the plasma head body.

B. Impedance Matching Network

Inherent in any RF design is the complex impedance of the plasma head. RF power sources are designed to see a 50 Ω load. Any deviation from this impedance results in reflected power, putting stress on the source and requiring additional power input to power the plasma. Working with a senior engineer at MKS Instruments (Rochester, NY), an impedance matching network (matchwork) was designed (Figure 6). The matchwork is a modified ENI MWH-5 automated tunable matchwork consisting of a pi-network with two variable capacitors, an inductor, and a load capacitor. The variable capacitors are attached to motors that are varied by a control unit. The control unit determines optimal capacitance through an electrical phase and magnitude “phase/mag” detector at the input of the matchwork. In order to determine the appropriate capacitors and inductors, the impedance of the plasma was calculated. Based on previous work [6], in addition to capacitance calculations, a plasma equivalent circuit was created. MathCAD was then used to calculate the impedance of the entire circuit (matchwork and plasma equivalent circuit) and the variable capacitor range that would give the largest tunable range. The resultant allowable load impedance range can be seen on the Smith chart in Figure 7. Upon completion of the modified MWH-5, the unit was tested at low power using an Agilent E5071C network analyzer and determined to be capable of providing an accurate tune with an impedance of 50.203 – j0.074 Ω and a standing wave ratio of 1.09.
C. System Setup

The RITAPP plasma head is placed in an exhaust chamber for removal of effluent gases, as seen in Figure 8. A Comdel DX-2000 RF source (courtesy: Applied Materials) is attached to the matchwork and then connected to the plasma head within the chamber. A hotplate underneath the plasma head is used for heating of substrates during processing.

IV. RITAPP DIAGNOSTICS

A. First Plasma

Plasma was achieved by flowing helium between 15 and 50 sLm between the electrodes spaced 1.2 mm apart. 13.56 MHz RF power between 20 and 130 W was applied to the powered electrode, corresponding to a maximum power density of 5 W/cm². Power over 130 W resulted in arcing between the electrodes. Pictures of the discharge can be seen in Figure 9, taken with a Nikon D50 and a 15-55mm lens.

Additional investigation of He/O₂ (Airgas 99.999% purity) plasmas determined that a glow discharge can be sustained with oxygen making up less than 3 %vol of the gas. Emission intensity decreased as a result of the addition of oxygen, however power density reached 8 W/cm² (200 W applied) was reached before arcing. A comparison of a He and a He/O₂ plasma can be seen in Figure 10. Images were taken using a Nikon camera with a baffle and thimble lens.

B. Plasma Emission Intensity Profile

A photograph across the discharge, as seen in Figure 11, was taken for analysis of emission intensity profile. Variable spatial emission between the electrodes is observed – a result of capacitive sheaths adjacent to the electrodes. These space charge sheaths are a result of a net imbalance between ion and electron densities near the electrodes. This imbalance creates a local electric field which accelerates ions towards the electrodes and electrons into the bulk [13].

As a result of the low electron density, few excitation collisions occur within the sheaths, resulting in low emission. High electric field on the sheath edge results in higher emission at the edge of the bulk than in the center.
C. Optical Emission Spectroscopy

In order to determine excited species, optical emission spectroscopy (OES) (Ocean Optics HR4000, HC-1 grating) was utilized. Comparison of the emission of a 70 W helium and a 70 W helium/oxygen plasma can be seen in Figure 12. Emission intensity is substantially decreased in the oxygen plasma – likely a result of the higher breakdown voltage required. For the same power, lower current can be achieved. Numerous hydrogen, oxygen, and hydroxyl peaks are observed in the pure helium plasma, indicating water contamination. Efforts to determine the source of contamination are ongoing.

Time resolved OES of a helium plasma, Figure 13, revealed an increase in emission intensity with respect to time. Effluent gas temperature was measured with a Type T thermocouple placed 3 mm downstream of the electrodes over the same time and was seen to increase, reaching a maximum of 372 K. It is believed that heating of the electrodes leads to heating of the gas and emission intensity.

D. Determination of Non-Equilibrium Condition

The simplest model for a plasma is based on the Maxwell-Boltzmann distribution. This model, however, assumes an equilibrium plasma and is not suited for non-thermal plasmas. Nevertheless, application of the Boltzmann model to excitation temperature of atomic species in the discharge (1) can be used to determine whether the plasma is in an equilibrium state. The excitation temperature of an excited atom is

\[ T = \frac{E_i - E_j}{k} \frac{1}{\ln \left( \frac{I_{jk} \nu_{jk} A_{jk} g_k}{I_{jh} \nu_{jh} A_{jh} g_j} \right)} \]   (1)

where \( T \) is excitation temperature, \( E \) is the upper level energy of an excited atom, \( I \) is the relative emission intensity, \( \nu \) is the emission frequency, \( A \) is the transition probability, and \( g \) is the statistical weight. The latter three variables are obtained from the NIST atomic spectra database [14].

If the plasma is at or near equilibrium, the excitation temperatures should match. A distribution of excitation temperatures (notably from the gas temperature) supplies evidence of a non-thermal plasma. Using the emission profile of the helium plasma in Figure 13, excitation temperatures were found with respect to time, as seen in Figure 14. The distribution of excitation energies, all of which are above the effluent gas temperature, confirm that the RITAPP a non-thermal atmospheric-pressure plasma.

V. ATMOSPHERIC PRESSURE PLASMA APPLICATIONS

A. Surface Treatment

Capability of surface treatment using the RITAPP was performed on hydrophobic (100)-Si wafers. The substrates were RCA cleaned with a final 50:1 HF dip to remove the chemical oxide and exposed to a He/O2 plasma. Contact angle measurement revealed increased surface energy, making the wafer hydrophilic, as seen in Figure 15.
Fig. 15. Surface modification of a clean, bare silicon wafer. Following an RCA clean and 50:1 HF dip, the contact angle between water and the substrate was 81.3°. After a short exposure to a helium/oxygen plasma, wetting resulted in no measurable contact angle.

The plasma creates ionized molecular oxygen and radical atomic oxygen, which react with material and result in higher surface energy. Such a process is ideal for applications such as improved anodic bonding, textile treatment, and thin film adhesion promotion.

B. Silicon Dioxide Growth/Modification

Using a helium/oxygen plasma, silicon dioxide growth on bare (100)-Si substrates and (100)-Si substrates with a chemical oxide from an RCA clean was attempted. Analysis was performed using an ellipsometer (J.A. Woollam VASE) and a mercury probe capacitance-voltage tool (MDC). Optical and electrical thickness measurements do not agree, but both indicate oxide growth. C-V curves for samples not exposed to the plasma indicate poor dielectric properties. Dielectric properties of the samples exposed to the plasma were enhanced. Bare samples exhibit high hysteresis and interface traps, while those from the chemical oxide samples appear to be greatly enhanced.

VI. CONCLUSION

A non-thermal, atmospheric-pressure glow discharge plasma has been successfully designed, fabricated, and tested. Helium is flown between two bare metal electrodes separated by a 1.2 mm gap at velocities between 5 and 12 m/s. RF power between 20 and 200 W is applied to one electrode, generating a glow discharge plasma. Gas temperature of the plasma effluent was between 50 and 150 °C. Surface modification has been demonstrated on bare silicon exposed to a He/O₂ plasma. Exposure increased surface energy of the film. Oxides with optical thicknesses of 30 nm have been grown. Exposure of chemical oxides to the plasma enhanced their dielectric properties. The RITAPP system shows promise as a tool for low-temperature, atmospheric-pressure materials processing. Work is ongoing to characterize the plasma, investigate carbon nanotube growth at low temperature, and explore potential new applications.

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Fig. 16. Surface modification of a clean, bare silicon wafer. Following an RCA clean and 50:1 HF dip, the contact angle between water and the substrate was 81.3°. After a short exposure to a helium/oxygen plasma, wetting resulted in no measurable contact angle.

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Optical Ring Resonator and Other Photonic Devices (May 2008)

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**Abstract**—This project aimed to design, simulate, fabricate and test optical ring resonators and other waveguide devices. The computational technique used to simulate our devices was beam propagation method (BPM) in RSOFXT CAD software. These devices were developed to be fabricated on 4" silicon-on-insulator (SOI) wafers and fabricated in the Rochester Institute of Technology fabrication laboratory.

**Index Terms**—Optics, Photonics, Ring Resonator, Waveguides

The understanding and application of photonics has continued to mature as a necessary component of the information revolution. Communication with light has displayed some remarkable advantages over their electronic counterparts, such as speed, bandwidth, and power consumption [1]. Without a doubt, photonics will continue to play a large role as our society increases their demand for greater amounts of information traveling across longer distances. In the past 15 years photonic fabrication has benefited tremendously from the microelectronics infrastructure. The ability to produce waveguides on a micron scale has introduced new avenues in switching, filtering, and the modulation of light. It’s important to continue developing our understanding of photonic fabrication for the advancement of the microelectronic revolution.

In this project, 1μm optical ring resonators will be designed, simulated, and then fabricated on 4" silicon-on-insulator (SOI) wafers. The 4" substrates were chosen over the 6" substrates for budget reasons.

Photons has continued to grow and mature since the times of James C. Maxwell first successfully described the propagation of electromagnetic waves with his equations in 1878. Through the invention of the laser in 1960, the use of optics as a method of information transfer became more achievable. Communicating with light waves displayed some remarkable advantages over electronics. One such element in photonics is the enormous bandwidths possible. To comprehend the rational of ultra high bandwidths (5THz or 10^{12}Hz), one must understand the nature of electromagnetic waves in comparison to an electric current. In respect to single signal speeds, light waves propagate at speeds greater than electrons. However, the greatest advantage characteristic to light is the consequences of the lack of charge in photons. Since these particles carry no charge, their interference with each other carries very specific requirements in frequency and location. Therefore, a multitude of waves can coexist in the same medium while exhibiting negligible interference as they pass through each other. Such parallel processing allows optical systems to achieve the superior bandwidths.

I. DESIGN OF THE PHOTONIC DEVICES

A. Waveguides

One of the first hurdles in the goal of optical communication was finding a suitable medium of propagation. A wave traveling in through the atmosphere is far too susceptible to multiple variables such as temperature, scattering, and line-of-sight transmission. The natural attempt at a remedy to this issue was to enclose the wave in a protective pipe with an internal reflective coating. After years of examining methods to ameliorate the huge problems of attenuation, dispersion, and scattering of the waves, the solution resolved into the form of waveguides such as modern fiber optics.

Traditionally, 1550nm wavelength has been used for its low dispersion over long transmission distances, and negligible absorption through glass.

Building upon the enormous microelectronic fabricating infrastructure, nano-photonics platforms are using Silicon-on-Insulator (SOI) platforms for their devices. While silicon is conveniently transparent to the traditional 1550nm light, photonics on silicon also benefit from the mature etching methods of silicon which prove critical when developing low loss devices. Furthermore, the use of silicon solves the cladding question since it has a natural oxide (SiO₂) which grows from its surface. This glass layer retains an index of refraction of n=1.46 which is advantageously discrepant from the silicon waveguide (n=3.45). This contrast assists the total internal refraction necessary for information transfer.

These waveguides will house electromagnetic radiation (light) which propagates with an electric and magnetic component. Maxwell’s equations below in Fig1 describe the relationship between the electric field (E), Magnetic field (H), charge density (ρ), and current density (J).
B. Ring Resonator

In photonics, a ring resonator is simply a waveguide which exist in a closed loop. Such a loop is usually coupled with another straight waveguide where power can be transferred via the evanescent wave which exists outside the donor waveguide boundary. This phenomenon can be physically explained through Maxwell’s equations stating that the electric and magnetic fields must be continuous at boundaries. Light with the tuned wavelength will travel in the ring and will eventually build up due to constructive interference. Because this coupling is highly sensitive to the wavelength of the light, ring resonators can be used as filters; an essential function in the goal of photonic logic. [5] An all-pass filter with a single resonating ring is shown below.

![Figure 2: Optical ring resonator comprised of a straight waveguide and a ring adjacent to it.](image)

As depicted in Fig 3, the waveguides are silicon slabs resting on a silicon surface. Surrounding these waveguides is SiO2 which will act as an optical cladding. Total internal reflection needed for photon propagation is enabled by the difference in the refractive indexes between the silicon waveguide and the oxide. The dimensions shown in Fig. 1 are the optimum designed values of the coupling region. A primary restriction in this design was the lithography equipment which allowed a minimum dependable feature size of 1µm. The key dimensions of the optical devices where the waveguide slab height, minimum bending radius, and racetrack length in the ring resonators.

![Figure 3: Cross section of the coupling region of two straight waveguides traveling into and out of the page plane.](image)

C. Simulations

Simulations were done using RSOFT CAD software using the Beam Propagation Method as a calculations model. Fig. 4 displays the simulated transfer of a signal through coupling of two straight waveguides over 185um. The dimensions of these waveguides match the cross section shown in Fig. 3. Fig 4 is just one example of the several iterations tested while varying etch depth, slab height, and bending radius.

![Figure 4: Simulation using BPM showing the transfer of power from one waveguide to an adjacent waveguide.](image)

Fig. 5 below shows a compilation of the data describing the relationship between device sizes and etch depths. The Coupling line represents the length of racetrack needed to achieve a 10% transfer. The Bend line describes the radius of curvature which would result in a loss of 10% of power. The ability to match power loss and coupling is needed to achieve a resonating system.
Figure 5: Simulation information describing the device size needed to attain the 10% coupling gain and 10% loss.

D. Processing

Several challenges arise in the fabrication photonics using the semiconductor technology. One such step, is the development of Silicon-on-Insulator (SOI) wafers which house a layer of Buried Oxide (BUX) thick enough to isolate the waveguides from interacting with the substrate. One method of creating this layer of oxide is Separation by implantation of Oxygen (SIMOX) [7] which uses a high energy implant of oxygen ions combined with high temperature anneals. This process yields great uniformity but requires very high implant voltages to produce sufficient thickness. Another method of producing BOX is called Smart Cuttm [6] where a wafer is prepared with an oxide layer grown on the surface. Another sacrificial wafer is then implanted with hydrogen atoms. These wafers are then sandwiched together to bond. Then after heat treatment, the implanted wafer will cleave at the hydrogen implanted projected range creating a single SOI wafer. All of these methods are not viable at RIT and wafers will need to be ordered for further steps.

A thin layer of oxide can be used as the hard mask for defining the silicon structures. This material is beneficial because it is not a contaminate in most tools and its resistance to the reactive ion etch (RIE) used in the process. Photoreist has a much lower melting point and shows poor selectivity compared to silicon in a reactive ion etcher. The layer of oxide will be deposited using the P5000 TEOS chamber.

Lithography was done using the GCA 4” stepper. Even though the Cannon has a smaller resolution, the GCA was used because the wafers were not large enough to be accepted in the Cannon tool. Shown in Fig 6 are the photonic devices written to the aluminum mask.

As shown in Fig 6, several rings were placed on the same die with various racetrack lengths. This was done in hopes of achieving critical coupling at the 1550nm wavelength.

Fig 7 shows the substrate reflectivity simulated in PorLith simulation tool as a function of TEOS thickness. In order to avoid the standing wave effect, a minimal amount of reflectivity is desired from the substrate. A thickness of 375um of TEOS was used.

The original mask made at RIT contained stitching errors. This was caused by a slight misalignment in the writing tool used to pattern the mask. As shown in Fig. 8, such stitching errors which occurred several times across our 7mm long devices would cause a substantial loss in the wave signal. This issue was avoided by using an outside mask provider.
E. Results

Proof of concept was achieved in fabricating the waveguide devices in the RIT SMFL. Shown below in Fig 9 are the fabricated ring resonators.

In Fig 10, one can see a single waveguide with some oxide left over on top. The waveguide and silicon layer is on top of the lowest layer buried oxide.

F. Future Work

The reproduction of this project would include active devices using a PIN diode to enable switching through use of the electro-optical effect. The electric field placed across the ring only, would slightly skew its effective refractive index. This in turn would shift the filtered wavelength.

Furthermore, a more selective anisotropic etch is needed for the silicon etch. The DryTek Quad used for this project had some isotropic characteristics and left some rough sidewalls.

G. Conclusion

Photonic devices were successfully fabricated using microelectronic fabrication technology. There were several processes steps which needed to be customized such as using photoresist as a thermal transferring agent in the P5000 REI. Future projects should consider using 6" substrate since technology favors their too. set.

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Keywords: Si-on-insulator (SOI); Smart-cut™; Wafer bonding; Surface blistering

Unbalanced Mach-Zehnder Electro-Optic Modulator and Waveguide Components

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Abstract—Design and fabrication of waveguide structures on silicon-on-insulator (SOI) such as couplers and S-bends as components of Mach-Zehnder modulator (MZI) are presented here. These basic devices are important for processing light signals using silicon. Beam propagation method (BPM) was used to obtain dimensions of discussed structures for future manufacturing. During the design of the interferometer it was found that parameters of only either of branches could be altered to induce desired interference effect at the output of MZI. Hence, the device was dubbed unbalanced MZI. Since coupling separation was a factor that determines coupling length, it was chosen to be 1um in order to decrease overall length of the final structure and ensure that photolithography could be contained within the field size of the available steppers. The width for all waveguide components was chosen to be 1um to accommodate photolithographic constraints as well. It was discovered that MEBES mask-writing tool produces field stitching. Features written across the boundary of two fields gaps produced notches that were expected to severely decrease the transmission of the 1.55um light through the waveguides. New mask was sought and some devices were still built with the old mask to determine the viability of the proposed process.

Index Terms—Mach-Zehnder, waveguide, photonics, coupler, y-junction, interferometer

I. INTRODUCTION

Mach-Zehnder modulator employs interference produced between phase coherent light waves that have traveled over different path lengths. A beam splitter is used to divide the light into two equal beams that are set to travel through parallel waveguides. The injection of carriers (electrons or holes) into these silicon guides can cause band shrinkage and band filling that change the refractive index of the material thus effective optical path length.

Optical path length is defined to be the product of the geometric length of the path light follows through the system, and the index of refraction of the medium through which it propagates.

Ideally, the path lengths and waveguide characteristics are identical, so that without the carrier injection the split beams recombine in the output waveguide to produce the lowest-order mode similar to the input. If an electric field is applied to produce a phase change of \( \pi \) radians between the two arms the modulator can be switched off from a transmitting to non-transmitting state.

Free-carrier plasma dispersion effect is used to convert the phase-shift to an amplitude modulation. This phenomenon is employed to alter the properties of silicon of one of the branches of MZI to produce a phase-shift at the output side of the device.

Confinement of light in a material is dependent on condition called total internal reflection. Total internal reflection is an optical phenomenon that occurs when a ray of light strikes a medium boundary at an angle larger than the critical angle with respect to the normal to the surface. If the refractive index is lower on the other side of the boundary no light can pass through, so effectively all of the light is reflected.

However, an electromagnetic wave cannot propagate at any angle less than the critical angle but rather only discrete allowed angles. These discrete solutions are called modes of propagation.

To ensure that the majority of optical power is delivered and the resulting field distribution is most confined the structures are condition to operate in the single mode region. At multi-mode operation the optical power is split equally between the modes.

Mach-Zehnder interferometers can be used to fulfill two functions: modulation and switching. Optical modulators are devices that are able to control the amount of light passing through them. Optical switches are devices that change spatial position of light (on/off).

Device description: The source beam with wavelength of 1.55\( \mu m \) is split into two waves using a coupler and guided along varying path lengths. The split beams are then recombined to produce phase change. The electro-optic effect states that the change in index of refraction in a material is produced by the application of the electric field. Refractive index of silicon without the electric field is 3.48, however it varies as function of bias under varying electric field. [2]

Silicon optical modulators are relatively low speed compared to those made from III-V semiconductor compounds or other electro-optic materials such as lithium niobate. The fastest silicon waveguide modulator was demonstrated to have frequency of only 20MHz although devices of gigahertz range frequencies were theoretically described. [4]
II. PROJECT OBJECTIVE

A. Goal
The main objective of this undertaking was to manufacture and characterize silicon waveguides, beam splitters, and Mach-Zehnder interferometers at RIT semiconductor and Microsystems fabrication laboratory (SMFL).

B. Components
1) Waveguides
An optical waveguide is a fundamental element that interconnects the various devices of an optical integrated circuit. Optical waves travel in these structures similar to electric current in a metal wire. Light however propagates in modes inside the material, which once again means that the optical energy of the traveling waves is spatially distributed in one or more dimensions. Ridge waveguide has been chosen for classification due to its ability to support single mode propagation over larger range of dimensions eliminating fabrication constrains that are present in more planar models.

Figure 1.0 shows the cross-sectional view of a silicon waveguide, the shaded area below the structure is the buried oxide layer located in bulk material. To minimize losses from sidewall scattering the waveguide is most desired to be of dimensions that guarantee the confinement of fundamental mode. [3] These dimensions include a specific height and width of the structure that can be determined using theoretical calculations and software simulation.

2) Splitters
Splitter is a device that allows branching of optical power. There is a number of alternatives that can be used to accomplish this: couplers and multi-mode interference waveguides (MMI). 1x2 power splitter can be used to split the optical power entering the Mach-Zehnder and to merge it after the phase shift is introduced.

3) Carrier drivers
Forward biasing the p-i-n diode across the intrinsic region of the waveguide accomplishes carrier injection or depletion of electrons and holes into the silicon and changes its refractive index. Using an MOS capacitor produces the same results, however instead of direct injection of carriers accumulation conditions are applied and the majority carriers modify the silicon properties.

C. Mach-Zehnder Device
Modulation of the refractive index of silicon can be achieved via the free carrier plasma dispersion effect. The phase change can be determined using the following relationship:

$$\Delta \phi = \frac{2\pi}{\lambda} \Delta n_{eff} L,$$

where \(L\) is the active length of the phase shifter, \(\lambda\) is the wavelength of light in free space, and \(\Delta n_{eff}\) is the effective index change in the waveguide, that is the difference of the refractive index of the waveguide with and without electric bias. The output light intensity is related to the phase difference and can be expressed as:

$$I_{out} \propto I_{in} \cos^2(\Delta \phi/2),$$

where \(I_{in}\) is the intensity of light at the input of Mach-Zehnder.

![Fig. 1. 3D profile of an optical ridge waveguide](image)

III. PLAN OF WORK
The following section details accomplished and future project's steps.

A. Simulations
1) Waveguide dimensions
Using BeamProp software a number of ridge waveguides was simulated, this assisted at studying the dependence between the structures sizes and propagation of the modes of light through the device and its components. Parameters suitable for such investigation were waveguide height and width. It was determined that for single mode propagation necessary waveguide ridge height was found to be 0.7 um.

2) Splitter dimensions
The dimensions of the coupler also a splitter were found using alike method. These parameters included length,
width of the coupler and the distance between the output waveguides that is a property dependent on the location where the multi-mode operation occurs inside the coupler. The minimal coupling length for equal optical power splitting was found to be dependent of the slab height of the silicon in which this waveguide structure was fabricated. The smallest coupling length allowed was found to be around 200 um.

Figure 3.0 shows one of the numerous simulation runs that allowed determining coupler size for future mask design.

3) S-bends
S-bend is a curved waveguide that allows spatial shifting of light in respect to plane within which light propagates.

![Fig. 3. Coupler beam propagation method simulation](image)

Optimal S-bend radius was determined for slab thickness range of 1.2 um to 1.4 um of silicon layer on top of silicon dioxide film. It was determined that 300 um bending radius was minimal for manufacturing of nearly ideal Mach-Zehnder interferometer (MZI) using this thickness range. Figure 4.0 shows power loss inside one of simulated silicon S-bends.

4) Diode
In order to obtain electric properties for the carrier driver p-, n-well implant doses and junction could be simulated using Deckbuild Athena. Using this information active length of this device could be found and targeted at manufacturing. Also placement of the diode wells in relation to the waveguide would be extracted from this study.

B. Preliminary steps
Since this was a planned five level lithography process, alignment marks test features, and overlay verniers were needed. These are generally standard features available in the CAD library for GCA type steppers and can selected when the layout for the masks is proposed.

C. Fabrication
First level photolithographic was designed to define physical structures on the wafers. These included definitions of waveguides, beam splitters, s-bends and Mach-Zehnder modulators of varying dimension. GCA resolution of 1um and field size of 2cm by 2cm were considered when these structures were mapped in the L-Edit layout environment. Aligned second and third level lithography were to be devised to define p- and n-wells, fourth level to provide contact cuts and fifth exposure to pattern metal. Only first level lithography was performed and future processing was required to be carried out to produce electrically active devices. Some passive testing was to be done after the first level lithography to observe whether the waveguides and couplers were transmitting optical power. This stage would allow determination whether the entire process flow could be carried out or the processed wafers would have needed rework.

D. Characterization
IV characteristics and threshold voltage of the diode were to be measured at SMFL device testing area. The light intensities measurements of the light would be completed in the photonics laboratory. Devices would be considered functioning if the power at the output of the interferometer would be minimal when the voltage was applied to the driving diode. Plots of the diode bias to the normalized output intensity would be generated to make conclusion about device performance.

IV. RESOURCES, EQUIPMENT AND MATERIALS
SOI 4 inch wafers were used as fabrication substrates. GCA g-line (436nm) stepper was used for photolithographic steps. For exposure wafers would be coated with Shipley 1813 and developed in CD-25 aqueous developer. PE5000 tool was used for depositing and etching LTO layer to produce mask for silicon etching, which was later patterned using Drytech Quad plasma etcher. Boron and phosphorous would be the dopant species used to define wells using Varian 350D implanter. Implant energies and dose would be obtained using the software simulations.
V. PRELIMINARY INVESTIGATION

A. Y-Junction Vs. MMI

When deciding which of the coupler is more suitable fabrication tolerance was considered. Since MMI is a relatively large structure, edge roughness does not influence it performance significantly. Also, relative dimensions of an MMI coupler is smaller compare to that of a y-splitter because it device has a short coupling region comparing to single-mode waveguide couplers. Performance of y-junctions is also heavily dependent on the capabilities of the lithographic equipment unlike MMI’s. However, MMI splitters are difficult to design, hence the coupler was chosen as the power splitters for this design.

B. Diode Vs. Capacitor

Capacitor MZI requires extra process steps. p-i-n diode MZI is slower than capacitor driven device. [1] P-i-n diodes enable the use of plasma dispersion if it is forward bias and use of thermo-optic effect if it is reverse bias. [5]

Injection of excess of free carriers leads to recombination, and heating in the waveguide core. Small changes in temperature can produce a large thermo-optic shift in the refractive index, leading to a device dominated by thermal rather than electrical effects. [6]

In order to minimize the volume over which recombination occurs, and prevent carriers from diffusing, isolation trenches are usually etched to the buried oxide layer. This method ensures increase in injection efficiency.

VI. RESULTS

Manufactured devices included interferometers consisting of 300 um and 500 um S-bends, coupling regions of lengths of 200um, 250um, 300um, 350um, and 400um as well as waveguide structures. Photolithography yielded desired critical dimension on SOI substrates. Figure 5.0 shows successfully manufactured devices.

It was determined that to produce a nearly ideal oxide mask for silicon etching using SMFL tools and to accommodate this design, the thermal conductivity of the substrate had to be increased. Using photoresist to improve conductivity showed positive results. However, etching in Drytech Quad did not produce ideal silicon structures. Undercutting was observed and the coupler separation was increased. Further optimization of the etching of silicon was required to be carried out however the time and budget constraints did not allow for further processing. Figure 6.0 shows undercutting of the waveguide ridge during dry etching of silicon. If this stage was successful and passive characterization of the devices was completed, it was expected from coupler to split the optical power into beams of equal intensity, and also merge such beams into one even if the input and output of this device were reversed. It was expected for light wave to experience attenuation, as it would travel through the waveguide structures. Attenuation in return would reduce the total transmitted power. Some losses that are encountered in literature associated with waveguide components are presented below.

A. Scattering Loss

1) Volume Scattering

Caused by imperfections such as contaminants and crystalline defects. This type of scattering is negligible when the volume imperfections are small comparing to wavelength.

2) Surface Scattering

Surface roughness causes optical loss when propagating waves interact with the waveguide. Surface roughness arises due to non-ideality of wet and dry etch of the material.

B. Absorption Loss

Absorption loss is negligibly small compared to scattering loss. Photons with energies greater than the bandgap energy of silicon are absorbed in the waveguide structure to raise electrons from the valence to conduction band.
C. Radiation Loss

Radiation loss occurs when optical energy is lost from the waveguide if photons emitted into the media surrounding the waveguide instead of being guided within the structure. Attenuation that happens due to this usually occurs in curved and angled structures like splitters and s-bends.

VII. Conclusion

Fundamental characteristics of Mach-Zehnder device and other optical structures were described. The Mach-Zehnder interferometer (MZI) is the basis of a wide variety of optical devices e.g. modulators, sensors and optical switches. Beam Prop simulations were used to make decisions about the selecting appropriate feature size for mask design. Using this information unbalanced Mach-Zehnder interferometers and other waveguide components were fabricated. Thinning of waveguides was discovered upon inspection using scanning electron microscopy. High transmission loss for features with such defect was expected. An alternative etching technique was suggested to produce devices with minimal undercutting. Silicon etch resistant masks were successfully manufactured. However, more dry etching process experiments were suggested to adapt this design of 1um wide silicon waveguide components and MZI to SMFL.

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