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Michael Aquilino  
*Rochester Institute of Technology*

Reinaldo Vega  
*Rochester Institute of Technology*

Mohammed Rabman  
*Rochester Institute of Technology*

Bryant Mann  
*Rochester Institute of Technology*

Michael Latham  
*Rochester Institute of Technology*

*See next page for additional authors*

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ATTENDEE LIST

AIR PRODUCTS
Dr. Raymond Vrtis
Air Products
Electronics Division
7201 Hamilton Blvd
Mail Stop R4203
Allentown, PA 18195
610-481-2160
vrtirn@apci.com

ANALOG DEVICES
David Kneedler
Analog Devices
21 Osborn Street
Cambridge, MA 02139
617-761-7118
david.kneedler@analog.com

BREWER SCIENCE
Joseph Raposo
Brewer Science
78 Faunce Corner Road
Suite 540
North Dartmouth, MA 02747
508-992-3590
jraposo@brewerscience.com

CANON USA
Ray Morgan
Canon USA
3300 North First Street
San Jose, CA 95134
408-468-2265
morgan@cusa.canon.com

DESIGN INTEGRATION TECHNOLOGIES
Amil Schmitt-Weaver
ASML
1081 Exchange Street
Boise, ID 83716
208-342-8757
amil.schmitt.weaver@asml.com

EASTMAN KODAK CO.
Dan Fullerton
Eastman Kodak Co.
1999 Lake Avenue
Rochester, NY 14650-2023
585-722-5155
daniel.fullerton@kodak.com

John Spoonhower
Eastman Kodak Co.
1999 Lake Avenue
Rochester, NY 14650-2107
585-588-6173
john.spoonhower@kodak.com

FAIRCHILD SEMICONDUCTOR

Thomas Grebs
Fairchild Semiconductor Corp.
125 Crestwood Road
Mountaintop, PA 18707
570-474-6761 x4505
tom.grebs@fairchildsemi.com

Todd Kyser
Fairchild Semiconductor Corp.
333 Western Avenue
Mail Stop 01-51
South Portland, ME 04106
207-775-8072
tkyser@fairchildsemi.com

INTEL CORPORATION

Kirk Smith
Intel Corporation
5000 W. Chandler Blvd
Mail Stop CH3-84
Chandler, AZ 85226
kirk.d.smith@intel.com

Margaret Sova
Intel Corporation
5000 W. Chandler Blvd
Mail Stop CH10-87
Chandler, AZ 85226-3699
480-554-2865
margaret.a.sova@intel.com

INTEL CORPORATION

Mike Wegener
Intel Corporation
5000 W. Chandler Blvd
Chandler, AZ 85226
971-215-8212, 971-214-0781
mike.r.wegener@intel.com

IBM

Louis Anastos
IBM
2070 Route 52
Mail Stop EMI
Hopewell Junction, NY 12533
845-892-3808
anastos@us.ibm.com

Richard Behun
IBM
863M
1000 River Road
Essex Junction, VT 05452-4299
802-769-9285
behun@us.ibm.com

MICRON TECHNOLOGY

Pary Baluswamy
Micron Technology
MS 718
8000 S. Federal Way
Boise, ID 83716
208-368-1290
pbaluswamy@micron.com

MOTOROLA

David Laurer
Motorola
611 Jamison Road
Elma, NY 14059
716-687-6209
david.laurer@motorola.com
**MOTOROLA**

John Mullane  
Motorola  
611 Jamison Road  
Elma, NY 14059  
716-687-6305  
john.mullane@motorola.com

**ROCHESTER PHOTONICS**

Eric Prince  
Rochester Photonics  
330 Clay Road  
Rochester, NY 14623  
585-272-2857

**ROHM & HAAS ELECTRONIC MATERIALS**

Stewart Robertson  
Rohm & Haas Electronic Materials  
455 Forest Street  
Marlboro, MA 01752

**VIRGINIA COMMONWEALTH UNIVERSITY**

Barton Cregger  
VCU  
School of Engineering  
601 West Main Street  
P.O. Box 843068  
Richmond, VA 23284-3068  
804-827-2278  
bbcregger@vcu.edu

**XEROX CORPORATION**

Josef Jedlicka  
Xerox Corporation  
800 Phillips Road  
MS 128-52E  
Webster, NY 14580  
585-422-3411  
j jedlicka@crt.xerox.com

**SYNOPSIS**

Pamela McDaniel  
Synopsys, Inc.  
700 E. Middlefield Road  
Mountain View, CA 94043  
650-584-1922  
pamelam@synopsis.com

**TEXAS INSTRUMENTS**

Jason Neidrich  
Texas Instruments  
6550 Chase Oaks Blvd  
MS 8479  
Plano, TX 75023  
214-567-0886  
jn@ti.com
Editorial

These proceedings contain papers presented at the 22nd Annual Microelectronic Engineering Conference held at the Rochester Institute of Technology (RIT) on May 10 through 11, 2004 by senior undergraduate students of Microelectronic Engineering of RIT. The students graduating with BS degree in Microelectronic Engineering are required to take a two-course sequence of capstone design courses, 0305-680 and 0305-690 entitled Seminar/Research I and II in their fifth year. The first course consists of submission of a research proposal, related to the field of semiconductor devices and processing, by each student. Following the approval of the proposal, the students carry out their projects through the ten-week spring quarter. Toward the end of the spring quarter, the students are required to present their work at the Microelectronic Engineering Conference held at RIT annually in the month of May and publish in this Journal of Microelectronic Research.

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All correspondence should be directed to
The Department of Microelectronic Engineering
Kate Gleason College of Engineering
Rochester Institute of Technology
Rochester, NY 14623
585-475-6065
www.microe.rit.edu

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Advancing RIT to Submicron Technology: Design and Fabrication of 0.5μm N-channel MOS Transistors

Michael Aquilino, Student Member, IEEE

Abstract—The design and fabrication of N-channel MOS transistors with effective gate lengths of 0.5μm or smaller have been completed at the Semiconductor and Microsystems Fabrication Laboratory at the Rochester Institute of Technology. An NMOS device with \( L_{\text{eff}} = 0.25 \mu m \) results in a \( V_{dd} = 105\mu A/\mu m \). The drive current for this device with supply voltage of 3.5V is \( 108\mu A/\mu m \). The sub-threshold slope is \( 100mV/\text{decade} \) and a DIBL parameter of \( 29mV/\text{V} \) is reported. An NMOS device with \( L_{\text{eff}} = 0.6\mu m \) results in an \( L_{\text{eff}} = 0.4\mu m \). The drive current for this device with supply voltage of 3.5V is \( 140\mu A/\mu m \). The sub-threshold slope is \( 103mV/\text{decade} \) and a DIBL parameter of \( 110mV/\text{V} \) is reported. These are RIT’s first sub-0.5micron MOS transistors.

Index Terms—CMOS, NMOS, Process Development, Silvaco, Athena, Atlas, Terada-Muta

I. INTRODUCTION

The goal of this project is to design and fabricate n-channel MOS transistors with gate lengths down to 0.5 μm. To date, the smallest transistor fabricated in the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT has an effective channel length, \( L_{\text{eff}} = 0.75 \mu m \). The motivation for fabricating 0.5 μm transistors is to allow RIT to continue the microelectronics industry trend of scaling towards smaller, faster and cost effective devices. The integration of a new manufacturing process flow has been implemented. The device technology employed includes: n+ poly gates, LOCOS isolation, aluminum metallization, shallow ion implanted n+ sources/drifts, blanket p-type well, p+ channel stop and is designed to operate at a supply voltage of 3.5V. In addition, this project has provided hands-on experience in transistor level design and layout, mask design and fabrication, process development and integration, and electrical testing.

This work is part of capstone design project for a B.S. degree in Microelectronic Engineering at the Rochester Institute of Technology (RIT), Rochester, NY. The results of the project were first presented as part of the 22nd Annual Microelectronic Engineering Conference, May 2004 at RIT.

M. Aquilino is with the Microelectronic Engineering Department, RIT, (e-mail mva6237@rit.edu )

Design and layout of the test chip has been done using Mentor Graphics IC Station. The test chip includes transistors scaled down to 0.5μm as well as test structures, capacitors, and alignment verniers. Four lithography levels: Active, Poly, Contact Cut, and Metal are exposed on the Canon FPA 2000i1, a 365 nm i-line exposure tool. The mask set is fabricated using a MEBESIII electron beam mask writer. Control wafers along with the device wafers are processed for in-line process verification and characterization.

Theoretical calculations have been made to determine process parameters such as doping profiles, junction depths, material thicknesses, and threshold voltages. A process flow is developed to achieve the required device parameters. Simulation of the process is carried out using Silvaco Athena to modify theoretical values and obtain more accurate process parameters. Electrical simulations are in progress using Silvaco Atlas for electrical performance analysis. At the completion of fabrication, the devices will be electrically tested for on and off-state performance. Parameter extraction will then be done to create a SPICE model for these devices that can be used in more complex circuit designs.

II. CHIP DESIGN

A new test chip was designed that can be used for either NMOS or PMOS processes. There are a total of 122 transistors on the design with various Length/Width ratios. Three unique sets of transistors were designed that include fully-scaled NMOS based on MOSIS 2.0 μm design rules, and two flavors of non-scaled devices. The fully scaled devices are designed with mask defined gate lengths of 0.5μm to 10μm where the gate length is two times the minimum feature size, \( \lambda \). Mask defined gate lengths range from 0.35μm to 100μm and widths of 10μm to 20μm for non-scaled devices.

The results of the device discussed in this paper are based on a non-scaled design with contact cut dimensions of 5μmx5μm and 12μm spacing between contact and poly edge. Other design rules have been relaxed in terms of metal and poly overlap. A second set of non-scaled devices feature 2μmx2μm contact cuts and a 4μm spacing between contact and poly edge. The fully scaled devices cannot be tested due to isotropic wet etching of the Aluminum metal.
Also included on the chip are capacitors with areas that range from 40k \( \mu \text{m}^2 \) to 250k \( \mu \text{m}^2 \). These can be used for Capacitance-Voltage analysis to determine Accumulation, Depletion, and Inversion capacitance, oxide charge effects, and threshold voltage.

Various other test structures such as Van-der-Pauw structures for sheet resistance measurements of n+, poly, and metal, and Cross-Bridge Kelvin Resistors, for metal contact resistance to n+ and contact resistance to poly are included. There are also contact cut test structures with various contact cut dimensions ranging from 0.5\( \mu \text{m} \times 0.5\mu \text{m} \) to 5\( \mu \text{m} \times 5\mu \text{m} \). A simple test for conduction between a contact pad and a reference pad will yield if a conductive current path is made and whether it is ohmic or non-ohmic.

Transistors with field oxide as a gate oxide are included to determine field threshold voltage to be sure it is high enough to stop on parasitic conduction channels from source to drain or device to device.

Included in Figure 1 is the layout of the test chip designed in Mentor Graphics IC Station. It uses 5 design layers: active, poly, metal, contact to active, contact to poly. The two contact layers are combined to form one contact mask and individual masks for active, poly, and metal were fabricated using a MEBESIII electron beam mask writer.

### A. Process Simulation

The process used to fabricate the NMOS transistors has been simulated in Silvaco Athena to verify the correct process parameters such as implant dose and energy, thermal steps, and film deposition, result in the desired doping profiles and device structure. Figure 2 is the final simulated device structure.

The final simulated doping profiles achieved are shown in Figure 3. They include shallow S/D junctions with a depth of approximately 0.15\( \mu \text{m} \). The junctions must be scaled deeper to give the gate more control over turning the device on and off. The p-well is doped moderately high to reduce the depletion region extending from the S/D into the well. This will enable deep submicron transistors to perform as long channel devices by reducing channel length modulation and preventing lateral punch-through.[1]
B. Electrical Simulation

The final device structure was imported into Silvaco Atlas and simulated for on and off-state performance. For the 0.5µm physical gate length device, an on-state saturation drive current with \( V_G = V_D = 3.5\text{ V} \) is simulated to be 300µA/µm. The threshold voltage is targeted to be 0.85V. In the off-state, a sub-threshold slope of 112mV/decade and sub-threshold swing of 9.5 decades is obtained. Figure 4 is a simulated ID-VD plot with the transistor biased in the linear and saturation mode. Figure 5 is a ID-VG plot with ID on a linear scale for threshold voltage extraction and on a log scale for sub-threshold characteristic extraction. \( I_{OFF} \) is simulated to be 10fA/µm with \( V_G = 0\text{ V} \).

IV. Fabrication

All fabrication for these devices was done in the Semiconductor and Microsystems Fabrication Laboratory at RIT. The entire process takes approximately 4-5 weeks to complete with an average of 5-6 hours of processing time per day. A total of 32 process steps are required to bring the devices from bare silicon to test. A cross-section is shown in Figure 6 with the final device topology.

A. P-Well Formation

- Grow 500Å Pad Oxide
- Ion Implant \( 2\times10^{13}\text{ cm}^{-2} \) B11 @ 40 KeV
- Drive in for 60 min @ 1025°C in N\(_2\)
- \( N_A = 2\times10^{17}\text{ cm}^{-3} \)
- \( X_j = 2 \mu m \)

A pad oxide is used as a screening layer for the implant so that channeling of ions along certain crystal planes in the silicon lattice does not occur. Also, the pad oxide will be used as a stress relief layer between the subsequent Si\(_3\)N\(_4\) deposition. The doping of the p-well is chosen to be moderately highly doped so that depletion regions extending from the source/drain do not touch when the device is biased; leading to a short channel effect known as punch-through.

B. Creation of Active Area

- Deposit 1500Å of Silicon Nitride
- Level I Lithography: Active Area Define
- Channel Stop Implant: \( 1\times10^{13}\text{ cm}^{-2} \) B11 @ 40 KeV
- Grow 3500Å Field Oxide

The silicon nitride is patterned so that the active area of the device is masked. A channel stop implant is done through the pad oxide to place additional boron in the field region so that parasitic conduction channels do not form between source and drain or from transistor to transistor.
A moderately thin field oxide is grown to reduce the birds beak effect inherent in a LOCOS process and to reduce the amount of boron outdiffusion into the field oxide.

C. Gate Formation
- Strip Nitride and Etch Pad Oxide
- Grow 250A Kooi Oxide & Etch
- Grow 150A Gate Oxide
- Deposit 3500A Polysilicon
- Dope Poly with Solid Source Phosphorous
- Level 2 Lithography: Poly Gate Define
- Poly Etch in SF$_6$ Plasma

A thin oxynitride layer is formed after LOCOS field growth so a 30 second Buffered HF etch is performed. Next the silicon nitride is stripped off in a wet hot phosphoric acid bath at 175°C. The pad oxide is etched and a thin Kooi oxide is grown in dry O$_2$ with a 99 min soak at 900°C. This is done to remove any nitride stringers that are formed along the edges of the active region. This effect is called "white ribbon" and is created by a reaction between NH$_3$ and Silicon at the LOCOS edge. Next a 150A gate oxide is grown with a 45 min soak at 900°C in dry O$_2$. A chlorine pregrowth clean is done to neutralize sodium ion contamination in the tube and in the quartz boat. The poly is deposited via LPCVD and doped with a solid source dopant. A 10-minute soak at 1000°C in N$_2$ is done to drive-in the n+ poly dopant. Level 2 lithography is performed to pattern the gate and is etched in an SF$_6$ gas in a LAM490 plasma etcher.

D. Source/Drain Formation
- Ion Implant $5\times10^{14}$cm$^{-2}$ P31 @ 15 KeV
- ND = $7\times10^{19}$ cm$^{-3}$
- $X_J = 0.15$ µm

Shallow source/drain implants are done with a P31 ion to introduce phosphorous into the source/drain regions. The field oxide is being used as a hard mask for the implant into the field region. A $5\times14$cm$^{-2}$ dose at 15 KeV is performed with the use of a Varian Ion-Implanter. The resulting junction depth after anneal is targeted to be 0.15µm with a surface concentration of $7\times10^{19}$cm$^{-2}$.

E. Back End Processing
- Deposit 3000A PECVD TEOS
- Anneal for 30min at 900°C in N$_2$
- Level 3 Lithography: Contact Cut
- RIE Oxide in SF$_6$/CHF$_3$ mixture
- Sputter Deposit 5000A Aluminum
- Level 4 Lithography: Metal
- Wet Etch Al wiring

An inter-level dielectric is deposited to a thickness of 3000A using an Applied Materials PECVD tool with TEOS chemistry to form an insulating oxide. The source/drain anneal step is done after the oxide deposition to densify the TEOS so that its insulating properties are enhanced. Level 3 lithography patterns the contact cuts, which are then etched in an SF$_6$/CHF$_3$ mixture in a Drytek Quad RIE plasma etcher. The resist is stripped, the wafers cleaned, and 5000A Aluminum is deposited via a CVC601 sputtering tool. Level 4 lithography patterns the metal features and a wet etch in a 50°C Phosphoric/Nitric/Acetic acid is performed. Finally, the wafers are sintered in a 5 slpm H$_2$/N$_2$ forming gas mixture for 10 minutes at 420°C.

V. RESULTS

The results of the first lot of devices did not yield characteristic transistor IV. The ID-VD plot of a 10µm NMOS device is shown in Figure 7.

![Figure 7: L/W=10µm/20µm Failed NMOS Device](image)

It was determined that the contact cuts to the source/drain were etched through the n+ silicon and into the p-well due to aggressive RIE plasma etch. This causes a parasitic conductive path from source to drain through the well, bypassing the inversion channel as the primary current conductor. It was also found that the channel stop implant was too low in dose and energy. To fix the problem, 2 wafers that were left behind in the process after gate oxide growth were processed. Additional boron was implanted through the field oxide with a $1.5\times13$cm$^{-2}$ dose at 75 KeV. The etch time in the RIE tool was cut nearly in half to ensure no silicon would be etched.

The results of the second lot were successful in producing transistor characteristic curves, which exhibited long-channel behavior. Figure 7 is a cross-sectional SEM micrograph of the final device fabricated.
An ID-VD plot for a device with $L_{\text{mask}}/W_{\text{mask}} = 0.6\mu m/20\mu m$ is shown in Figure 8. Through the Terada-Muta Method of $L_{\text{eff}}$ extraction, an $L_{\text{eff}}$ of 0.4$\mu m$ is reported. This $L_{\text{eff}}$ takes into account process biases such as isotropic polysilicon etch and source/drain lateral diffusion under the poly gate which makes the channel length smaller. This is RIT’s first sub-0.5$\mu m$ MOS transistor.

Figure 8: NMOS ID-VD for $L_{\text{eff}} = 0.4\mu m$

There is some non-ohmic behavior, which has been attributed to a residual interfacial oxide layer that exists between the Aluminum and silicon. A more aggressive sinter recipe is needed to correct this problem. It is also noticed that there is high series resistance, which is causing the ID-VD curve to slope over and not deliver the entire 3.5V that is applied to the drain to actually appear across the transistor. There is some slight upward slope in the saturation region of operation, which is due to channel length modulation, another short channel effect common to submicron transistors. Preliminary mobility parameter extraction yields values of around 200$cm^2/V$-sec, which is very low. This can be attributed to velocity saturation effects since a high voltage is being placed across a small gate length. Low doped drains can be implemented in the future to add additional resistance to the transistor, thereby decreasing the effective voltage across the S/D terminals.

An ID-VG plot is shown in Figure 9 on a linear current scale to extract the threshold voltage. The threshold voltage for this device is 0.75V. It is also noticed that the current slopes over dramatically as VG is increased due to high series resistance.

Figure 9: NMOS ID-VG for $L_{\text{eff}} = 0.4\mu m$

A plot of ID-VG on a Log ID scale is shown in Figure 10. The sub-threshold slope is 103$mV$/decade at 0.1V drain bias and increases to 110$mV$/decade at 3.5V drain bias. $L_{\text{eff}}$ is approximately 10$fA/\mu m$ at 0.1V drain bias, which matches exactly with simulation. There is about 7.5 decades difference between $I_{on}$ and $I_{off}$.

Figure 10: Sub-threshold ID-VG for $L_{\text{eff}} = 0.4\mu m$

Figures 11, 12, and 13 are off-state performance plots as the devices are scaled submicron. $V_t$ roll-off is a common phenomenon as devices are scaled down in gate length. It can be seen in Figure 11 that the $V_t$ doesn’t roll-off to any significant amount until around 0.4$\mu m$. At 0.75V, this is only a 12% decrease compared to the 0.5$\mu m$ device with a $V_t$ of 0.85V.

Figure 11: $V_t$ Rolloff vs $L_{\text{eff}}$ for NMOS Transistors

The sub-threshold slope is plotted vs $L_{\text{eff}}$ in Figure 12, for drain biases of 0.1V and 3.5V. It is seen that the two curves do not diverge until around 0.4 $\mu m$. 
Figure 12: Sub-threshold Slope vs. \( L_{\text{eff}} \)

Figure 13 is a plot of DIBL vs. \( L_{\text{eff}} \) to characterize the short channel effect of Drain Induced Barrier Lowering. This effect causes the gate to lose control over turning the device off and increased off-state current results even when sub-threshold slope does not increase dramatically. The DIBL parameter is calculated in units of mV/V and corresponds to a change in gate voltage per change in drain voltage at a fixed current level[1]. A DIBL value of around 25 mV/V is good. It is seen that the DIBL does not start to dramatically increase until the device is scaled to an \( L_{\text{eff}} \) of 0.4\( \mu \)m.

A summary of the performance between an \( L_{\text{eff}} \) of 0.4\( \mu \)m and 0.5\( \mu \)m is shown in Table 1. A summary of additional electrical parameters is shown in Table II. It is noted that the sheet resistance of the n\(^+\) region is very high, 360 \( \Omega/\mu\text{m} \), this is due to very shallow junctions.

**Table I**

<table>
<thead>
<tr>
<th>( L_{\text{eff}} ) (( \mu )m)</th>
<th>( V_{\text{t}} ) (V)</th>
<th>( \text{ID} @ \text{VG} = \text{VD} = 3.5\text{V} ) (( \mu \text{A}\mu\text{m} ))</th>
<th>( S_{\text{SS}} ) (mV/dec)</th>
<th>DIBL (mV/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>0.75</td>
<td>140</td>
<td>103</td>
<td>110</td>
</tr>
<tr>
<td>0.5</td>
<td>0.85</td>
<td>108</td>
<td>100</td>
<td>29</td>
</tr>
</tbody>
</table>

A mask drawn gate length of 0.7\( \mu \)m yielded a device with an effective channel length of 0.5\( \mu \)m. The threshold voltage for that device is 0.85V, which came out exactly as simulated. The drive current in the saturation mode of operation with \( V_{G} = V_{D} = 3.5\text{V} \) is 108 \( \mu \text{A}/\mu\text{m} \). The sub-threshold slope is 100 mV/decade at \( V_{D} \) of 0.1V and 3.5V. The DIBL parameter is 29 mV/V, which is very good. It can be seen that the 0.5\( \mu \)m \( L_{\text{eff}} \) device has well controlled short channel effects. The smallest device tested on the die was a mask drawn gate length of 0.6\( \mu \)m, which yielded an effective channel length of 0.4\( \mu \)m. The threshold voltage for this device begins to roll-off to about 0.75V with a sub-threshold slope of 103mV/decade. The DIBL parameter quickly increases to 110mV/V, which is much higher compared to the 0.5\( \mu \)m device, but depending on off-state current requirements, this may be acceptable. As an advantage, the 0.4\( \mu \)m device features a 33% increase in drive current at \( V_{G} = V_{D} = 3.5\text{V} \) at a value of 140 \( \mu \text{A}/\mu\text{m} \).

**VI. CONCLUSION**

The goal of this project was to design and fabricate NMOS transistors with gate lengths of 0.5\( \mu \)m or smaller. It has been demonstrated that 0.5\( \mu \)m and sub-0.5\( \mu \)m N-channel MOS transistors are capable of being fabricated completely in-house at the SMFL at RIT using standard CMOS processing techniques. Future work will include integrating low doped drains using sidewall spacer technology and silicided source/drains and gates. This will allow for a second, deeper, implant to be done, which will lower the sheet resistance in the active area.

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Michael Aquilino, originally from Liverpool, NY, received a B.S. degree, Summa Cum Laude, in Microelectronic Engineering from the Rochester Institute of Technology in 2004. He obtained co-op work experience at Atmel Corporation in Columbia, MD and Integrated Nano-Technologies in Henrietta, NY. He is currently pursuing an M.S. degree in Microelectronic Engineering at RIT.
Metal Source/Drain Schottky Field Effect Transistors – a Proof of Concept

Reinaldo A. Vega, Student Member, IEEE

Abstract—Field effect transistors, in which the sources and drains are made of metal (aluminum), as opposed to silicon, have been conceived, designed, fabricated, and tested. For the n-body device, maximum Jon was found to be 74.69 μA/μm after a “burn-in” process was performed. For 1V to 10V drain bias, extracted Vt values varied between 2.3V and 6.5V, gm between 0.002 and 341 μS, sub-Vt slope between 111 and 706mV/dec, and Ion/Ioff between 1.11 and 3.99 decades. The Schottky barrier height was found to be 0.503eV. Additionally, full CMOS operation using one metal for both NFET and PFET operation is proposed and discussed. The long-term goal of the presented device is 3D circuit integration, for which a potential implementation scheme is presented.

Index Terms—3D circuitry, metal source/drain, SBMOSFET, SBTT, Schottky source/drain.

I. INTRODUCTION

Over the past few decades, the drastic increase in consumer demand for smaller, faster, and cheaper computing devices has played a major role in driving the semiconductor industry to its current state of technology, as well as increasing the range of applications for microprocessors. Quite naturally, however, new technologies pose new challenges. One such challenge is overcoming the degrading ability of aggressively-scaled transistors to act as desirable switches in digital circuitry, which has been running in parallel with overcoming the degrading ability to manufacture said transistors using conventional methods. Some solutions propose to scale devices in three dimensions rather than the current two (known as 3D circuitry for its suggestion of building multiple semiconductor levels on a single chip), while other solutions propose to better the performance characteristics of the devices themselves by utilizing unique processing techniques. It is the primary purpose of the Metal Source/Drain Schottky Field Effect Transistor (MSD SFET) to attempt to provide the potential for both such solutions with one [relatively] simple approach.

The MSD SFET was initially conceived as a means to circumvent potential thermal processing issues upon implementing 3D circuitry in microelectronics. However, further investigation shows that the MSD SFET may prove a potential candidate for future device scaling in traditional 2D CMOS.

The MSD SFET itself has sources and drains which are made of metal. With the right type of metal and the right type of semiconductor (i.e., n-type or p-type silicon of a particular doping level), a Schottky barrier is formed at the metal-semiconductor interface (a comprehensive analysis of metal-semiconductor junctions can be found in [1]). A gate is placed perpendicular to the source-body and drain-body interfaces, and modulates the barrier dimensions by accumulating or depleting majority carriers at the interface. In doing so, the interface becomes either more Schottky-like or more ohmic-like, thus resulting in a gate-modulated current flow.

Similar work has, coincidentally, been performed over the years using sources and drains made of metal silicides [2]-[9]. Metal silicides, however, are formed through diffusion of metal through silicon and some subsequent reaction to induce alloying. Since the MSD SFET uses pure metal rather than metal silicides, this silicidation step is not necessary, and it may even be conceivable to use the same process level for both the NFET and PFET sources and drains as well as the first level of interconnects, thus decreasing manufacturing costs substantially.

Some potential advantages that the MSD SFET has over conventional MOSFET's are: 1.) the source-body and drain-body junctions are ideally abrupt (e.g., no dopant concentration gradient exists), and so the device should be less susceptible to short channel effects such as DIBL and Vt rolloff; 2.) since the MSD SFET is a majority carrier device, it should, in theory, experience zero floating body effect when manufactured on SOI substrates; 3.) since the MSD SFET switches through majority carrier accumulation (as opposed to moderate-to-high inversion), it is presumed that a lower voltage is needed to run a MSD SFET than an equivalently-sized conventional MOSFET.

II. THEORY

A. SBMOSFETs and SBTTs

Any given Schottky diode can be made to act in an ohmic manner by either using a semiconductor of the opposite doping (e.g., p-type vs. n-type), or by using a heavier-doped...
semiconductor. In the first case, the barrier height will decrease in value, and so the dominant current mechanism will be thermionic emission of carriers over the barrier. This is the principle of operation behind conventional SBMOSFETs (Schottky Barrier MOSFETs), where typically an n-type silicon body is used to make a Schottky barrier with Pt-Si, with a barrier height on the order of 0.85 eV \[1\]. Inverting the body region to p-type decreases the barrier height to about 0.25 eV \[1\]. In the second case (using a heavier-doped semiconductor), the effect is that the band bending in the semiconductor at the metal-semiconductor interface increases, eventually to the point at which carriers have a high probability of tunneling through the sufficiently narrowed barrier. Therefore, in this case the dominant current mechanism is tunneling current. The effect of higher dopant concentrations can also be realized by accumulating or depleting carriers from the metal-semiconductor interface (with a gate bias) for a semiconductor of a given dopant level. Such is the principle of operation behind a different form of SBMOSFET, known as a SBTT (Schottky Barrier Tunneling Transistor).

Since conventional SBMOSFET operation relies on thermionic emission for the on state of the transistor, it is desirable for the source/body and drain/body barrier heights to be as low as possible under inversion to minimize contact resistance. This contact resistance can be expressed as \[1\]:

\[
R_c = \frac{k}{qA^T} \exp \left( \frac{q\phi_B}{kT} \right)
\]

where \(k\) is Boltzman’s constant, \(\phi_B\) is the barrier height, \(T\) is the temperature, \(q\) is the charge of an electron, and \(A\) is the effective Richardson constant. Neglecting the temperature dependence of \(R_c\), barrier height becomes the only variable which can be changed to affect the contact resistance in a conventional SBMOSFET.

For the SBTT, the on state takes place during high majority carrier concentrations, and so contact resistance can be expressed as \[1\]:

\[
R_c = \exp \left[ 2\sqrt{\frac{\varepsilon_i m^*}{\hbar}} \left( \frac{\phi_B}{\sqrt{N}} \right) \right]
\]

where \(\hbar\) is Planck’s constant, \(m^*\) is the effective carrier mass, and \(N\) is the majority carrier concentration. While the same exponential dependence on barrier height is present, the contact resistance is effectively modulated by the gate bias which accumulates or depletes carriers at the source/body and drain/body junctions. Therefore, the effect of larger barrier heights can be countered by stronger accumulation (at least until quantum carrier confinement becomes significant). This allows the SBTT to use large barrier height metal-semiconductor junctions to allow for greater thermal operating stability without a significant loss in on state current.

Considering that both conventional SBMOSFETs and SBTTs start from the same device, and that the only difference between the two is the polarity of the gate and drain biases, it would not be unreasonable to suggest that a transistor with Schottky sources and drains would exhibit both conventional SBMOSFET-like and SBTT-like characteristics with the appropriate biases at each terminal (more on this later).

B. MSD SFETs

The MSD SFET is a form of SBTT, in that switching takes place through accumulation (and so tunneling current dominates the on state current). For the particular design discussed, it is only the NFET which acts as a SBTT, as the goal is to implement CMOS circuitry by using one metal instead of two separate metals for two separate Schottky barriers for n-Si and p-Si. Since this design uses an n-Si body for the NFET, the PFET uses a p-Si body, and so a Schottky barrier formed with the source/body and drain/body junctions in the NFET is either schottky but with a lower barrier height or simply ohmic for the PFET. With zero gate bias, then, the PFET is in the on state and must be switched off through depletion or light inversion.

To utilize such a PFET in CMOS circuitry, however, the device would need two gates, by which one gate (the bottom gate) would have a constant bias which depletes the silicon in contact with the metal source and drain (the off state). The other gate (the top gate), when biased, would counteract the effect of the bottom gate, thus making the source/body and drain/body junctions ohmic again. Such a setup would require a high dopant concentration in the body region for acceptable current drive. A possible implementation using a single gate MSD PFET would use a low-doped p-Si body region, which has very low current drive in the off state. A negative gate bias would accumulate carriers toward the silicon/gate dielectric interface, thus turning the transistor “on.” Since the dual gate PFET allows for greater Vt control, it should exhibit better performance characteristics (namely subthreshold slopes).

C. MSD SFET Theory of Operation

In a conventional MOSFET, pinchoff occurs when the difference between drain bias and gate bias is small, such that the channel region near the drain is no longer inverted. This results in the saturation region in the \(I_d\) vs. \(V_d\) characteristic. Understanding the mechanisms behind saturation in the MSD SFET is somewhat less trivial.

Consider Fig. 1 on the following page. At zero drain bias, and for any gate bias, some sort of band bending takes place at the source-body and drain-body interfaces. For an n-Si body SFET, the drain-body diode is forward biased (and so the “barrier height” is the built-in voltage of the diode) and the source-body diode is reverse biased (the barrier height is that on the metal side of the junction). As a drain bias is applied, the built-in voltage of the drain-body diode decreases by \(V_{sd} - V_{dsat}\), and eventually this diode will turn on much like a standard p-n diode. However, even in the “on” state, the drain current is limited by the source current, and the source-body
diode current is the reverse bias saturation current (for a given source barrier width, there exists a limit as to the number of carriers that can be injected from the source into the body). The energy gradient in the body due to the drain bias, however, will serve to decrease the source barrier width (the degree of this effect is dependent on gate bias, as will be discussed later). The decrease in this width will increase tunneling through the barrier, consequently increasing the maximum amount of carrier injection (this becomes significant beyond the saturation region) from the source. At low drain biases, the maximum source injection current is relatively constant, and not being utilized to full capacity, thus resulting in the linear region of the Ids vs. Vds plot. At Vd(sat), the maximum number of carriers are injected from the source for the specific source barrier width, and within some region afterwards increasing the drain voltage will result in little if any increase in drive current. It is at this point that the transistor is in the saturation region of operation.

At drain voltages well beyond Vd(sat), there is enough of a lateral field throughout the transistor such that the drain has control over the source barrier width (the aforementioned DIST effect from Fig. 1). At this point, the maximum source carrier injection current increases with drain bias, and this injection current is fed to the drain-body diode which, at such high biases, is already in an “on” state. This results in a diode-like I-V behavior at very high drain biases. Increasing the gate bias will decrease the source barrier width, thus increasing the lateral field required to further decrease the barrier width. Additionally, an increase in gate bias will increase the built-in voltage of the drain-body diode, thus increasing the turn-on voltage of that diode. At higher gate biases, then, the drain voltage at which DIST occurs is increased.

D. MSD SFETs on SOI Substrates

If SCI substrates were used to manufacture MSD SFETs, it should be expected that the SFET would experience little if any floating body effect (which correlates to the “history effect”). First considering the NFET, the reverse-biased diode is the source/body diode. Applying a drain bias with zero gate bias should result in little charging of the body region, as the majority carriers (electrons in this case) must first traverse the source/body junction. Since Schottky diodes are majority carrier devices, in the case of the NFET, only electrons may enter the body region and bring it to some potential. Therefore, only if there were an ohmic contact between the drain and the body (or at very high drain biases such that DIST occurs) would the body be at some potential to induce electron flow from the source, and in such a case, the gate of the NFET would be ineffectual in controlling current flow anyway (as it is now controlled almost entirely by the drain), thus rendering the device as non-yielding.

The PFET is more like a gate-modulated resistor – it starts off as having ohmic contacts at the source/body and drain/body interfaces, and the device is switched off when the gate “blocks” current flow between the source and drain. When the PFET is in the off state, the body region in contact with the source/drain regions is either depleted or lightly inverted. In the depleted case, no net carrier concentration exists, and so the body region cannot charge up to some potential. In a lightly inverted case, presumably the source/body and drain/body junctions see a Schottky barrier which is the same as the NFET in its off state, and it has previously been shown that the body region of the NFET should not float on SOI substrates. This lack of a floating body effect is an extremely important effect to note of, as it is considered to be a primary disadvantage regarding circuit design on SOI substrates (due to the resultant dependence of the threshold voltage on the body potential, which is not constant throughout a clock pulse). That the body region of a MSD SFET should not float to a potential allows one to utilize the advantages of SOI technology without the challenge of taming the history effect.

E. 3D Circuit Integration

The notion of 3D circuitry, by which multiple device layers are stacked on top of each other within a single chip, has been around for some time, with efforts performed by various research groups [11]-[18]. These implementations, however, utilize conventional MOSFETs. Likewise, as of yet SBMOSFET and SBTT research has not hinted at applications to 3D circuit integration. Considering the possibility of Schottky CMOS becoming a placeholder on the ITRS roadmap [19], integration of Schottky CMOS into 3D circuitry would seem a natural progression.

The real strength of 3D circuitry is not that individual logic gates can be built using multiple levels (thus consuming less area), but rather that entire logic branches can be built on
multiple levels, and that this can be exploited to minimize transmission delays through interconnects. For example, an ALU unit in a microprocessor can be built with three device levels, thus consuming less area. Or, perhaps, the ALU can be built on one level and the SRAM can be built directly on top on another level. With enough levels, it might also be feasible to realize solid state hard drives which operate much faster than the mechanical units in present day computer systems. The potential for maximizing packing density is quite staggering, as are the implications for System-on-a-Chip (SoC) solutions.

Some approaches to 3D circuit integration involve chip-to-chip bonding. This is effective in that it realizes single-crystalline silicon for each device level, thus maximizing performance. The temperatures required for the bonding techniques are low enough so as not to significantly affect the performance characteristics of the fabricated devices. However, that n separate chips must be manufactured to build an n-level 3D circuit results in the final product costing roughly n-times as much. This clearly raises practicality issues for large volume, low-cost fabrication. For high-end systems where cost is not a concern, however, it may well be the best solution.

Another approach to 3D circuit integration is to deposit silicon films on top of previous device layers. This allows a multi-level “chip” to be fabricated on a single wafer, presumably reducing manufacturing cost. The deposited silicon film is recrystallized to form a polysilicon film of some grain size, on which devices are fabricated. The disadvantage to this process is that, by virtue of the devices being manufactured on polysilicon films as opposed to single-crystalline silicon films, the devices themselves exhibit poorer performance characteristics due to degraded carrier mobility and increased leakage currents. However, if the grain sizes can be made large enough such that one device, or one logic gate, or perhaps an entire logic branch, can be fabricated within a single grain, then the device performance in such large grain polysilicon films is equivalent to that of single crystalline silicon.

One of the more promising methods for recrystallization of deposited silicon films to large grain polysilicon is known as MILC (Metal-Induced Lateral Crystallization) [14], [15]. Normally, recrystallization takes place vertically, and so the grain size is on the order of the film thickness. For aggressively scaled devices, this is not desirable, as thinner silicon films are becoming necessary to maintain or improve performance. The MILC process uses nickel “trenches” between areas of amorphous silicon. At elevated temperatures, the nickel forms a silicide and diffuses through the amorphous silicon, leaving large grain polysilicon in its wake. Further recrystallization takes place at higher temperatures (albeit over less time). Two level 3D circuits built using this method have been shown to exhibit enhanced performance over 2D SOI circuits [14]. However, the primary issue is that recrystallization takes place over very long periods of time (tens of hours), and at temperatures which may affect device performance.

The most significant challenge to 3D circuit integration, however, is thought to be the optimization of vertical interconnect routing [15], rather than the formation of single crystalline or near single crystalline silicon films. The MSD SFET can be useful for 3D circuit integration in that, in the design presented, the device is more comparable to a switch within the interconnects than the current day perception of devices separate from the interconnects. This in itself has potential for increased 2D packing density, but also has increased potential to overcome device contact issues (also for 2D circuits) at very small sizes, as well as interconnect routing issues for 3D circuits. If very thin interfacial layers (oxide, nitride, etc.) are placed between the metal source/drain regions and the body region, such that the interfacial layer is thin enough to be transparent to tunneling but thick enough or of the right material to slow down or prevent reaction between the metal source/drain regions and the silicon body region, or the interfacial region, at elevated temperatures during MILC processes, then the MSD SFET may prove a universally useful device for both 2D circuitry and most approaches to 3D circuit integration.

III. EXPERIMENTAL PROCEDURE

The devices were fabricated on 4-inch 15Ω-cm bulk n-Si wafers with aluminum as the metal of choice. Aluminum was chosen because it is relatively simple to manufacture Schottky diodes using aluminum and lightly doped n-Si. A top-down view and two cross-sections of the MSD SFETs are shown in Figs. 2, 3, and 4, respectively. The manufacturing process requires seven microlithography levels. Level 1 defines the N+ implant which acts as an ohmic contact to an Al/n-Si Schottky diode. Level 2 defines the p-well implant, which results in a p-Si body for the MSD PFETs. Both implants are performed through a 500Å dry pad oxide, and the anneal/drive-in process uses the same pad oxide recipe. The resulting ~1000Å of oxide serves as a field oxide, through which active areas are defined and etched (Level 3). The exposed silicon surface is put through a pre-evaporation clean (1 min. dilute HF, 1 min. DI rinse, N2 blow dry), and then placed in a bell jar evaporator for pure aluminum deposition (wafers under vacuum in 5-10 min.).

Level 4 defines the metal source and drain as one piece. The photoresist is left on the aluminum, and a silicon etch is performed using SF6 and CHF3. The photoresist is then stripped, and a channel define etch is performed which splits apart the source and drain regions (Level 5). The gate dielectric (500Å PECVD TEOS) is then deposited and patterned (Level 6), as is the second layer of aluminum, which acts as the gate electrode (Level 7).
In various stages of the process, different wafers were sintered at 450°C in H2/N2 forming gas for 15 min. MSD SFETs were manufactured on a total of nine wafers, with four processing splits, as defined in Table 1. One wafer from each of the first three splits was run through the entire 7-level process to fabricate both n-body and p-body SFETs (as well as test structures), while the other six wafers saw a 6-level process for the n-body SFETs and test structures. It should be noted that a complete comparison between the process splits was not performed, as the uniqueness of the I-V characteristics placed a greater importance on understanding the true operating theory behind the device.

**TABLE 1**

<table>
<thead>
<tr>
<th>Wafer number</th>
<th>Split definition</th>
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</thead>
<tbody>
<tr>
<td>2.3.4</td>
<td>Post M1 deposit sinter</td>
</tr>
<tr>
<td>5.6.7</td>
<td>Post silicon etch sinter</td>
</tr>
<tr>
<td>8.9.10</td>
<td>Post channel define sinter</td>
</tr>
<tr>
<td>2.6.10</td>
<td>P-well implant for n-body SFETs</td>
</tr>
</tbody>
</table>

**IV. EXPERIMENTAL RESULTS AND DISCUSSION**

Fig. 4 shows the “burn-in” process performed on an n-body SFET. With the gate set at 10V, the drain is swept from 0V to 10V for a number of runs until the resultant curves begin to look similar. This allows for greater consistency when comparing the results of various devices. It has been found that a burn-in process of 14 runs is sufficient, and that leaving the device untested for one day after the burn-in process has no significant effect on the device characteristics.

Fig. 5 shows the complete Ids vs. Vds characteristic of the same device for both SBTT-like (first quadrant, n-channel, electron tunneling current) and conventional SBMOSFET-like (third quadrant, p-channel, hole thermionic emission current) operation, as predicted from the theory section. Electron current: is seen in third quadrant operation at low gate biases, as these low gate biases are not enough to offset the Vt shift from the oxide charge present in the PECVD TEOS used as a gate dielectric (and so the channel is not yet inverted). Considering this Vt shift, the peak current in the third quadrant should be larger for Vg=10V with a gate dielectric with minimal charge density. Likewise, the peak current in the first quadrant should be lower. Nevertheless, the difference in current
between first and third quadrant operation can be explained by both the difference in electron and hole mobilities, as well as the difference in contact resistance between the inversion and accumulation cases, shown by (1) and (2). It should be noted that under very strong inversion, the contact resistance can be expressed using (2), as the dominant current mechanism becomes hole tunneling as opposed to hole thermionic emission. Fig. 6 shows the $I_d$ vs. $V_{gs}$ characteristic for the same device, and Fig. 7 shows the sub-$V_t$ slope and maximum transconductance vs $V_{ds}$.

etch is 3.24μm, corresponding to a peak $J_on$ of 74.69μA/μm. Peak current in the third quadrant is 27μA, or 8.33μA/μm.

Fig. 6: $I_d$ vs. $V_{gs}$ characteristic for 2μm x 5μm n-body SFET (n-channel). $V_{ds}$ was varied from 1V to 10V in 1.5V increments.

Fig. 7: Sub-$V_t$ slope and $g_m_{max}$ vs. $V_{ds}$ for 2μm x 5μm n-body SFET (n-channel). Minimum sub-$V_t$ slope is 111mV/dec., maximum transconductance is 341μS.

As Fig. 6 shows, a very large increase in off-state leakage current occurs with increasing drain bias. This is due to the aforementioned DIST effect, whereby at lower gate biases, a lower drain voltage is necessary to modulate the source barrier width. The decrease in drain current at larger drain biases for gate biases from 0V to about 3V reinforces this idea, as at higher gate biases the source barrier width is smaller (thus requiring a larger drain bias for DIST).

The erratic behavior of the sub-$V_t$ slope in Fig. 7 is simply due to the behavior at $V_{ds}$=4V, apart from which the sub-$V_t$ slope increases rather smoothly from 111mV/dec. at $V_{ds}$=2.5V, tapering off at 706mV/dec. at $V_{ds}$=10V. At low drain biases, there does not exist a large enough voltage to turn on the drain-body diode, and so little or no current is displayed (as shown in the $V_{ds}$=1V case in Fig. 6). This causes the sub-$V_t$ slope to increase. Therefore, for low voltage operation it is critical to fabricate drain-body Schottky diodes with low turn-on voltages or a drain-body junction that is ohmic. The ohmic case would provide for better low voltage current drive and sub-$V_t$ slope; however, it may also lower the drain bias requirements for DIST to take place, thus potentially increasing off-state leakage current.
Vega, R.

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V_{tsat} vs. V_{ds} is shown in Fig. 8, and corresponds with Figs. 6 and 7 in that lower sub-Vt slopes result in larger V_{tsat} values, ranging from 2.3V to 6.5V.

Fig. 8: V_{tsat} vs. V_{ds} characteristic for 2μm x 5μm n-body SFET (n-channel).

Fig. 9 shows I_{on}/I_{off} and I_{off} vs. V_{ds}. It is stressed that V_{ds} is used in these relationships, as opposed to Vdd, where the on state current is the drain current at V_{gs}=10V, and the off state current is the drain current at V_{gs}=0V. In looking at Fig. 6, it becomes clear that using Vdd as a metric would not give much information, since large gate biases are required to achieve an on state with little regard for drain bias.

The Schottky barrier height for this device was extracted from test diodes on the same die, using the current-temperature method [10]. Diode characteristics were measured at 30°C to 80°C in 10°C increments, and the resultant barrier height was calculated as 0.503eV.

An example of DIST is shown in Fig. 10. As expected, an increase in gate bias results in an increase in the drain bias at which DIST occurs. The plot is a standard I_{ds} vs. V_{ds} relationship, but with the drain swept to 20V. At V_{gs}=7V and V_{ds}~18V, it is shown that the gate dielectric broke down. Further current measurements were at the 100mA rail.

Fig. 9: I_{on}/I_{off} and I_{off} vs. V_{ds} for 2μm x 5μm n-body SFET (n-channel). Maximum I_{on}/I_{off} is 3.99 decades. I_{off} increases exponentially, in accordance to the diode-like behavior resulting from DIST.

Fig. 10: I_{ds} vs. V_{ds} for 1μm x 10μm n-body SFET (n-channel). Onset of DIST occurs at about 10V and above, increasing with increased gate bias.

Of particular interest with the n-body, n-channel SFET is the high V_{gs}, high V_{ds} region in Fig. 5. In this region, the drain current decreases with increasing drain bias (this is also seen in Fig. 10). The current theory regarding this "NDR" (Negative Differential Resistance) region is as follows.

In the n-body MSD SFET, the source-body junction is reverse-biased, as previously mentioned. As V_{ds} increases, two events take place. First, the increasing reverse bias on the source-body junction causes the source-side depletion width to grow. Second, the increase in V_{ds} causes a decrease in V_{gd} for a given gate bias, thus causing the drain end of the body region to become less accumulated (and eventually depleted as V_{ds} surpasses V_{gs}). Therefore, with increasing V_{ds}, the body region becomes increasingly depleted, thus increasing the body resistance. Since the NDR region occurs after saturation, which is after the point at which the source has reached its maximum carrier injection capacity for a given gate bias (and before the drain takes control via DIST), an increase in body resistance will decrease the current drive in this region (it is presumed that the increase in source injection capacity in the DIST region far outweighs the increase in body resistance), thus resulting in the observed phenomena.
Fig. 11 and 12 serve to not falsify the aforementioned NDR theory. Fig. 11 shows that the source and drain currents are almost exactly equal, and any difference is due to gate leakage, which is very small, as shown in Fig. 12. Therefore, there are no body current or gate current phenomena which are decreasing the drain current in this NDR region, suggesting that the effect is related to the behavior of the device itself.

Fig. 11: \( I_{ds} \) and \( I_s \) vs. \( V_{ds} \) for 5\( \mu \)m x 10\( \mu \)m n-body SFET (n-channel). Square points are \( I_s \) data, solid lines are \( I_{ds} \) data. Equality of source and drain current indicate zero presence of body current which may subtract from \( I_{ds} \) in the NDR region of operation.

Fig. 12: \( I_{ds} \) and \( I_{gs} \) vs. \( V_{ds} \) for 5\( \mu \)m x 10\( \mu \)m n-body SFET (n-channel). \( I_{gs} \) is very small (tens of \( \mu \)A), therefore, the NDR region is not influenced by gate leakage.

P-body SFET operation is demonstrated in Fig. 13. That there is a measured \( I_{ds} \) at \( V_{ds} = 0 \)V suggests some form of gate leakage, and it turns out that the p-body SFET is dominated entirely by gate leakage current. This observed leakage is highly repeatable in the p-body devices, which is interesting considering the thickness (500\( \AA \)) of the gate dielectric. Considering that gate leakage in the n-body devices is very low, as shown in Fig. 12, it becomes clear that the p-Si in the p-body devices is in some way facilitating current flow through the gate dielectric. The exact mechanism/s behind this observation are, as of this writing, unknown.

Fig. 13: \( I_{ds} \) vs. \( V_{ds} \) for 2\( \mu \)m x 5\( \mu \)m p-body SFET. Gate leakage current dominates device operation, and does not allow switching via gate-induced body depletion.

V. CONCLUSION

It was the purpose of this investigation to show that field effect transistors made of metal sources and drains can function via gate-modulated tunneling, thermionic emission, and body depletion. Gate-modulated tunneling and thermionic emission have been demonstrated in the n-body MSD SFET, and the results show potential for full CMOS operation. If it is possible to creatively utilize the dual-mode behavior of the n-body MSD SFET, it might be conceivable to realize CMOS operation with one type of transistor. P-body MSD SFET operation was shown to be dominated by gate leakage, and a higher quality gate dielectric would be necessary to demonstrate the device as it was intended to operate. Additional investigations must be performed regarding single metal CMOS, temperature dependence of operation, potential for 3D circuit integration, and potential for conventional 2D CMOS in future technology nodes.

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Reinaldo Vega received the B.S. degree in microelectronic engineering from the Rochester Institute of Technology, May 2004, and will begin working towards the M.S. degree in microelectronic engineering from the Rochester Institute of Technology in September 2004.

He joined Integrated Nano-Technologies in Rochester, New York during Summer/Fall of 2001 as a Co-op student, working on fabricating prototype DNA detection devices. In Summer/Fall of 2002, he worked as a Co-op student at IBM in East Fishkill, New York, where he performed research on RF MEMS, alternative power generation techniques, and worked on copper thru-plated inductors. He returned to IBM in Summer/Fall of 2003, where he worked on SOI device characterization of thermal diodes, FETs, and electrically programmable fuses at the 90nm technology node. In Spring of 2004, he performed a NSF Research Experience for Undergraduates, working on a multi-valued logic test setup and fabrication/circuit design for resonant interband tunnel diodes.

Mr. Vega, as part of a team, received First Place in the 2004 RIT IEEE Student Design Contest for his work in MSD SFETs, and is a recipient of the 2004 Professor I. Renan Turkman Scholarship for Outstanding Achievements in Semiconductor Device Engineering.
Abstract - A Tri Gated Fin Field Effect Transistor is one of the many novel devices that may be replacing planar MOSFETs, by reducing short channel effects. The FinFET has emerged as one of the most promising double gate structures primarily because of its ease of manufacturing. There are still significant challenges to overcome it in order to make the process available commercially. The Tri-Gated FinFET is trigate meaning that the gate overlaps the top and the two sides of the FIN. Three dimensionally the gate depletes three surfaces of the FIN, which results in a higher drive current relative to a planar MOSFET. In order to reduce current crowding in the Fin corners, we have curved the corners using oxide etch back process. FinFETs has been built previously at Rochester Institute of Technology. We have designed and fabricated Tri-Gated FinFETs of various geometries. Electrical test showed poor performance of the devices. Proper scrutiny of the electrical results and the SEM micrographs allowed us to conclude that if LTO or Nitride is used as etch hard mask for silicon fin etch, electrical results closer to that of an ideal NMOS transistor could be achieved.

Key Words: FinFET, MOSFET, SOI, Ion Implant, DIBL, and Ballistic Transport.

1. Introduction:  
1.1 Need for FinFET  
The scaling of planar MOS is approaching the practical limits. With the scaling of the channel length below 50 nm complex channel profiles are required to achieve desired threshold voltages and to eliminate short channel effects. Some of the proposed bulk structures for 50 nm and beyond include Silicon on nothing (SON-planar ultra thin dual gate), Vertical MOS, Delta Doped MOSFET, etc. In all these structures, bulk doping concentration need to be increased to suppress the short channel effect; this degrades mobility, worsens sub-threshold swing and increase parasitic junction capacitance [1]. Essentially, the short channel effect reflects the extent of drain-bias influence on channel potential. In order to increase gate control electrostatics, the entire channel semiconductor needs to be "brought closer to the gate" [1]. SOI (silicon on insulator) technologies such as Full-Depleted, Ground-plane and Double gate achieve this by using a thin silicon film controlled by one or more gates [1]. Researchers have shown through extensive Monte Carlo simulations that multi-gated structures are scalable to the lowest channel length for a given insulator thickness [2]. The FinFET is a dual or tri-gated structure that has become one of the most important choices for its ease of manufacturability using well-understood Planar MOS process steps.

1.2 Silicon-On-Insulator (SOI) Substrate

The figure 1 below shows the cross section of a SOI wafer.

![Figure 1. SOI Wafer](image)

One of the most common ways to manufacture SOI wafers is by using SIMOX technology. The following process steps are done to make a SOI wafer [3].

- The starting material is typically a (100) device quality wafer. The wafer is first subjected to a high dose (~2 x 10^{19}/cm^2) oxygen (O^+) ion implantation step at high enough energy (150-300 KeV) so the peak (projected range) of the implant is deep within the silicon) 0.3-0.5μm). This step is usually carried out with the wafers held at >400°C to ensure that the silicon maintains its crystallinity during the implantation.
- The wafers are given a post-implant anneal in N2, for sufficient time (3-5 hours) at a relatively high temperature (1100-1175°C). This step forms a buried oxide (BOX) layer of silicon dioxide near the peak of the implantation and removes any many of the defects (dislocations) formed during the ion implantation step. The depth of the ion

1.3 The FinFET

The figure 2 below shows the tilted 3-D cross section of the Fin-FET....
Figure 2. 3D Tilted Cross Section of the FinFET [4]

Figure 2 above shows the 3D tilted cross section of the FinFET. The gate overlaps the fin from 3 sides. It is a type of Tri-gated MOSFET. The initial silicon doping before patterning is the same as the bulk substrate as shown above in the SOI manufacturing. Like the conventional planar MOS the fin under the gate is externally undoped. The rest of the silicon is doped with opposite polarity similar to a planar MOS. If the starting substrate were p-type 100 orientation SOI, the Fin and the source/drain would be doped with n-type dopants. The region under the gate would remain at the doping level of the starting material. At the assigned turn on gate voltage, channel would be formed in three faces of the fin, which further will define the FinFET state of operation. It has to be understood that three surfaces are getting inverted unlike single surface inversion of a planar MOSFET. The gate is high-doped n+ polysilicon or insitu doped Si_xGe_y which will be discussed in the later sections. Our FinFet Gate metal was n+ polysilicon.

2.1 Mathematical Modeling of the FinFET.

Reference [5] describes initial framework of the FinFET model with given constraints and the results are applicable for any kind of double gate MOSFET. For simplicity, the important results are written in the paper. I have modified the number of equations of reference 5 for simplifying the models to only symmetric Double Gate/FinFET structure. Figure 3b [ref 5] shows the 3D view of the FinFET showing only the silicon fin and the two gates and figure 3b is a top down schematic.

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2. Theory

The FinFET is a symmetric three-gate structure. This means that both the front back and the top gates have the same work function and are tied to the same bias, so all the three surface channels turn on at the same time. In this section the mathematical modeling of the symmetric double gate MOSFET/ FinFET Electrostatics are first explained which is followed by the Design theory, Scaling effects. Mathematical modeling for a tri-gated FinFET is still under investigation and no journal has been published. It will be similar to that of a DG-FinFET and the only difference will be an addition of a top transistor to the DGFinFET modeling results. The modeling of the top gate in the first order will just be an addition of a transistor, which is the same as a planar MOSFET, with the width of the Fin defining the width of the planar MOSFET. Thus for simplicity, we derive the current equations for a DG-FinFET in the next subsection.

\[ I_{DS} = \mu_{eff} W q_1 \frac{dV_{ch}}{dy} \]

where \( q_1 \) is the normalized inversion layer charge given by \( Q_{in}/C_{ox} \). \( V_{ch} \) is the quasi Fermi potential in the channel and the current flows in the positive y direction. The inversion charge in the channel can also be expressed by

\[ q_1(y) = q_{10} \exp \left( \frac{\phi_s(y) - V_{ch}(y)}{V_{th}} \right) \]

where \( V_{th} \) is the same as \( q_1 \) or \( kT/q \).

In the original modeling of reference 5, the two gates were considered to be asymmetric and thus to account for that an ideality factor of \( n_1 \) was used. For the case of the FinFET the \( n_1 \) term can be reduced to equation (3) as shown below.

\[ n_1 = 1 + \left( \frac{C_{si}}{C_{si} + C_{ox}} \right) \]

An expression for current in terms of charge is obtained as

\[ I_{D} = \mu_{eff} W \frac{1 + q_1}{n_1} \frac{\partial q_1}{\partial y} \]

Integrating (4) from source to drain, the drain current is explicitly given by

\[ I_{D} = \mu_{eff} W \frac{q_d^2 - q_s^2}{2n_1} \left( q_2 - q_3 \right) \]

where \( q_s \) and \( q_d \) are the normalized charge at the source and drain respectively. The author has modified equation (10) of reference 5 to get the analytical solution for \( q_1 \). Equation 6 below is an analytical solution for \( q_1 \).
$q_f = n_1 \ln \left( \frac{n_1 V_G - V_T}{n_1} - V_{ch} \right)$ \quad (6)

In order to solve for the $q_S$ and $q_D$, the $V_{ch}$ has to be replaced by the source and the drain voltage respectively. $V_T$ is the threshold voltage, which is given by equation (7) below.

$$V_T = 2V_{FB} + 2\phi_B + qN_At_s \left( \frac{C_{SL} + C_{OX}}{C_{SL}C_{OX}} \right)$$ \quad (7)

In equation (7) $t_s$ is the width of the Fin and $\phi_B$ is the fermi potential. It can be seen that the $C_{OX}$ and $C_{SL}$ are in series.

2.2 Design Theory and Dimensions:

**Fin Height [1]:**

The height ($h$) of the Fin represents the channel width of a single-fin transistor as illustrated in figure 2. The current $I_{DS}$ for conventional and FinFET transistor technologies ($I_{DS} = \text{on-current per unit channel width}$) is proportional to the channel width as shown in equation 5. Thus for a single-fin FinFET would be proportional to

$$I_{DS} \propto (2\times h) \times W_{FIN} (\alpha \text{ is the sign of proportionality})$$ \quad (10)

Where ‘h’ is the height of the Fin and the width of the side channels. If more Fins are placed the right side of equation has to be multiplies by the number of Fins. The equation becomes

$$I_{DS} \propto [(2 \times h) \times n_{Fin} (n_{Fin} \text{ is the number of Fins}) + n_{Fin} W_{FIN}]$$ \quad (11)

From the above equation it can be seen that increasing the number of Fins can increase the drive current.

If multiple Fins are used, the following conditions has to be used:

$$2 \times h \geq \text{pitch}$$ \quad (12)

3. Designs and Fabrication:

FinFETs of various geometries were designed. The smallest device had a Fin Width of 0.5um and Gate Width of 05um. FinFETs of other geometries were also included in the mask. FETs with multiple fins were also included. Below are fabrication process steps listed in sequence starting from Level 1 the Alignment Level.

1. Starting Substrate: 100 P-type silicon wafer with BOX thickness of 2300 and Silicon thickness of 3750.

2. Lithography Level 1: Alignment Marks Patterning.

Loading effect, the etch time was very different from the target etch time.


7. After the Resist ash was done, a sacrificial SiO$_2$ of thickness one 160Angstrom was grown. The Sacrificial Oxide was then etched away using Hydrofluoric Acid Chemistry. This step was done for two reasons. Firstly for rounding the corners for the Fin/Fins so that current crowding or spreading resistance effects can be prevented. The next reason was to prepare the surface for the gate oxide.

8. Gate oxide of 580Angstrom was grown using the Bruce Dry Oxide Furnace. For the prevention of Fixed Charges, nitrogen annealing was done after growth step.

9. Poly Silicon of thickness 2300Angstrom was deposited using Low Pressure Chemical Vapor Deposition.
10. Level 3 Lithography: Gate Patterning

After the gate was patterned, the polysilicon in the unmasked area was etched using the Dry Tech Quad Reactive Ion Etcher Etcher. The etch recipe was as follows:

- RF Forward Power: 185 Watts
- SF₆: 30 SCCMs
- CHF₃: 30 SCCMs
- Pressure: 43 mTorr
- Etch Time: 2 minute 10 seconds.

12. Resist Ashing in Branson Asher was done using oxygen plasma.

13. Ion Implantation for Self-Aligned Source/Drain and Gate:

Ion-Implant of phosphorus using the Varian 350D ion-implanter was done to introduce dopants into the polysilicon gate and source/drain. In order to prevent channeling and implant damage the implant in the Source/Drain area was done through the 580 Angstrom dry oxide. The implant conditions were as follows:

- Implant Specie: P³⁺
- Implant Energy: 60 KeV
- Implant Dose: $1 \times 10^{15}$/cm²


Annealing the wafer at 1000°C for 15 minutes in the furnace activated dopant ions.

15. Oxide Etch:

Oxide in the Source/Drain area etched using Hydrofluoric Acid base etchant.

16. Aluminum Deposition:

The source/drain contact area was slightly bigger than the probe contact area. Thus a separate contact mask was not used. To make an ohmic contact with the sour/drain 2000 Angstrom of aluminum was deposited by evaporation using the CVC evaporator. The base pressure of the evaporation process was $4.2 \times 10^{-6}$ Torr.

17. Level 4 Lithography: Metal Patterning:

Aluminum in the Source/Drain and Polysilicon contact area were masked using photoresist.

18. Aluminum Etch:

Wet Aluminum Etch was done in the unmasked areas using phosphoric acid based chemistry. The etch time was 47 seconds, which includes a 100% over etch.

19. Sintering:

To make the contact ohmic, the wafer was sintered in the furnace at 450°C in Forming Gas ambient.

**4. Electrical Results and Analysis:**

Electrical tests were done using the Keithly 8200 Semiconductor Parameter Analyzer. The electrical results showed very poor performance. Figure 4 below shows the drain family of curves for one of the FinFETs.

![Figure 4: Drain Family of Curve for a NFET FinFET.](image)

A proper scrutiny of figure 4 shows that, current flows only had very high Vds. The current flow decreases as the gate bias is increased. All the other transistors showed similar performance. In order to further investigate the results, we took high magnification scanning electron micrographs of the devices. Figure 5 shows the SEM micrographs:

![Figure 5a: FinFET of 0.5 gate length and 4um Fin.](image)

![Figure 5b: FinFET of 0.5 gate length and 0.8um Fin](image)

Investigation of the electrical results show that, there were large pits and holes in the silicon fin and the source drain areas. This pit and holes came from the second level etch, that is the etch of the Source/Drain and Fin as described in the process flow. The pits and the holes pattern got transferred in the other levels. Another FinFET project was conducted with my project [6], which used low temperature oxide as a hard mask to etch the silicon Fin. A SEM micrograph of the other project using LTO as a hard mask after the Source/Drain and Fin etch is shown in figure 6.
Figure 7: Electrical Result of FinFET [6]

After investigating and analyzing the results we can say that photo resist alone is not a sufficient etch mask. The other group's FinFET works because it is protected by a separate hard mask. The roughness caused holes and voids to be formed through the box. The roughness also transferred to the Polysilicon Gate. As a result, the fin was highly resistive and the metal short-circuited with the silicon under the BOX. This caused Current Flow from under the Box at high Vds. Further Field Effect due to increasing Vgs, reduced the current flowing under the gate.

5. Conclusion:

Our 620 Resist is not sufficient to mask the silicon etch due to its poor selectivity. This results in highly resistive Fin. We learned that a hard mask like LTO or silicon nitride has to be used for the silicon fin Etch.

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Development of Thin Gate Oxides for Advanced CMOS Applications

Bryant Mann, Rochester Institute of Technology

Abstract— A study has been performed to investigate oxynitrides as thin gate dielectrics. The method of nitridation was a two step process involving variations of nitrous oxide and oxygen thermal soak times. The investigation of oxynitride gate dielectric was carried out through the fabrication of MOS capacitors. Thickness measurements were obtained using VASE ellipsometry and CV analysis was performed to test the electrical integrity of the dielectric. The CV analysis resulted in high frequency curves that displayed a low frequency response due to minority charge.

Index Terms—Oxynitride, thin oxide, nitrous oxide, CV analysis, breakdown, VASE

I. INTRODUCTION

THERMALLY grown films of silicon dioxide serve various key roles in the fabrication and operation of integrated circuits. The most critical role of silicon dioxide is its use as a MOSFET gate dielectric. The gate dielectric for a MOSFET must satisfy a number of demands to be successful and silicon dioxide has been successfully used since the early 1970's. One demand is that the oxide thickness must be controlled to the desired thickness that matches the design specifications of the MOSFET. This thickness must be sufficiently uniform across the wafer, wafer to wafer, and from run to run. Another requirement is an electrically stable interface for the oxide film and the silicon surface including minimal values of charge in the oxide and at the interface. The oxide film must also exhibit a dielectric breakdown strength in the 8-10 MV/cm range implying a pinhole free film that contains a negligible number of defects that would cause breakdown at lower than expected electric fields. The dielectric must be chemically, electrically and thermally stable under the processes for fabricating integrated circuits and compatible with other materials used during manufacturing. The oxide must also exhibit sufficient levels of leakage-current to meet the off-state current leakage requirements of the integrated circuit. Furthermore, the oxide needs to exhibit high resistance to hot-carrier damage and the oxide needs to be resistant to boron penetration or out-diffusion during subsequent processing temperatures. Lastly, the most important requirement of a gate dielectric is its ability to be scaled in thickness with the scaling of transistor channel lengths.

As CMOS integrated circuit technology advances, the main focus of scaling the MOSFET is with respect to scaling the gate length. The advantages of scaling the gate length include an increase in the drain current, a decrease in gate area of the minimum sized transistor, both of which lead to improved circuit speed, and thirdly an increase in the density of devices per chip. However, scaling of the gate length in deep sub-micron devices can lead to unwanted short channel effects such as drain-induced barrier lowering (DIBL). DIBL is an increase in the subthreshold (off-state) drain current, $I_{	ext{Dss}}$, as the gate length is reduced. The subthreshold drain current is one component of the total off-state leakage current.

Two measures to reduce this effect are shallow source/drain extension regions and reducing the depth of the channel depletion region. The second measure is achieved by increasing the dose of the threshold adjust implant to increase the doping in the channel. However, if the gate oxide thickness remains constant, the threshold voltage is increased as the doping concentration near the surface is increased. Since the threshold voltage is held constant or is slightly decreased as MOSFETs are scaled, the increased threshold voltage due to increased channel doping must be offset. This can only be done by decreasing the gate oxide thickness. In summary, this means to continue to scale the gate length of transistors, the gate oxide thickness must be decreased by approximately the same scaling factor as the gate length.

II. THEORY

One modification to the basic silicon dioxide gate material that has been examined is the incorporation of nitrogen into the oxide (oxynitrides). Oxynitrides have been studied as replacement gate dielectrics for thicknesses below 4.0nm. There are four main advantages of oxynitrides over silicon dioxide as the gate dielectric. The first and most important being improved suppression of boron penetration which can lead to shifts of the threshold voltage. Boron has a preference to outdiffuse from the poly gate and reside in the oxide. The incorporation of nitrogen into the gate dielectric prevents this
mainly due to an increased lattice density which prevents diffusion. The second advantage being improved hot electron immunity. This results in larger electric fields being allowed with the same level of hot electron reliability. The third advantage being improved breakdown characteristics and reliability. The incorporation of nitrogen into the dielectric improves the integrity and breakdown characteristics depending on the concentration of nitrogen, however too high a concentration will reduce the benefits and even lead to large flatband voltage shifts. The fourth and final benefit being increased high-field electron channel mobility.

Nitridation of oxides is considered a variation of silicon oxidation. Such films are formed through the nitridation of silicon dioxide by the oxidation of silicon in a nitrogen containing ambient (NH₃, N₂O, NO), or thermal growth of nitrogen-implanted silicon. Figure 1 below depicts the multiple methods used to incorporate nitrogen which include thermal and physical and chemical vapor deposition methods.

Figure 1: Methods of Nitridation

Exposing silicon dioxide films to pure ammonia (NH₃) or nitrous oxide (N₂O) at high temperatures and atmospheric pressures will cause thermal nitridation of silicon dioxide. This technique will result in a mostly silicon dioxide film with nitridation occurring at the silicon surface and the silicon-dielectric surface.

The reactions that lead to the nitridation of the dielectric are shown in figure 2. The introduction of nitrous oxide into the furnace tube will rapidly decompose it into N and atomic oxygen. The atomic oxygen will then initiate a series of reactions to form nitric oxide. This is the key step of the reactions as nitric oxide is the main nitriding agent. The nitric oxide will then diffuse through the SiO₂N₆ layer and react with silicon at the surface to incorporate nitrogen. However, nitrogen is also removed due to the atomic oxygen and the concentration of nitrogen is dependant on the amount incorporated and the amount removed by the atomic oxygen.

However, the use of a hydrogen containing ambient results in a higher fixed charge density (Qf) and a large number of electron traps (Q0) in the dielectric film. These charges and traps will shift the threshold voltage and reduce stability under hot carrier stressing. To alleviate this issue, the NH₃ ambient can be replaced with N₂O to avoid hydrogen incorporation. This is usually performed as a two-step oxidation with an oxide grown in dry O₂ followed by a nitridation step or a post-oxidation anneal in the N₂O ambient.

The placement of the nitrogen peak can be engineered based on the application. To aid in the suppression of boron penetration from a P⁺ doped poly gate the peak would be desired away from the surface and below the gate. However, this profile would not serve as a good barrier for hot carrier immunity. For that application a nitrogen peak near the surface would be preferred to prevent hot carrier injection. The engineering of the nitrogen profile results from the ambient the oxynitride is grown in and the order of the oxidation and nitridation steps in a two-step recipe.

A uniform nitrogen profile can be achieved by growing the dielectric layer in a nitric oxide (NO) ambient. Dielectrics grown in a nitrous oxide (N₂O) ambient will have a peak near the dielectric-substrate interface. This profile can be attributed to some of the nitrogen being removed from atomic oxygen.
A peak near the interface may also be achieved by annealing a previously grown oxide in a nitric oxide or nitrous oxide ambient. The peak near the interface may also be attributed to the removal of nitrogen near the surface by atomic oxygen. A reoxidation of a previously grown oxynitride layer in an $O_2$ ambient will push the nitrogen peak away from the interface and towards the poly gate.

Figure 3: Nitrogen peak location for NO and $N_2O$ grown films

Figure 4: Nitrogen peak location for NO, $N_2O$ and Reoxidized grown films

### III. EXPERIMENT

To investigate the properties of the nitrided oxide, capacitors were manufactured using two different recipes for the formation of the oxynitride layer. The wafers were cleaned in a standard RCA clean and followed by a final HF dip to ensure there was no moisture on the surface of the wafers. A TransLC chlorine clean was performed on the thermal furnace tube to reduce sodium ion contamination of the furnace tube and quartzware. The oxynitride was grown at 900°C with a 30 minute soak in nitrous oxide. This was followed by two splits of the oxygen soak, a 20 minute soak and a 10 minute soak. Next inline measurements of surface charge analysis on the SCA and oxynitride thickness measurements using the VASE ellipsometry. Aluminum was then evaporated instead of sputtered to eliminate unnecessary plasma damage. The aluminum was then patterned using a g-line stepper with the standard capacitor mask and NMOS active mask. The aluminum was then etched in a wet bath and the resist removed in wet baths instead of being ashed to eliminate plasma damage.

The manufactured capacitors were then tested using the Keithley 82 test setup. High frequency capacitance voltage measurements were performed on the capacitors. The voltage was swept from -4 to 2 volts in 20mV steps with a 70ms delay between steps.

### IV. Results and Discussion

The VASE measurements carried out inline yielded the thickness measurements of the nitrided oxide. The thickness for the thirty minute $O_2$ soak was 149Å. The thickness for the twenty minute $O_2$ soak was 92 Å. Following the above described testing procedure, capacitance voltage analysis of the capacitors was also performed. The two different splits were measured with varying size gate areas. The plots for the two different splits are shown below in figures 5 and 6.

Figure 5: 149Å Gate Oxide High Frequency CV Measurement

The capacitance voltage curves are high frequency measurements. However, both curves display a low frequency characteristic by the inversion portion of the curve rising towards the accumulation section as happens during low frequency sweeps. This low frequency response can be attributed to minority charge being available at the field regions of the dielectric surrounding the gate. This minority charge does not allow the gate to fully invert the region underneath it and this results in the low frequency response.
Figure 6: 92A High Frequency CV Measurement of 100Kum Gate Area

The capacitance voltage curves in figure 6 display the same low frequency response as the curves in figure 5. However, the three curves are from different areas of the wafer and the response in the inversion portion is different for each curve. The shift in the response between the three curves could be attributed to different charge levels across the wafer which would result in different levels of minority charge. However, more investigation would need to be done to further examine the reasoning.

V. CONCLUSION

This study investigated the methods of nitriding an oxide dielectric and employed a two step oxynitridation recipe. The two splits on soak times yielded different gate dielectric thicknesses showing the ability to scale the oxynitride. MOS capacitors were successfully fabricated to demonstrate electrical use of the oxynitride dielectric. The expected trend of oxide capacitance dependency on gate area was still obtained. However, the high frequency CV measurements demonstrated a low frequency response and further work to investigate this issue should be carried out.

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Capacitance-Voltage Analysis of High-\(\varepsilon\) Dielectric on Strained Silicon

Mike Latham, Student Member, IEEE

Abstract—Device characteristics are reported on HfO\(_2\) gate dielectrics deposited by atomic layer deposition (ALD), and jet vapor deposition (JVD) on strained-Si and bulk Si samples. Capacitance-Voltage (CV) analysis of samples shows comparable interface charge levels between strained-Si and bulk Si samples. A flat band shift of \(-0.5\) V was noted between the strained-Si and bulk Si for the JVD samples.

Index Terms—Capacitance Measurement, Hafnium, Strain

I. INTRODUCTION

The scaling of MOSFET devices has allowed for tremendous performance improvements in the semiconductor industry for years. However, with the current trends in scaling the use of a conventional Si-MOSFET will reach its limits by the year 2005 [1]. In order to reach the drive current necessary for the 90nm node a change in the conventional MOSFET structure will be needed. With the introduction of a strained-Si layer in the channel of the device a mobility enhancement can be seen resulting in a higher drive current [2]. Another concern for the continued scaling of MOSFET devices is the SiO\(_2\) gate dielectric. The current devices with 1.3nm gate oxides seem to have reached a fundamental limit with SiO\(_2\). As the gate oxide thickness is reduced below this thickness the leakage currents present between the gate and the substrate present a major concern. In an attempt to circumvent these fundamental limitations extensive investigations have been done in search of high-\(\varepsilon\) dielectrics suitable for the replacement of SiO\(_2\) as the gate dielectric in MOSFET devices.

This study investigates the integrability of strained-Si substrates with high-\(\varepsilon\) dielectrics, Hafnium oxide (HfO\(_2\)). Metal Oxide Semiconductor (MOS) capacitors are manufactured using a high-\(\varepsilon\) dielectric for the oxide on strained and bulk Si samples. CV measurements are made on each of the capacitors and the traces are compared to determine interface qualities.

II. THEORY

A. Strained Silicon

Strained-Si is being investigated as a direct replacement to bulk Si for MOSFET fabrication. With the introduction of strained-Si into the channel of the device can increase drive currents, while decreasing the power consumption. Strained-Si substrates are fabricated using multiple epitaxial thin film growth steps forming a stack of films on the silicon substrate. The first film grown on the substrate is a Silicon Germanium (Si\(_{1-x}\)Ge\(_x\)) heterostructure layer, used as a strain introduction layer. Next, a 10-40nm layer of pseudomorphic silicon is epitaxially grown on the Si\(_{1-x}\)Ge\(_x\) layer. The lattice spacing of the Si\(_{1-x}\)Ge\(_x\) layer is different than that of the Si layer grown on the relaxed Si\(_{1-x}\)Ge\(_x\) layer. This difference in the lattice spacing causes the atoms of the grown Si layer to adjust to match the lattice spacing of the underlying layer. As the Si atoms conform to the underlying layer the lattice is stretched in the lateral direction causing a biaxial tensile strain in the silicon lattice. The introduction of the strain into the Si increases the effective mobilities of the carriers in the strained-Si layer. This mobility enhancement comes about as a result of the energy band splitting of the \(\varepsilon_{24}\) conduction bands due to the vertical electric field in the MOS devices [3]. As these energy levels are repopulated the carriers are at a lower energy reducing the effective mass and increasing the low field effective mobilities. The amount of band splitting and the energy band gap throughout the can be calculated using the method presented by Richard based on the percent of Ge contained in the relaxed Si\(_{1-x}\)Ge\(_x\) layer [4].

B. High-\(\varepsilon\) Dielectrics

As transistors are scaled the gate oxide thickness must also be reduced to maintain a constant electric field in the device. As the thickness of the gate oxide begins to approach 2nm the gate leakage current begins to increase exponentially [5]. These large leakage currents have detrimental effects on the device performance as well as a drastic increase in the power.
consumption. The attempt to reduce these leakage currents is the main driving force behind the switch to alternative gate dielectric materials. These leakage currents arise due to electron tunneling through the gate dielectric. With increased scaling the oxide is correspondingly reduced, resulting in elevated leakage currents. By increasing the relative permittivity of the dielectric being used for the gate a thicker film can be deposited while maintaining the same capacitance. By making the gate dielectric thicker the direct tunneling of carriers from the gate can be prevented. The relative permittivity of the high-$\varepsilon$ dielectric and the equivalent oxide thickness (EOT) are related by (1).

$$EOT = \frac{\varepsilon_{ox}}{\varepsilon_{nit}} T_{\text{physical}}$$  \hspace{1cm} (1)$$

Where $\varepsilon_{ox}$ is the dielectric constant of SiO$_2$, $T_{\text{physical}}$ and $\varepsilon_{nit}$ are the physical thickness and dielectric constant of the high-$\varepsilon$ film respectively.

There are many properties of the new material that must be taken into consideration when choosing a new dielectric. These include the thermodynamic stability with silicon at elevated temperatures, the dielectric constant, and the conduction band offset. Some of the candidates being explored to replace SiO$_2$ are; Tantalum Pentoxide, Aluminum Oxide, Zirconium Oxide, and Hafnium Oxide. For this investigation Hafnium Oxide (HfO$_2$) was used because of its physical characteristics, dielectric constant around 20, thermodynamically stable with Si up to 950°C, and has a conduction band offset of 1.5 eV.

III. EXPERIMENT

NMOS capacitors were fabricated on strained and bulk Si substrates with boron background doping of approximately 5 x 10$^{15}$ cm$^{-3}$. Strained-Si substrates were donated by AmberWave Systems, upon receipt these 200mm wafers were laser cut into two 100mm wafers. After this, the wafers were cleaned using a standard RCA clean to prepare the surface for dielectric deposition. Wafers were sent to University of Texas at Austin were an HfO$_2$ film was deposited by ALD, and a TaN gate material was deposited using a reactive sputter technique. At the same time wafers were sent to Yale University for HfO$_2$ film deposition by JVD. Al gate material was deposited using evaporation. The gates were then patterned using a g-line stepper exposure system. The Al gates were etched using a phosphoric, nitric and acetic acid wet chemistry mixture. The TaN gates were etched using a CF$_4$ RIE technique.

The samples were then characterized using a Keithley 82 CV meter. Capacitance curves were measured from -4V to +2V in the forward and reverse directions. Also, VASE measurements were used to determine the HfO$_2$ film thickness.

IV. RESULTS AND DISCUSSION

The interface between the gate dielectric and substrate is a critical part of the MOS device. The quality of this interface affects all aspects of the operation of the device. A degraded junction between the dielectric and substrate will decrease transconductance lowering the overall performance of the device. SiO$_2$ has a very high quality interface with Si. In fact this aspect of SiO$_2$ and Si has been a large driving factor for staying with Si for so long. In order for a new high-$\varepsilon$ dielectric to replace SiO$_2$ the charge levels of the interface must be kept low near the levels of SiO$_2$. Without these low charge levels the new material will not be accepted as an alternative.

![Figure 1: CV Curves for ALD deposited HfO2 filmson a.) bulk Si and b.) Strained-Si](image-url)
A. ALD HfO₂ Capacitors

Figure 1 shows the CV characteristics at 100 kHz for MOS capacitors with 5nm of ALD HfO₂. The bulk Si trace is shown in figure 1a and the strained-Si trace is shown in figure 1b. The calculated equivalent oxide thickness (EOT) for these samples is approximately 1.74nm for the bulk Si and 1.89nm for the strained-Si sample. These values were calculated using a SiO₂ dielectric constant of 3.9 and equation (2):

\[ C_{ox} = \frac{\varepsilon_{SiO2} A}{EOT} \]  

(2)

Where \( \varepsilon_{SiO2} \) is the dielectric constant of SiO₂ (3.9), A is the area of the capacitor and \( C_{ox} \) is the oxide capacitance of the capacitor during accumulation. TEM images of the dielectric film show the presence of an interfacial layer between the HfO₂ and the substrate. This interfacial layer is mostly SiO₂ and is shown to historically be between 0.5-0.7nm for films of this thickness. Using the following equation the high-\( \varepsilon \) dielectric constant can be calculated.

\[ EOT = \varepsilon_{SiO2} \frac{T_{int}}{\varepsilon_{int}} + \varepsilon_{SiO2} \frac{T_{hi}}{\varepsilon_{hi}} \]  

(3)

Where \( T_{int} \) and \( T_{hi} \) are the thicknesses of the interfacial layer and high-\( \varepsilon \) dielectric respectively, and \( \varepsilon_{SiO2} \), \( \varepsilon_{int} \) and \( \varepsilon_{hi} \) are the dielectric constants of SiO₂ the interfacial layer and the high-\( \varepsilon \) dielectric respectively. Using equation (3) the dielectric constants were calculated to be 18.8 for the bulk Si sample and 16.4 for the strained-Si sample. The capacitance curves for these two traces overlay one another almost perfectly. This shows that the charge levels in these two samples are nearly identical. The differences in the two traces in the accumulation region is minimal and is most likely due to differences in the as etched capacitor areas.

B. JVD HfO₂ Capacitors

Figure 2 shows the CV characteristics at 100 kHz for MOS capacitors with 5.7nm of JVD HfO₂. HfO₂ film thickness was measured using variable angle spectroscopic ellipsometry (VASE). Using the accumulation region oxide capacitance and equation (2) the EOTs for these samples were calculated to be 2.11nm for the bulk Si sample and 2.24nm for the strained-Si sample. TEM images of the JVD samples show that the interfacial layer is slightly larger, approximately 1.2 to 1.5nm of SiO₂. Using 1.2nm for the interfacial oxide thickness and equation (3) the dielectric constants were calculated to be 24.4 for the bulk Si sample and 21.3 for the strained-Si sample. Looking at these two traces the first thing that was noticed is the flat band voltage shift. The flat band voltage of the strained-Si sample is approximately 0.5 volts lower than that of the bulk Si sample. This shift cannot be said to be caused by the strained-Si because the ALD samples did not show this shift. At this time the cause of the shift is unknown. Other than the shift the strained sample has less of a hysteresis effect from the dual sweep. This implies that the charge levels in the

V. CONCLUSION

The study showed the ability of incorporation of HfO₂ and...
strained-Si in a MOS device. Interface charge levels were shown to not have any large affect on the CV response of the device. Future work should be done to further characterize and explore the effects of the interface on device performance as well as full MOSFET fabrication incorporating HfO2 and strained-Si.

ACKNOWLEDGMENT

The author would like to thank Dr. S. Kurinec, Dr. S. Rommel, and Dr. K. Hirschman for their guidance in this project. Also, a special thanks to the RIT Semiconductor and Microsystems Fabrication Laboratory staff for technical assistance and support on tools. A special thanks is given to AmberWave Systems for donation of strained-Si wafers making this work possible.

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Mike Latham (S’04)Originally from Syracuse, New York, received a B.S. degree in microelectronic engineering from Rochester Institute of Technology in May 2004. He obtained co-op work experience from Fairchild Semiconductor Mountaintop, PA. He is currently pursuing an M.S. degree in microelectronic engineering at RIT.
Work Function Engineering With Molybdenum and Molybdenum-Nitride Gate PMOS

Valarie Welsh

Abstract — The motivation for the creation of RIT metal gate PMOS process transistors was to investigate and prove the work function of molybdenum can be changed through reactive sputtering and thermal processing. The existing RIT metal gate PMOS process was adapted to form Molybdenum and Molybdenum-Nitride PMOS transistors. Processing of the molybdenum films affected the final composition of the gate electrode and ultimately its work function. Through theoretical and real analysis, the work functions of Mo and MoN gates were extracted and compared with one another as well as to Al. Examination of the extracted work functions revealed the presence of other phenomena accountable for 1.5-2.0V shift in $V_t$ from one gate type to another. While no single mechanism is identified as the source of extra charge, contamination of the Mo/SiO$_2$ interface, oxidation of the Mo, work function difference, or some combination of all three are likely to explain the shifts in threshold voltages.

Index Terms — Work function, PMOS, Amorphization

I. INTRODUCTION

The 2003 International Technology Roadmap for Semiconductors predicts that by 2005-2007, the CMOS industry will steer toward several paradigm shifts in standard processing to meet the projections of Moore’s Law. Specifically it is projected that the polysilicon gate electrode and SiO$_2$ gate dielectric will be replaced with alternate materials. A major goal of replacement gate technology is the ability to tune the threshold voltage via the gate metal work function independently for PMOS and NMOS transistors. With a focus on reducing gate resistance and preventing tunneling and leakage current, a modification of the currently used RIT Metal Gate P-type MOS process has been created. The modification concentrates on the replacement of the Aluminum gate with the mid-gap work function metal of Molybdenum and Moly-nitride. Research shows Mo and MoN to be compatible with other dielectric films. Because so much attention is given in research to hi-k dielectrics, it is important to recognize that alternative gate materials must be well suited for them. The Mo work function of ~ 4.5eV makes it a promising candidate material for use with Silicon substrates. Because it is a metal, it ensures the prevention of gate depletion and offers significant reduction in resistance. However, in using metal gate materials, the work function required for a desired threshold voltage is not so easily achieved or changed and eithe: must be varied with an alloy mixture and/or dimension. By conducting this project, the further establishment of an alternative gate process at the RIT SMFL will be achieved. Additional knowledge of the benefits and drawbacks of alternative gate materials will be realized.

II. MOTIVATION

As scaling of integrated circuits continues, new challenges for engineers arise. As channel lengths become smaller, the issues with polysilicon as gate electrode tends to grow. Resistance at the gate becomes an issue, as this characteristic does not scale equally with channel length. Also, with existing CMOS technology threshold adjustment doping at the gates can be hard to control. If the gate material is doped to heavily, excessive concentrations of dopant in the gate can punch through thin gate oxides (assuming SiO$_2$). If doped too lightly, depletion of dopant from the gate/dielectric interface may occur. This gives rise to the poly depletion effect.

Figure 1: Polysilicon Depletion Effect

Inadequate concentrations of dopant at this region can interfere with traditional carrier movement at the gate and dielectric interface when biased into strong inversion. This
mechanism is responsible for degradation of drive current and increases the effective oxide thickness.

III. DEVELOPMENT

Using Molybdenum as the gate electrode would resolve these issues. As a highly conductive metal, Mo offers low gate resistance. Its thermally resilient melting temperature of 2610°C and thermal coefficient of expansion of 5E-6/°C 20°C allow for much greater latitude with thermal budget and alleviates concerns regarding interfacial lattice stress. These characteristics make Mo attractive for self-aligned gate technology. Molybdenum also has a stable contact with SiO2 up to 1000°C again fitting nicely with existing and aging technology. Most importantly however, is the range of work functions this material is reported to have.

According to Ranade, the reported work function values for Molybdenum range from 4.2 to 4.7 electron volts. When implanted or otherwise combined with other materials and processed this range has been seen to vary 4.0-5.0eV[1]. Ranade’s work has shown that post sputter annealing alone (400-900°C) will raise the Mo work function by .7or .8 volts indicating that thermal processing has an effect on Molybdenum films. According to his work, "annealing in argon ambient produced results similar to annealing in forming gas ambient even after taking the effects of oxide fixed charge into account." This work function has been altered by almost a volt before implanting or reactivity sputtering it with anything else. It is generally accepted that the work function for molybdenum in device applications is dependent upon the conditions of its deposition and subsequent processing. Sputtering is the most widely used method for deposition. It is surmised that only plasma is feasibly capable of depositing refractory metal films. While literature is scarce, it is believed that the work function of Mo is initially determined at the initial deposition [2]. The morphology of the film at the dielectric interface is theorized to determine the work function of the film in this area. Naturally then the initial state of the film morphology will ultimately influence the final arrangement of the film and the measured work function.

A high percentage of the research available addresses the implantation of nitrogen and argon into sputtered molybdenum films. The formation of Moly-nitride through implantation is theorized to amorphize the Mo film structure. The breakage of surface bonds is detected by a negative shift in the flatband voltage. The corresponding work function is therefore lowered.

Process

Adapted from RIT’s metal gate PMOS process, one lithography mask was substituted and one added to incorporate Aluminum contacts and Molybdenum and Molybdenum-nitride gate electrodes. The metal gate PMOS process:

- Scribe, 4pt probe, RCA Clean
- Masking Oxide Growth 5000Å

Figure 2: Representative Cross-section through pattern oxide growth

- Level 1 Lithography opens S/D regions
- Pattern Oxide through BOE

Figure 3: Representative Cross-section through S/D opening

- RCA Clean, Spin on Boron Dopant
- Furnace Pre-deposition
  - drives dopant into surface
  - consumes Si in S/D region

Figure 4: Representative Cross-section through SOG application

- BOE all material from surface

Figure 5: Representative Cross-section through S/D predeposition

- Grow Field Oxide 5000Å while driving in S/D

Figure 6: Representative Cross-section through Field Oxide growth and S/D drive-in

- Level 2 Lithography opens active device area
- Pattern Oxide through BOE

Figure 7: Representative Cross-section through active area definition
IV. FABRICATION

The current PMOS process uses Al for the gate and source drain contact. Recently Boise State University in conjunction with RIT has conducted research using alternative gate materials and had ordered a lithography mask for this process that patterned the gate separately. The process uses a spin on glass for the source and drain formation followed by a drive in and field oxide growth process that gives a junction depth of about 1.5um. Aluminum was used for the source and drain to ensure and ohmic contacts in these regions. The aluminum pattern was followed by a lot split where some wafers received Mo sputter deposition and others were reactively sputtered with MoN.

A separate designed experiment with reactive sputtering was conducted to determine what ratio of nitrogen was appropriate in the creation of a Moly-nitride film. As nitrides are classically insulators, the DOE was used to establish what percentage of nitrogen in the sputter would give the lowest resistivity.

At the lower limit of the nitrogen flow, resistivity in the Moly-nitride film dropped from independently sputtered Molybdenum. As the incorporation of nitrogen in the film increased, tensile stress in the film was more and more evident and resistivity appeared to increase linearly. While the experiment was not repeated, the substrates used were of various oxide thicknesses in attempts to normalize the results. The theory is that plasma induced damage would have the same amorphizing effect on the sputtered film as the nitrogen implantation of previous research. A 3% ambient content of Nitrogen was concluded to give the lowest resistance.

Once the gate electrode material was deposited the original RIT metal gate PMOS gate and contact mask was used. This resulted in the formation of a double contact to the source and drain, the wafers were then etched with the same phosphorous wet Al etch chemistry and sintered in forming gas at low temp.

V. RESULTS

Following the sinter process, the appearance of the devices showed corrosion and contamination of the gate material.
Microscopic inspection revealed the gate material was brown “spongy” in appearance and easily removed.

In fact, “MoO2 is known to be conductive and hence as long as the MoO2 is formed without chemical reaction at the interface, oxidation is unlikely to alter the oxide capacitance.” --Ranade[1].

Without an without timely access to (EDS) analysis one cannot definitively say whether Mo or MoO2 is present on the gate.

Further analysis a threshold voltage shift from Al to Mo gate transistors on the same chip. With “documented” work functions of Al=4.1 & Mo=4.5 The calculated difference between the metals should be approximately .4volts. It stands to reason identically manufactured transistors would be expected to exhibit just this shift. Even with a widely ranging work function for the Mo, there remains a 1.5- 2 volt shift in positive direction for Vt. This amount of charge must then be accounted for with Nss & substrate doping. Understanding that almost all incidental are positive in nature, and that those encountered would push the threshold voltage to be more negative there arises the question of where negative charge could have been picked up and trapped after the aluminum deposition.

Notice again the process flow used. With this sequence, the gate oxide cannot be cleaned once the aluminum is applied. Using the aluminum etch followed by an IPA/IPO resist removal process offered the first and best possibility for source contamination. The threshold voltage and flatband equations are typically used to extract the quantity of excess charges in a device when the gate work function is already known. Using the documented value for the Al work function, the excess trap charge density was calculated to be 1.26E19/cm. Using this estimation for the adjacent Molybdenum gate device the work function of the gate electrode was calculated to be 5.99eV.

MoN Re-process Description

Recognizing that only two processes were performed with Molybdenum (pattern and sinter) the remaining wafers were re-processed to determine whether the wet Al etch or the sintering would give rise to this same Vt shift. Both wafers were cleaned, and 1500Å of Al evaporated, patterned and etched with the same Phosphorous Al etch bath. Again the IPA/IPO solvent resist removal was performed. Then one of the remaining two wafers was sintered at 400°C 30min and both reactively sputtered with 1700Å of Molybdenum-nitride (3%). The MoN gates were then patterned and the sintered wafer etched again with the Al wet etch. The other wafer was plasma etched with SF6 for 3min, solvent removal performed again followed by its own sinter.

The wafer that received no MoN thermal process produced a comparable family of curves to the original Mo gate devices, but looked very different.

Figure 15: “Molybdenum” Gate electrode post sinter

Figure 16: “Molybdenum” Gate Family of Curves

Indeed, further research proved Molybdenum is “highly prone to oxidation at elevated temperatures....”[1].
Indeed, the threshold voltage was lower than that of the Mo gate device as predicted. The wafer that received the plasma MoN etch followed by a sinter in forming gas appeared as expected upon emergence from the furnace. Unexpectedly though, none of the devices tested have yet yielded.

VI. CONCLUSIONS

Regarding the comparison of Mo to MoN gate transistors, the extracted work functions for each were found to be $-0.7$ and $-2.0$ volts respectively. While the work function of the gate materials has shifted 1.3 volts, the Al to Mo gate comparison and the appearance of the Mo post sinter cannot be ignored. The threshold voltage difference is more likely the result of a combination of work function difference, contamination from negative charges in the wet metal etchant, and the nature of the oxidized film at the gate. The last of these hypothesis is supported by the belief that oxidized Molybdenum would raise the work function of the gate electrode.

The first, best solution to guarantee a Mo to MoN gate electrode comparison would be the manufacture of the gate first as is ideal in self-aligned gate processes. Further work should also be done to ensure that the Mo is not oxidized during subsequent processing.

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The Interaction of Ultra-Pure Water and Photoresist in 193nm Immersion Lithography

James H. Park

Abstract—The proposed paper investigates the effects of ultra-pure water on DUV photoresist used in 193 nm immersion lithography. Microlithography is the key technology that is pacing Moore's Law. With critical transistor features reaching the 45nm device node, the development for new techniques in optical lithography are well underway. Large investments have been made into the Next Generation Lithography (NGL) technology development such as VUV (vacuum ultraviolet) and EUV (extreme ultraviolet) projection lithography. However, an extension of optical imaging at 193 nm deep ultraviolet (DUV) to immersion lithography at the same wavelength offers considerable potential for it to be used as a next step in production, postponing the introduction of EUVL.

Index Terms—193nm Immersion Lithography, EXITECH, Microstepper, Photoresist, SEM (Scanning Electron Microscope) and Ultra-pure water

I. INTRODUCTION

Immersion lithography technology involves the use of an immersion fluid between the lens and the wafer to enhance the patterned image in the photoresist. This phenomenon is based on the discovery by Ernst Abbé in the 1870’s, who enhanced his microscope by using oils that matched the index of refraction of the glass. The matching index of refraction prevents reflective effects at the interfaces of the lens and the sample. By using ultra-pure water between the objective lens and the wafer, the resolution of the features could be theoretically enhanced by 43% due to the difference of indices between water and air.

This project focuses on the study of interaction of water and 193 nm photoresist materials. Contact time of photoresist with ultra-pure water was varied in order to determine the impact water has on the imaging performance. Test exposures were carried out on the RIT's 193 nm 1.05NA projection immersion microstepper. Quantitative results such as sidewall angle, post-exposure delay sensitivity and image quality were compared. With these results, an optimum process for the immersion lithography at 193nm can be engineered here at RIT.

II. THEORY

A. Lithography

Moore’s Law states that the number of transistors per square inch would double every year, however in actuality, the number of transistors has doubled about every 18 months [4]. Photolithography is a major component to the drive of IC manufacturing and is the main factor in improving the complexity and cost of IC’s. The improvements are made through the ability of lithography to pattern smaller and yet smaller feature sizes. Since the mid-eighties, optical lithography was predicted to become obsolete within a few years. However, every time optical lithography approaches a limit, new and advanced techniques seem to prolong the life of the technology. Recently however, optical lithography has encountered several physical barriers, which have led to an immense investment in alternative techniques such as Scalpel (ebeam), EUV (extreme ultraviolet lithography [projection]) and a few others.

B. Resolution

Rayleigh equation governs the minimum feature that can be printed using an optical lithography system:

\[ R = k_1 \lambda / NA , \]

where,

\[ R = \text{resolution} \]
\[ k_1 = \text{resolution factor} \]
\[ \lambda = \text{wavelength of exposing radiation} \]
\[ NA = \text{numerical aperture of the system} \]
As the resolution of minimum features have shrunk, the wavelength of the exposing wavelength has also shrunk. A table below shows the gradual decrease of feature width (CD – critical dimension) as well as the decrease in wavelength used as a function of years.

C. Wavelength Requirements

<table>
<thead>
<tr>
<th>Year</th>
<th>Linewidth (nm)</th>
<th>Wavelength (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1986</td>
<td>1200</td>
<td>436 g-line mercury lamp</td>
</tr>
<tr>
<td>1988</td>
<td>800</td>
<td>436/365</td>
</tr>
<tr>
<td>1991</td>
<td>500</td>
<td>365 i-line mercury lamp</td>
</tr>
<tr>
<td>1994</td>
<td>350</td>
<td>365/248</td>
</tr>
<tr>
<td>1997</td>
<td>250</td>
<td>248 KrF excimer laser</td>
</tr>
<tr>
<td>1999</td>
<td>180</td>
<td>248</td>
</tr>
<tr>
<td>2001</td>
<td>130</td>
<td>248</td>
</tr>
<tr>
<td>2003</td>
<td>90</td>
<td>248/193</td>
</tr>
<tr>
<td>2005</td>
<td>65</td>
<td>193 ArF excimer laser</td>
</tr>
<tr>
<td>2007</td>
<td>45</td>
<td>193/157</td>
</tr>
</tbody>
</table>

Table 1: Minimum Linewidths in IC processing since 1986 [1]

Below 193nm wavelength is the 157 nm Fluorine (F2) excimer laser which faces great challenges. (This is due to the fact that at this wavelength the optical exposure systems have to switch over to reflective optics due to high levels of absorption in the refractive lens. Mention other challenges)

Along with the shortening of wavelengths, improvements in lens design have led to the increase in NA (numerical aperture) of the exposure systems lens. The gradual increase of NA (max 1.0 in air) values has given lithographers the ability to produce features of higher resolution.

The last factor in Rayleigh equation is the k1 value. This value contains the variables in the photolithographic process such as resist quality, thermal bakes and resolution enhancement techniques, also known as RET, such as phase shift masks and off-axis illumination. The values of k1 have been decreasing over the last twenty years. The practical lower limit for k1 is thought to be ~0.25. Hence the trends to achieving smaller features or better resolution are as follows: decrease λ, increase NA and maximize k1.

D. Immersion (H2O)

Having introduced the art of microlithography and its gradual development in IC processing from the mid-eighties, companies are looking into a technology which is being considered the ‘next generation lithography’ [2]. *Immersion lithography*, which involves altering the medium at which exposure takes place, has lithographers grabbing the closest cup of water. Ernst Abbe first discovered in the 1870’s that the maximum ray slope entering a lens, could be increased by a factor equal to the refractive index of the imaging media [2]. Abbe used oils between his microscope objective and the cover glass with refractive indices close to that of glass to increase the resolution of the images that were produced by the scope. The concept was simple yet revolutionary, by matching the refractive indexes of the mediums he prevented the interference effects on the image. The first application of this ‘new technology’ came in the field of medical research where Carl Zeiss and Abbe developed oil immersion systems through the used of oils that match the refractive index of glass (~1.500).

Previous optical exposure systems had a physical limitation to NA (NA =1.0) due to the medium of air (n=1.0003) in between the lens and the wafer. Numerical aperture is determined by the acceptance angle of the lens and the index of refraction of the medium surrounding the lens [1]. By altering surrounding medium, hence the refractive index of the medium, a larger value of NA can be achieved. However, this will involve the ‘new’ medium having a refractive index greater than 1.0, have low absorption at 193nm, be compatible with the photoresist and lens material and most importantly have non-contaminating qualities. Another vital requirement is an objective lens that allows for larger ray angles and allows the angles to interface with the immersion fluid. The most frequently used form of immersion lens is a hemispherical lens or prism [2].

Surprisingly, ultra-pure water (H2O) may be the magic solution to be used as the immersion fluid. Water has absorption values below 0.50 cm⁻¹ at 185nm and below 0.05 cm⁻¹ at 193nm. In other words, at 193nm wavelength the absorption is below 5% at working distances of up to 6mm [1]. The refractive index of water is 1.437 which will effectively decrease the wavelength to 134nm and also increase the NA of the imaging system to 1.437*NA. This enhancement will result in a potential 43% improvement, which is twice that of going from 248nm to 193nm, 193nm to 157nm or 157nm to 126nm exposure wavelengths without immersion technology [2]. As the NA nears 1.44, resolution enhancement to 35nm is theoretically plausible.
E. Challenges

Below is a table comparing the challenges for lithography at UV/DUV/EUV optical wavelengths and the solutions of such challenges using immersion lithography at 193nm.

<table>
<thead>
<tr>
<th>UV/DUV/EUV</th>
<th>IL @ 193nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>UV resists release great volumes of dissociated nitrogen upon exposure</td>
<td>193nm resist platforms release relatively low volumes of gas upon exposure</td>
</tr>
<tr>
<td>High index fluids tend to react with photoresist</td>
<td>Reaction of water with 193nm photoresist is minimal and can be reduced through modification</td>
</tr>
<tr>
<td>Standard immersion fluids are not transparent below 300nm</td>
<td>Water is transparent below 0.05cm^2 @ 193nm</td>
</tr>
<tr>
<td>Wafer handling processes of fluid wetting, cleaning and drying</td>
<td>Water is an existing component of wafer processing</td>
</tr>
</tbody>
</table>

Table 2: Challenges of UV/DUV/EUV lithography vs. IL @ 193nm

There are number of challenges yet to face with immersion lithography. Several prototypes have been developed to help measure the important parameters that must be taken into consideration. One of the fundamental issues is the compatibility of water with conventional lithography components. Also, in order to achieve high throughput, the stage must move from field to field quickly as possible and maintain a bubble free liquid between the lens and the wafer. There have been several approaches that have been developed to tackle this problem. The most probable to be used is a technique that involves a nozzle that will disperse a ‘puddle’ of water under the lens in between the wafer and the objective. Another issue will be maintaining the temperature of the system environment, which may affect the refractive index and hence the image resolution. The challenge will be to maintain the temperature when the stage is moving rapidly and a pulsed laser passes through the system [1].

Overall, there are still a number of issues and challenges that still need to be resolved in immersion lithography technology. The main challenges include the overall imaging capabilities, fluid properties of water (micro-bubbles) and the interaction between water and photoresist. The study of interaction between water and 193nm photoresist will be the focus of this paper.

III. EXPERIMENT

The objective of the project was to determine the interaction of water with photoresist in 193nm Immersion Lithography. In order to simulate the contact of water with the photoresist before exposure, coated wafers were soaked in ultra-pure water for different intervals. Intervals were: 1min, 2min, 4min, 8min, 16min, 32min and 64min. These times were chosen to accommodate a wide range of soak times from 1min to over an hour.

The film stack used in this experiment is as follows:
- BARC: Shipley AR40-800
  - 1230rpm, t=826Å
  - PAB: 215°C ~60sec
- Photoresist: Shipley XP 1020B
  - 1090rpm, t=1500Å
  - PAB: 120°C ~60sec
  - PEB: 120°C ~90sec
- Developer: CD-26

[All wafers were processed on the Brewer Science Stand-Alone Developer/Coater Equipment]

After the soak in water, the wafers were dried off and exposed on the EXITECH system. Using a binary mask at 0.7s, 100µm fields were exposed on the wafer. The mask consists of lines and spaces ranging from 80nm~300nm (80nm, 100nm, 120nm, 140nm, 160nm, 180nm, 200nm, 250nm and 300nm) with each set having 9 lines and spaces. All the wafers (8 intervals) were exposed with a FEM (Focus Exposure Matrix) of 21x17 with the focus varying from 5~7µm (inc. 0.1µm) and dose varying from 8~12mJ/cm^2 (inc. 0.25mJ/cm^2).

![Figure 2: 100µm field exposed on the EXITECH tool](image)

Using an optical microscope, the dies with the optimum focus and dose were recorded for further SEM work. Using the recorded values as a guideline, SEM work was done in order to obtain images of 80nm, 100nm and 120nm lines and spaces. The results were compared and contrasted to detect any trends that may occur due to the soak in water prior to exposure. Line Edge Roughness (LER), leaching effects, T-topping and any
signs of contamination were investigated.

The analysis of results was very qualitative in this experiment. The quality of lines and spaces of three different sizes at different soak times were studied. By detecting any kind of pattern due to the soaking will help identify any effects of the water on the immersion photoresist.

IV. RESULTS AND ANALYSIS

SEM results were obtained using the AMRAY SEM at Rochester Institute of Technology. With considerations to the dose uniformity of the fields, the images were captured at the same exact locations for each die in order to achieve consistency in the results. Optically, the best focus range was, 5.7~6.1μm and the best dose range was, 8~10.5mJ/cm². Using this data, dies at these locations were imaged and observed. Again, 80nm, 100nm and 120nm lines and spaces were photographed and the results were compared. Here are the results:

Compared to the baseline, the 1 min soaked wafer produced lines and space of 100nm very well. There is definite evidence of an increase in LER and a trend may be forming.

At 2min soak, the increase in LER is more and more evident. There are evidences of some micro-bridging which refers to lines that form a bridge over a space separating them. This is normally due to an excess of T-topping (amine contamination causing the top of lines to form a 'hat' or a crust which looks like the letter T from a cross-sectional view) and contamination. 120nm lines and spaces are extremely straight and have very low LER. The 100nm lines and spaces do not compare perfectly with the baseline thus adding to a possible trend of increasing LER due to the soak in water.
Above is a SEM image of the 4mm soaked wafer. Here, it is clear that the 100nm lines and spaces compare very closely to the baseline wafer. The LER is extremely low and there are no signs of T-topping or micro-bridging. At this point, it was possible to make the observation that the water has minimal effects on the quality of imaging. However, at a short 4min soak, it was inadequate data to make any strong conclusions on the effects of water. The trend of increasing LER due to the water soak had to be further verified by studying longer soak times. Images at 8min, 16min and 32min had similar qualities to images taken previously. However, the most important result was the 64min soaked wafer. After a long soak of over an hour in H2O, poor image quality was expected. SEM images were taken at the exact same location as the other soak times and the results were phenomenal. The SEM image below shows the quality of the image is extremely high contrast and no signs of degradation are evident.

V. CONCLUSIONS

After initial analysis of results, it was possible to conclude that good imaging of 100nm lines and spaces can be achieved for different soak times up to 4 min past one hour. Further soaking results were not obtained in this project. The ability to resolve 100nm lines and spaces after a whole hour of soaking in water prior to exposure is a great result. This range of soak time covered any amount of time the water may be in contact with the photoresist prior to exposure. Although the EXITECH system is not ready to expose the entire wafer (6" or 8"), the hour simulation of water to photoresist contact should have simulated any possible prolonged contact.

These results are very beneficial to any further work with the EXITECH system since it has verified imaging capability for up to an hour of water contact with photoresist. However, the results obtained here in this project are only qualitative results. Possible works include chemical analysis of the water after certain soak times. This kind of analysis will help determine if any of the chemicals from the photoresist such as PAG (Photo Acid Generator) has leached into the water. If such results can be obtained, then the percentage of PAG loss during soaks can be determined and calculated. These kinds of effects may result in alterations in the properties of water, which is critical in Immersion Lithography.

Also, further SEM analysis of the results can be performed in order to view cross-sectional profiles which will reveal any other effects of water. Sidewall angle decrease/increase can be used to determine the interaction between water and photoresist.

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James H. Park (DOB: June 28, 1980) Born in Rockford, Illinois into the PARK family. Started school in In-Chon, Korea and moved around many times before settling in Rochester, NY for University. Attended public schools in New Jersey and international schools in Jakarta, Indonesia (JIS) and New Delhi, India (AES). Arrived in Rochester, NY in the summer of 1999 and have been attending RIT since then. Currently working for Dr. Bruce Smith in Immersion Lithography research with the EXITECH System.
Phosphoric Acid as a High-Index Immersion Fluid

Karen R. Wolf

Abstract—A study has been performed to determine the viability of phosphoric acid as a high-index fluid for immersion lithography. The ability to image in the immersion fluid, and the compatibility of the fluid with photoresist were examined. Samples were soaked in the fluid before and after exposure in water to demonstrate no significant damage to the imaging capability of the resist. The refractive index of photoresist samples soaked in various immersion fluids was measured with a variable angle spectroscopic ellipsometer (VASE), and results did not show a significant variation from photoresist that was not soaked. Sixty-eight nanometer lines were imaged through phosphoric acid in 193nm photoresist without a topcoat layer.

Index Terms—Immersion lithography, interferometry, high-index fluid

I. INTRODUCTION

Optical lithography has played a critical role in the advancement of the semiconductor industry and is expected to take industry to at least the 65 nm node and possibly beyond [1]. Throughout the past two decades, lithography pushed the physical limits of optical lithography through three main trends: (1) reduction in exposure wavelength; (2) increase in numerical aperture (NA) of projection systems; and (3) implementation of resolution enhancement techniques such as phase shifting masks and off axis illumination leading to a reduction in the $k_1$ factor [2].

Resolution of diffraction-limited optical lithography is generally defined by the Rayleigh criteria

$$R = k_1 \lambda / NA,$$

where $R$ is the minimum dimension, or pitch, that can be printed, $k_1$ is the process dependent resolution factor, $\lambda$ is the exposure wavelength, and NA is the numerical aperture of the projection lens. The resolution factor, $k_1$, is typically between 0.6 and 0.8, and is dependent on the process used for exposure. The NA value is dependent on the optical system and is defined as $n \sin \Theta_0$, where $\Theta_0$ is the angle of acceptance of the lens, and $n$ is the refractive index of the medium surrounding the lens. For typical optical lithography, the medium surrounding the lens is air. Therefore, the maximum NA achievable is 1.00, since the refractive index of air is 1.00 [2].

Historically, significant improvements in resolution have been the result of shrinking exposure wavelength. Another method to achieve smaller resolutions is to increase the refractive index between the lens and the photosensitive substrate. One way this has been accomplished is to place a liquid with a high refractive index between the projection lens and the photoresist during exposure. This technique is referred to as immersion lithography. The resulting resolution enhancements can be quantified by an increase in NA of the system. However, NA is not the only factor affected. The system can also be modeled by scaling the exposure wavelength to the effective wavelength in the given medium. This wavelength, $\lambda_{eff}$, is equivalent to $\lambda_0/n_1$, where $\lambda_0$ is the wavelength in vacuum, and $n_1$ is the refractive index of the immersion medium. As the fluid refractive index increases, the minimum pitch that can be imaged will decrease, as defined by Equation 2 [3].

$$R = \frac{k_1 \lambda_{eff}}{\sin \Theta_0}$$

Through the increase in index between the projection lens and the photoresist, the depth of focus (DOF) also improves, as illustrated in Figure 1.

There are many aspects to consider when imaging with an immersion system. The immersion fluid of choice must be compatible with the photoresist to be used, and must have a high refractive index at the wavelength of interest. In addition, polarization, bubbles, and the absorption spectra of the immersion fluid can affect immersion imaging [3].

Water is a common immersion fluid because of its high refractive index (1.44 at 193nm), and compatibility with lithography systems and resist. However, other high-index fluid options are being studied. A viable immersion fluid for 193 nm lithography needs an absorption peak below 193 nm, and a high refractive index at that wavelength. This project explores the photoresist compatibility and imaging capability of phosphoric acid ($H_3PO_4$) in water as an immersion fluid. The absorption peak of the hydrogen phosphate in solution is at a
wavelength of 170 nm, and the refractive index of the 85% (by weight) phosphoric acid in water is 1.54 at 193 nm. Thus, phosphoric acid is a viable candidate for high-index immersion lithography at 193 nm.

Fig. 1. Image intensity in resist shows increased depth of focus for increased refractive index of the immersion medium. Left: exposed in air (n=1.0003). Center: exposed in water (n=1.437). Right: exposed in 85% phosphoric acid solution (n=1.54).

Fig. 2. Left: Immersion lithography using a flat plate. Right: Immersion lithography using a half ball.

II. EXPERIMENTATION AND RESULTS

A simple and effective way to implement immersion lithography is with an interferometric system (Figure 4). Interferometric lithography offers high contrast over a large range of spatial frequencies, and is well suited for the study of alternate immersion fluids [4].

Interferometric lithography utilizes two mutually coherent beams of wavelength \( \lambda \) that are incident on a photosensitive substrate. Their wave vectors are coplanar and each make an angle \( \Theta \) with respect to the normal to the substrate, as shown in Fig. 3. Interference of the two plane waves produces a sinusoidal intensity pattern, with period \( \Lambda \) given by Equation 3 [4].

\[
\Lambda = \frac{\lambda}{2 \sin \Theta}
\]  

As \( \Theta \) approaches 90°, \( \lambda \) approaches the limiting value of \( \pi/2 \), which corresponds to the highest spatial frequency that is theoretically achievable with freely propagating light beams of a given wavelength in air. For light propagating through an optically dense medium, a finer grating is formed with a period

\[
\Lambda = \frac{\lambda}{2n_i \sin \Theta}
\]  

The high index fluid is placed between a quartz piece and the substrate in order implement immersion lithography on the interferometric system. However, for an immersion interference system, the NA advantage is only possible if the two interfering beams enter normal to the quartz surface, as shown in Figure 2. Thus, a "half-ball" or a prism must be used to realize the advantages of immersion imaging. In a flat plate setup, shown in Figure 2, the immersion advantages cancel out, and there is no image improvement observed. To demonstrate the ability to image through the fluid, this project utilizes a flat plate. Thus, the pitch imaged in the resist will be defined by the limits of the interference system without an advantage due to the high refractive index of the fluid.

Five samples were exposed in Ultra Pure Water under various conditions using an ArF 193nm excimer laser coupled with the interferometric system. The five conditions are as follows:

1) Soaked 60 seconds in \( \text{H}_3\text{PO}_4 \) (47% solution) and rinsed 30 seconds in \( \text{H}_2\text{O} \) before exposure
2) Soaked 90 seconds in \( \text{H}_2\text{O} \) before exposure
3) Soaked 60 seconds in \( \text{H}_3\text{PO}_4 \) (47% solution) and rinsed 30 seconds in \( \text{H}_2\text{O} \) after exposure
4) Soaked 90 seconds in \( \text{H}_2\text{O} \) after exposure
5) Not soaked before or after exposure.
Images collected from these samples, shown in Figure 6, demonstrate imaging in photoresist soaked in 47% by weight phosphoric acid in water. Resist scumming is observed on samples soaked in the acid. However, this may be the result of an insufficient exposure dose.

A second set of samples was then exposed in the phosphoric acid solution instead of water. These samples were not soaked before or after exposure. The first of the samples was exposed in the 47% phosphoric acid solution, and the second was exposed in 85% solution. Sixty-eight nanometer lines were imaged in each case in resist without a top-coat layer.

Finally, a variable angle spectroscopic ellipsometer (VASE) was used to explore effects of the fluid on the photoresist. The refractive indexes of the following three resist samples were measured:

1) Unexposed resist soaked in water for 90 seconds  
2) Unexposed resist soaked in phosphoric acid (85%) for 60 seconds and rinsed in water for 30 seconds  
3) Unexposed resist (not soaked)

The results were analyzed using Wollen VASE (WVASE) software to fit the collected data using a Lorentz model. Table I shows the resist refractive indexes measured. No significant difference is observed between the samples soaked in water and in the phosphoric acid solution.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Resist Refractive Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>No soak</td>
<td>1.70</td>
</tr>
<tr>
<td>Water soak</td>
<td>1.71</td>
</tr>
<tr>
<td>Phosphoric acid (85%) soak</td>
<td>1.71</td>
</tr>
</tbody>
</table>

### III. DISCUSSION AND CONCLUSIONS

Phosphoric acid did not destroy the photoresist used in the experiment. The samples soaked in acid, illustrate some scumming compared to the water soaked samples. However, this is a result of the exposure conditions rather than a damaged photoresist. Samples soaked or exposed in phosphoric acid required approximately twice the dose to clear as samples exposed only to water. This implies that the absorbance of phosphoric acid in solution is approximately twice as much as that of water at a wavelength of 193nm.

The samples exposed in phosphoric acid illustrated the ability to image through both 47% and 85% phosphoric acid solution using an ArF excimer laser. Sixty-eight nanometer lines and spaces were imaged in the Shipley resist with no signs of T-topping.

The ellipsometer data collected shows negligible variation between the resist samples soaked in the immersion fluids. As shown in Table I, the refractive index of the samples soaked in the immersion fluid was slightly higher than the sample not soaked in fluid. This indicates a possible change in the properties at the surface of the photoresist. However, the full effects of the fluid on the resist cannot be determined through this measurement alone.

Phosphoric acid is a viable high-index fluid candidate for immersion lithography. The acid has not demonstrated significant damage to the resist properties, and imaging through the fluid has been achieved. Further work must be completed to determine the full effect of the immersion fluid on photoresist.

### APPENDIX

#### A. Sample Preparation

To carry out the experiment, five four-inch wafers were coated with a Shipley bottom anti-reflective coating or BARC, and Shipley 193nm photoresist using the process below.

1) Spin on Shipley AR-40 BARC   
   a. Spin speed = 2300 RPM   
   b. Post Apply Bake (PAB) = 215°C, 60 sec.

2) Spin on Shipley XP1020 193nm photoresist   
   a. Spin speed = 3500 RPM
b. \[ \text{PAB} = 120^\circ \text{C}, 90 \text{ sec.} \]

Samples were then exposed according to the conditions described. Post exposure bake was set at \(120^\circ \text{C}\) for 60 seconds. Then, samples were developed in CD-26 developer for 60 seconds, rinsed 30 seconds in water, and blown dry with a nitrogen gun.

In preparation for SEM pictures, each sample was cleaved and sputtered with gold. Images were collected on an Amray SEM.

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**REFERENCES**


Karen R. Wolf, originally from Binghamton, NY, received a B.S. degree in Microelectronic Engineering from the Rochester Institute of Technology in 2004. She obtained co-op work experience at Micron Technology in Manassas, VA.
Quadrupole Illumination Design for a 193nm Hyper-NA Exitech Immersion Stepper

Derek J. Summers

Abstract — As device sizes reduce in size and processes become more complex, enhancement techniques for optical lithography are essential. Several ways to enhance the current lithographic systems include immersion lithography, phase-shifting masks, optical proximity correction and OAT (off-axis illumination). Depending on the process, these RETs (resolution enhancement techniques) may be used individually or in combination to compensate for image degradation caused by optical diffraction and resist behavior.

The purpose of this project is to design and test a quadrupole off-axis illumination aperture for the 193 nm Immersion stepper at RIT. Process window simulations, using Prolith, were used to determine theoretical effectiveness and benefits for off-axis illumination conditions. The targeted features of 100 nm and 80 nm respectively, each with a duty ratio of (1:1), were processed and compared to simulations. Improvements in terms of (DOF) Depth of Focus and resolution, have been demonstrated for 100 nm and 80 nm features. Off-Axis Illumination and Liquid Immersion are cost effective techniques to extend the lifetime of optical lithography.

Index Terms— Resolution Enhancement Techniques; Off-Axis Illumination; quadrupole; immersion; aperture design

I. INTRODUCTION

When exploring the theory behind lithographic imaging systems it is important to understand the factors that influence them including the illumination wavelength (?), numerical aperture (NA), coherence factor (s) and method of illumination. These factors will be defined by presenting the components of the lithographic system that will be used for this research, the Exitech 193nm Immersion system. This will be followed by a theoretical discussion on the implementation of a quadrupole aperture into the system as a resolution enhancement technique. The quadrupole aperture can be inserted into the optical column between the radiation source and the condenser lens.

![Diagram](image)

Figure 1 Illustration of lithographic system depicting main components of the EXITECH 193nm system.

The source for the EXITECH system is an Argon Fluoride (ArF) laser designed to a wavelength of 193nm. Following the source, a condenser lens sufficiently distributes the energy to illuminate the reticle.

The reticle is the next component in this optical system following the condenser lens. The reticle is the optical tool, which provides the pattern or “information” that is to be recreated on the wafer in the resist. After the light passes through the lines and spaces on the mask the resulting “patterned” light is to be collected by the objective lens. Then the “patterned” light is often reduced by four to five times the original size by the specific combination of lenses in the optical column. The Exitech Immersion stepper has a 90X reduction factor. This means that a 100nm feature on the wafer was printed with a 9000nm or 9μm feature on the reticle. In order to ensure that the latent image captured by the resist is sufficiently close to the intended design on the reticle, the objective lens must be able to capture a sufficient amount of information namely the $\theta$ and some of the $\pm 1^\circ$ diffraction orders. A more thorough understanding of this will be presented later in this paper when discussing the benefits of off-axis illumination on the basis of diffraction theory.
This optical system is based upon the theory of Köhler illumination. This theory demonstrates a system by which an image of the source is created at the entrance pupil of the objective lens by the means of the condenser lens. In this system the resulting image is then projected through the reduction optics to a focal plane near the level of the resist. The theory of diffraction must be discussed in order to understand how this system is used in conjunction with a reticle to produce a latent image in the resist.

As light is passed through the lines and spaces on the reticle, diffraction occurs spreading the light into orders of magnitude in reference to an optical axis (OA). These different orders of magnitude correspond to an electric field distribution modeled in increments of \( \pm \lambda / p \), which is defined as the wavelength of the source divided by the pitch of the feature (nominal critical dimension of a line plus a space). As previously mentioned, enough information must be collected by the objective lens to propagate the image to the resist.

![Conventional Illumination](image)

**Figure 2.** Conventional point source illumination illustrating diffraction.

The 0th diffraction order supplies intensity, whereas the \( \pm 1^{st} \) diffraction orders provide the feature and pitch information to transfer to the resist. Typically, the 0th and at least some of the \( \pm 1^{st} \) diffraction orders must be collected by the objective lens to propagate an image of acceptable quality. The following image illustrates the diffraction orders and the electric field distribution quantified in relation to the numerical aperture of the objective lens.

![Off-Axis Illumination](image)

**Fig. 3.** Illustration demonstrating Off-axis illumination

The amount of possible information that can be collected by the objective lens is a function of its numerical aperture. The NA is derived from the usable diameter of the objective lens, the distance from the reticle to the objective lens, and the refractive index of the media in which the light travels in that distance. The following is the resulting theoretical equation for numerical aperture.

\[
NA = n \sin(\theta)
\]  

(1)

The NA for the EXITECH system is 1.05. Numerical apertures that now have the capability of NA greater than 1 are so called “Hyper-NA”. Though it is true that building a larger usable objective lens increases NA, benefits must outweigh the cost and feasibility.

The theoretical resolution and DOF is limited by the NA and wavelength of the system.

\[
R = \frac{0.5\lambda}{NA}
\]  

(2)

\[
DOF = \pm k_2 \frac{\lambda}{NA^2}
\]  

(3)

A problem arises from this theoretical equation, due to a theory of diffraction limitation. The ability to propagate a “patterned” image to the objective lens is diminished as feature sizes on the reticle shrink. As feature sizes on the reticle shrink, the diffraction orders spread out to the extent where the objective lens only captures the 0th diffraction order. Again, at least some of the \( \pm 1^{st} \) diffraction orders must be captured to propagate the image as intended per the design. Therefore, there has been much research into Resolution Enhancement Techniques to reduce the diffraction effects and effectively allow a “sufficient” amount of energy for capture by the objective lens. Off-axis illumination is a well known RET used to adjust the diffraction pattern produced by the reticle. The following image illustrates the shift of diffraction orders.
By the means of changing the single point source illumination to two or several point sources “off-axis” in theory can provide enough of the 1st diffraction orders to the objective lens to sufficiently propagate the intended reticle design. The 1st diffraction orders overlap with the 0th diffraction order as illustrated in Figure 3. Note that the ±1st diffraction orders fall well within the limits of the objective lens at ±π/2p instead of ±π/p for on-axis illumination. When there are more than two point sources used in OAI, each of the resulting diffraction orders will be spread according to their orientation with the optical axis. What will be discussed further on is that depending on the targeted feature orientation may need to be taken into account when considering OAI. Once OAI is implemented the light is no longer coherent, but is partially coherent. The following equation relies upon on the numerical aperture of the condenser lens (NAc) and the numerical aperture of the objective lens (NAo).

$$\sigma = \frac{NAc}{NAo}$$ (4)

With standard illumination conditions the partial coherence for the EXITECH system can be adjusted from 0.3 to 0.7. The conventional standard condition is a partial coherence value of 0.7. The system achieves this by blocking off specific amount of radiation with the specified aperture. Each aperture corresponds to a specified coherence value based upon the set NA of the EXITECH system.

Based on the previously mentioned EXITECH system parameters and theories of OAI, the following will be a discussion of combining partial coherence and OAI to increase resolution capabilities. As previously mentioned, OAI orientation design will depend on targeted feature include critical dimension and pitch. Previous work has been completed on the design of slot pole apertures for the ASML 248nm system. However, there are known limitations to the design most important are isolated feature degradation and the ability to optimize imaging only in one direction. The investigation of this research will evaluate the efficiency of an OAI orientation design, which is capable of resolution enhancement, and depth of focus improvements regardless of x/y orientation of features. Depth of Focus can be defined as the distance along focal plane that still produces an image of acceptable quality. The OAI technique that is capable of such results is quadrupole illumination.

II. Quadrupole Illumination Design

In order to determine the correct sigma values for the quadrupole illumination, the system parameters and governing equations for OAI will be utilized. The requirements for quadrupole illumination can be further realized by understanding the governing relationships to improve the imaging of a feature with several duty ratios. The duty ratio of a feature is defined as the ratio of line critical dimension to space critical dimension. For example, a duty ratio of (1:1) corresponds to a feature with an equal line and space critical dimension. Furthermore, an 80 nm feature with a duty ratio of (1:3) has a pitch of 320 nm, where pitch is defined as the sum of a line and accompanying space critical dimension. The following illustration depicts the frequency plane of the objective lens and demonstrates the relationship that the pole positions have with a specific pitch, numerical aperture, and exposing wavelength.

![Quadrupole Illumination Theoretical Sigma Values](image)

This illustration specifically points out the definition of the quad center sigma value and the pole or radius sigma value again in relation to the frequency plane of the objective lens. Each sigma value is relative to the grey area which is a full $\sigma = 1$. The following equations govern the placement of the poles based on the pitch, numerical aperture and exposing wavelength.

$$Axis \sigma_c = \frac{\lambda}{2p(NA)}$$ (5)

$$Quad \sigma_c = \frac{\lambda}{\sqrt{2}p(NA)}$$ (6)

For this research, 100 nm and 80 nm features were targeted for imaging with an objective lens numerical aperture of 1.05 and an exposing wavelength of 193 nm. The following table is a summary of the design results for 80 nm features ranging in duty ratios from 1:1 to 1:6. It should be noted that the pole positions with respect to the optical axis spread out as the duty ratio approaches 1:1.

<table>
<thead>
<tr>
<th>Duty</th>
<th>Pitch (nm)</th>
<th>Axis Sigma</th>
<th>Quad Sigma</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:1</td>
<td>160</td>
<td>0.57</td>
<td>0.812</td>
</tr>
<tr>
<td>1:1.5</td>
<td>200</td>
<td>0.46</td>
<td>0.650</td>
</tr>
<tr>
<td>1:2</td>
<td>240</td>
<td>0.38</td>
<td>0.542</td>
</tr>
<tr>
<td>1:2.5</td>
<td>280</td>
<td>0.33</td>
<td>0.464</td>
</tr>
<tr>
<td>1:3</td>
<td>320</td>
<td>0.29</td>
<td>0.406</td>
</tr>
<tr>
<td>1:3.5</td>
<td>360</td>
<td>0.26</td>
<td>0.361</td>
</tr>
<tr>
<td>1:4</td>
<td>400</td>
<td>0.23</td>
<td>0.325</td>
</tr>
</tbody>
</table>
In order to improve the resolution and depth of focus for the entire range of duty ratios there needs to be a certain amount of overlap for duty ratio. To achieve this the quad center sigma and the radius sigma are determined by the following relationships:

\[
\sigma_c = \sqrt{2} (\text{Axis Sigma}_{\text{max}} - \text{Axis Sigma}_{\text{min}}) \quad (7)
\]

\[
\sigma_r \geq (\text{Axis Sigma}_{\text{max}} - \text{Axis Sigma}_{\text{min}}) / 2 \quad (8)
\]

The summary of the results for 80 nm features for optimized quad center sigma and radius sigma values are included in the following table.

<table>
<thead>
<tr>
<th>Pitch Range</th>
<th>Quad Sigma</th>
<th>Sigma Radius</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:1 - 1:3</td>
<td>0.61</td>
<td>0.14</td>
</tr>
<tr>
<td>1:1 - 1:6</td>
<td>0.52</td>
<td>0.21</td>
</tr>
</tbody>
</table>

Table 2. Summary of center sigma values for 80 nm features for range of duty ratios.

Based on this data the quadrupole illumination design to accommodate 80 nm features with a range of duty ratios from 1:1 to 1:3 would have a corresponding quad center sigma of 0.61 and a radius sigma of 0.15. The radius sigma value must have a minimum value to assure a sufficient overlap of pole position for each duty ratio.

For this research two quadrupole illumination aperture designs are fabricated for experimentation purposes. Each design is optimized for 80 nm and 100 nm features respectively, each with a duty ratio of (1:1). The resulting designs are summarized in the following table.

<table>
<thead>
<tr>
<th>Target Feature</th>
<th>Quad Sigma</th>
<th>Sigma Radius</th>
</tr>
</thead>
<tbody>
<tr>
<td>80 nm (1:1)</td>
<td>0.812</td>
<td>0.15</td>
</tr>
<tr>
<td>100 nm (1:1)</td>
<td>0.65</td>
<td>0.15</td>
</tr>
</tbody>
</table>

Table 3. Summary of center sigma values for 80 nm features for (1:1)

An increase in the radius sigma values for the quadrupole illumination translates to more light to pass resulting in greater intensity at the resist level. When compared to the conventional illumination the intensity of radiation is reduced which then requires a higher dose to clear the image on the resist and could translate to a lower contrast in the final image. Radius sigma values were chosen as to balance the benefits of the off-axis illumination with the loss of intensity.

Prolith can modify the illumination of a lithographic system and simulate the theoretical results. Figure 5 is an example of how prolith can be used to simulate the enhancement of off-axis illumination over conventional illumination. Although this is strictly a theoretical plot using ideal resist models and does not take into account aberrations in the lens, there is evidence of an increased depth of focus for quadrupole illumination over conventional on-axis illumination.

In order to use the Shipley BARC AR40 (bottom antireflective coating) to suppress standing waves and a novel Shipley resist 1020C. All processes were developed based upon Shipley recommendations. A VASE or variable angle spectroscopic ellipsometer was used to dial in the correct thicknesses for the BARC and resist accordingly. The BARC AR40 was coated to 80 nm (30 sec @ 1230 rpm) with a Post Applied Bake (PAB) for 60 seconds @ 215°C. The 1020C resist was coated to a thickness of 150 nm (30 sec @ 1190 rpm) and a PAB for 90 seconds @ 120°C. Although contamination can be an issue for this resist no top-coat was used for this experiment and the Post Exposure Bake was for 60 seconds at 120°C.

III. Fabrication of the Aperture

The partial coherence aperture for the EXITECH stepper was accessible and made it possible to fabricate a quadrupole aperture for experimentation purposes. The apertures have been fabricated from aluminum stock in a metal fabrication
facility at the Rochester Institute of Technology. From the theoretical sigma values and given system dimensions a schematic drawing was completed for each aperture design. The metal fabrication tools required to complete the apertures included a band saw, lathe, and drill press.

From the aluminum stock the aperture height was cut to the appropriate sizes. Each face of the aperture was cut and polished using the lathe. The lathe was used to bore out unnecessary material from the aperture. The drill press was used to cut the appropriate sigma values into the aperture. Each aperture was then individually inspected for defects from the fabrication process and fine alignment marks on the apertures for future alignment to the optical column. Each aperture was cleaned with specific cleaning solutions and residual organic materials were removed in preparation of insertion into the Exitech Immersion stepper. The following is and image of a completed quadrupole illumination aperture.

![Fig. 6. Finished quadrupole illumination aperture](image)

By utilizing this form of off-axis illumination the resolution limits can be tested for the given imaging system. The benefits of depth of focus and resolution enhancement are realized with the exposure results of the completed quadrupole illumination system. A summary and review of the exposure results will be presented in the following section. According to theory and the following experimental results, DOF and resolution enhancements are be realized for a completed quadrupole illumination system.

IV. EXPOSURE RESULTS

The exposure results from using the 80 nm quadrupole aperture is presented in this section. There was a significant improvement in the resolution of 80 nm lines and spaces (1:1). Resolution was also improved for the 100 nm line and space (1:1) feature and depth of focus seemed to have been improved for both feature sizes. The following SEM images illustrate the results of the experiment and provide a good representation as to the benefit of off-axis illumination.

The results of the exposure were promising especially considering there was no top-coat used for the experiment. As mentioned earlier a top-coat can be used as a protecting layer to the resist. Resist used at Deep Ultraviolet wavelength such as 248 nm and below can be susceptible to amine contamination. The amine contamination can produce a neutralized layer on the surface of the resist, which can cause the resist to become readily insoluble to the developer. In certain cases a resist feature deformity known as T-topping can occur. Even though no top-coat was used for this experiment there was no serious contamination issues present.

These cross-sectional SEM images captured by International SEMATECH demonstrate good exposure latitude performance for both 100 nm and 80 nm features with duty ratios of (1:1). The following SEM images also from SEMATECH illustrate a similar performance through focus, demonstrating the DOF for this experiment.

![Exposure Latitude](image)

![Depth of Focus](image)

The 80 nm features imaged consistently and clearly with
good aspect ratio the resist thickness was 150 nm therefore the aspect ratio was almost 2:1 (height/width). The results were encouraging with the fact that with conventional illumination of a on-axis partial coherence value of 0.7 the minimum sufficient resolved feature was a 100 nm (1:1). The research project was successful in relation to its given objective to use quadrupole illumination which coupled the benefits of off-axis illumination and immersion lithography to allow sub-100 nm imaging on the 193 nm Hyper-NA Exitech Immersion stepper at the Rochester Institute of Technology.
V. CONCLUSION and Future Research

The efficiency and benefits of off-axis illumination has been successfully demonstrated. Quadrupole apertures were designed based on the off-axis illumination theory discussed. Each design was fabricated at the Rochester Institute of Technology using materials and tools in house. A process was developed to run an experiment with the completed illumination system. The results were illustrated and summarized and the objectives of the research project were met. Sub-100 nm imaging was allowed on the 193 nm Hyper-NA Exitech Immersion stepper at the Rochester Institute of Technology due to a quadrupole illumination system that coupled the benefits of off-axis illumination and immersion lithography.

Further work can be completed including the optimization of further resist processes as well as alternative off-axis illumination systems including dipole. Dipole illumination has the capability to improve resolution beyond quadrupole, however only for features oriented in one direction. In response dipole and annular should both be investigated. The experiments to further assess these illuminations will require more test features on the mask that vary in pitch and orientation. Also, further improvement into the optical column alignment procedure can benefit from future work. Immersion lithography coupled with the correct illumination techniques is promising to extend the lifetime of optical lithography.

Acknowledgments

The following includes gratitude for the help and support received while conducting this research. Appreciation is given to Dr. Bruce Smith and Professor Dale Ewbank for advising me on my senior project. To RIT Imaging Science PhD candidate Lena Zavyalova and researcher Emil Piscani for their gracious hours spent on resist process development and exposures. To Thomas Grimsley for material support and tool access, Tom Locke for their assistance in fabricating the apertures in the machine shop. To SMFL staff Technician John Nash for advice and guidance through aperture fabrication. To Jeff Meute from SEMATECH for the cross-sectional SEM images and to Dr. Sean Rommel for support with the Leo SEM. And to my fiancé Terese Puma for her understanding and support during all the late hours spent on this research.

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Development of a Full Silicidation (FUSI) Process for Nickel Silicide

Yaser A. Alshehri

Abstract—Silicides have been long used to solve the problem of poly depletion effects in the CMOS circuits. The depletion layer in the poly-gates increases the total effective gate-dielectric thickness causing a poor device performance. Many advantages are promised in replacing the Polysilicon gates with metal gates, which include improved sheet resistance of the gates, decreased equivalent electrical thickness of gate dielectric by eliminating the Polysilicon gate depletion effect, and dual work functions, higher than n+ poly work function for NMOS and lower than p+ poly for PMOS in a single full Silicidation (FUSI) of Polysilicon gates. In the ever reducing gate dimension and junction depths, nickel Silicide has become one of the promising candidates for silicides applications in submicron CMOS devices. Nickel silicides has many advantages over other metal silicides due to its one step low temperature formation, low resistivity (14~20 $\mu\text{Scm}$), low Si consumption, and its nature of not suffering from resistivity degradation on narrow lines or gates. However, nickel silicides have some problems associated with them such as the large junction leakage current and sheet resistance degradation due to oxygen contamination and rough interface between NiSi and Si. Nickel Silicide was formed on doped Polysilicon to simulate the effects on gate CMOS regions. Sheet resistance will be measured on silicided Polysilicon and results will be introduced in this report as well.

Index terms—Ni Silicidation, full Silicidation, metal gate, RTP

1. Introduction

The Silicide process is defined by introducing metal into silicon, which has been used for a long time to overcome the high resistivity between metal and poly gates and source/drain regions in MOSFETs. Silicides are necessary in small devices that are limited in their performance by the resistance seen in source/drain and poly gates regions. Silicides are also necessary in dual gate devices because by replacing Polysilicon gate electrodes in MOSFETs with metal gates give the choice of work function allowing a higher work function than n+ poly work function for NMOS and a lower than p+ poly work function for PMOS, which would decrease the drive current loss due to mobility degradation and decrease the band to band tunneling across drain to body junction. Using metal gates offers many other advantages like lower gate resistivity, no boron penetration from Polysilicon gate into channel through very thin gate dielectrics as well as reduced electrical thickness of gate dielectric by eliminating depletion in doped Polysilicon gates. Silicides include two types in which they can be formed, the first Silicide is called Polycide process in which the Polysilicon is deposited, as well as the Silicide and both are then patterned, while in the
second process—Salicide—or better known as the self-aligned Silicide, the Polysilicon is deposited and patterned followed by a metal deposition then the Silicide is formed by thermal reaction.

There are different metals that can be used for silicides applications keeping in mind their different properties that contribute to weather the metal can be used or not, such as their Silicidation temperatures, etch capabilities, dominant diffused species, and resistivity. Some of the famous metals that have been used for silicides applications include Titanium Silicide (TiSi₂), Cobalt Silicide (CoSi₂), and Nickel Silicide (NiSi).

Titanium Silicide (TiSi₂) has been used for a long time in silicides technology, but begins to demonstrate limitations in the sub-250nm technology devices. Titanium silicides suffered from difficulties in forming the low-resistivity phase on narrow poly lines, as well as its silicon diffusion dominated formation of silicides leading to problems of bridging. Cobalt silicides (CoSi₂) has replaced titanium silicides around the 250nm technology node due to poly line-width problems associated with TiSi₂ discussed earlier and due to the fact that CoSi₂ does not suffer from narrow-line effects and bridging problems. CoSi₂ demonstrated better scalability for sub250nm nodes. However CoSi₂ started to have problems associated with it as the device dimensions are scaled down further, these problems include the difficulty associated in forming the low resistivity CoSi₂ on poly line-width less than 40nm. CoSi₂ also suffered from high sensitivity to ambient contamination as well as high consumption rate of silicon.

The nickel Silicide emerged as a prominent candidate for silicides applications for the sub-65nm advance technology devices. NiSi has many advantages over both titanium and cobalt silicides because of its low consumption rate of silicon, low resistivity reported to be in the range of 15~20 μΩcm, and most importantly no suffering from narrow-line effects. NiSi formation process can be performed in a single step annealing forming the low resistivity NiSi phase followed by a selective etch removal of the unreacted nickel. This study will investigate the properties and formation of NiSi on doped Polysilicon to simulate the effects on gate CMOS regions. NiSi polycide is formed on a blanket Polysilicon film and then the polycide’s sheet resistance is measured using the CDE Resistivity Mapper and compared to the sheet resistance of the doped poly before the Silicidation step to verify the formation of NiSi.

2. Theory

A. Nickel Silicide (NiSi) formation

The Silicidation process is usually performed by depositing some kind of metal such as tungsten, titanium, cobalt, or nickel on silicon followed by a rapid thermal reaction treatment creating a metal-semiconductor compound that have different properties depending on the processing conditions it has been through, and which have to be controlled and calibrated to get the desired end results. These conditions include the temperature at which the Silicidation step is done, surface and ambient contamination, and self-aligned Silicidation. The desired phase of nickel Silicide for this experiment was the nickel monosilicide (NiSi) which has been reported to form at temperatures around 500°C allowing for a lower thermal budget. One thing that should be kept in mind when considering the Silicidation temperature, is the distinction of nickel Silicide phase being formed. At higher temperatures of 750°C and above, another phase of nickel Silicide is formed—nickel diSilicide—(NiSi₂), which has a higher resistivity than the NiSi reported to be around 50 μΩcm² caused by silicon agglomeration in the NiSi film taking place at higher temperatures causing a serious degradation in the performance of the devices. Another important issue that must be closely monitored is the ambient contamination mainly silicon
oxides that can be grown on silicon as a native oxide or produced during the processing steps. Silicon oxides negatively affect the process of Silicidation by forming between the metal and the silicon interface allowing for a layer of SiO₂ to be formed on top of the Silicide, thus causing the formation of metal oxides and eventually preventing the Silicidation process. This problem can be overcome by depositing a capping layer on top of the Silicide right after the deposition of the Silicide to prevent any growth of native oxide and can be easily removed with the unreacted nickel after the Silicidation reaction. As for the self-aligned Silicidation in nickel Silicidation process the nickel will only react with silicon where nickel and Polysilicon are in contact and as mentioned before the unreacted nickel along with any capping layers used will be etched using a Piranha etch H₂SO₄:H₂O₂ which does not effect any silicides formed.

B. Resistivity Measurements

The sheet resistance measurements is most crucial factor due to its importance in confirming the formation of nickel Silicide NiSi and comparing them to sheet resistance measurements taking after doping the Polysilicon. The technique that was used to determine the sheet resistance of the nickel Silicide NiSi film was by using the four-point probe technique where a current is run two outer probes and measure the resulting voltage between the two inner probes as shown in figure 1. Full wafer sheet resistance measurements were made possible by using the Creative Design Engineering (CDE) Automated Resistivity Mapper.

The process was performed on 4” p-type <100> crystalline orientation silicon wafers with resistivity ranging from 1~25 Ω-cm. An RCA clean step was done to remove any contaminants. A layer of about 1000 A of oxide was then grown in the Bruce furnace using the factory recipe#350. The next step was to deposit about 2000 A of Polysilicon using the LPCVD and factory recipe#650 with a deposition rate of 200 A/min. doping of Polysilicon was done using the spin on doping method by spinning on N250 phosphorus dopant at 3000 rpm followed by a pre-bake at 200°C for about 15 minutes followed by an anneal in Bruce furnace using factory recipe#120 at 1000°C for about 15 minutes soak in N₂. Sheet resistance of the doped silicon was then measured as shown in table 1. The Polysilicon was then patterned using the CMOS Poly-gate mask and the G line lithography using the GCA 8000 with dose = 43.5 mJ/cm². A Dry etch step was done on the patterned samples using the Dry-Tech quad to etch the Polysilicon using the polyetch recipe. Resist was then stripped followed by an HF 50:1, 1 minute dip step to remove any native oxide that might have grown before the deposition of Ni followed by an SRD step. Nickel was then deposited on the samples by sputtering method using the CVC601 at a deposition rate of 1.52 A/sec with a target thickness of ~1000 A of Ni with base pressure of 1.9E-5 torr, and chamber pressure of 5.1 mtorr at 197.8 V and 0.75 A flowing Ar at 17 sccm. We also tried to evaporate Ni on some of the samples but turned out to be not a good idea to use a thermal evaporator with nickel because at different pressures the boat breaks before the Ni gets evaporated expect for one time where we were able to get a very thin layer of evaporated Ni ~400 Å. The Silicidation step was done by a thermal reaction step using the RTP AG 410 at 550°C for about 30 seconds. After the thermal reaction step, the unreacted nickel was then removed in a Piranha etch (H₂SO₄:H₂O₂ 1:2) at 100°C for about 3 minutes to remove all the unreacted Ni. The final step was to take sheet
resistance measurements on the samples using the CDE resistivity mapper.

4. Results and Discussion

Using the previously outlined process, sheet resistance on the nickel silicided NiSi samples were taken as shown in Table 1 using the CDE resistivity mapper.

<table>
<thead>
<tr>
<th>Poly Resistivity Rs Ohms/sq</th>
<th>NiSi Resistivity Rs Ohms/sq</th>
</tr>
</thead>
<tbody>
<tr>
<td>74.09</td>
<td>2.08</td>
</tr>
<tr>
<td>74.47</td>
<td>1.93</td>
</tr>
<tr>
<td>72.60</td>
<td>2.53</td>
</tr>
<tr>
<td>71.09</td>
<td>3.33</td>
</tr>
<tr>
<td>73.31</td>
<td>4.52</td>
</tr>
<tr>
<td>77.79</td>
<td>1.49</td>
</tr>
<tr>
<td>76.31</td>
<td>2.00</td>
</tr>
<tr>
<td>66.37</td>
<td>3.86</td>
</tr>
<tr>
<td>75.03</td>
<td>1.86</td>
</tr>
</tbody>
</table>

\[ \text{Ave } = 73.91 \quad \text{Ave } = 2.59 \]

The Nickel Silicide resistivity was then calculated to verify the formation on NiSi:

\[ \text{Rho} = \text{Sheet resistance} \times \text{NiSi Thickness} \]
\[ = 2.59 \times 1200 \times 10^{-8} \]
\[ = 3.11 \times 10^{-5} \text{ uOhms.cm} \]

From the previous NiSi resistivity calculation we can see that the NiSi was formed successfully and that resistivity has dropped down significantly. To further invistigate the formation of NiSi, SEM images were taken of the samples and in SEM#1 through SEM#3 we can see that there is a layer of oxide on top of silicon and another layer of NiSi on top of the oxide with a thickness of approximately 1200 A, and from the reported values of NiSi silicon consumption rates of about 1.83 A of silicon per A of metal and about 2.34 A of resulting Silicde thickness per A of metal, it appears that we have reacted about 938 A of Polysilicon with about 513 A of nickel Ni.
\[ Ni - \text{Thickness} = \frac{NiSi - \text{Thickness}}{\text{Silicon - required - rate}} = \frac{1200 \ \text{Å}}{2.34} = 513 \ \text{Å}. \]

\[ Poly - \text{reacted} = (Ni - \text{Thickness}) \times (Poly - \text{required - rate}) = (513 \ \text{Å}) \times (1.83) = 938 \ \text{Å} \]

The resistivity calculated previously for NiSi was about 31 \( \mu \)Ocm, which about twice the reported value of resistivity for NiSi of 15 \( \mu \)Ocm and that can be cause by couple of reasons including oxygen contamination during sputtering or even during the RTP step because they were not done in a vacuum environment, or it might be caused by some unreacted Polysilicon left after the Silicidation step.

5. Conclusion

This study was successful in forming NiSi that was formed on doped Polysilicon to simulate the effects on gates CMOS regions. In addition sheet resistance was measured using the CDE resistivity mapper and found that it was significantly decreased indicating the formation of NiSi. Further study may include verifying the conversion of Ni to NiSi by fully siliciding the poly, which has to be investigated using x-ray diffraction techniques. As well as varying RTP temperatures to look

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Implementation of Backside Vias as an Alternative to Wafer Thinning

Michael E. Hathorn

Abstract—A study has been performed to determine the viability of Potassium hydroxide (KOH) as a wet etchant to create backside vias to devices previously manufactured on thinned wafers. In order to protect front-side devices in the back end of line process, the KOH must not come in contact with the front of the wafer. A number of methods have been investigated with the advantage being in the use of a coat of black wax. This paper will present results obtained from tests with black wax as well as provide insight to the advantages and disadvantages of other protection options.

Keywords— backside via, black wax, \( R_{\text{on}} \), Potassium hydroxide (KOH)

I. INTRODUCTION

Each new generation of electronic devices are designed to be smaller, faster, and consume less power. By reducing the overall height of a vertical discrete power device, a lower on-state resistance can be achieved. This directly translates to an increased battery life and reduced internal heating.

One solution is to thin the entire wafer in a back end of line process by using mechanical methods. While a valid solution, this compromises the ability of the wafer to be handled because thin wafers become very brittle and can warp and sag. A Potassium Hydroxide (KOH) etch is being considered as an alternative in creating very deep (~300μm) vias. The advantages of using this wet etch process is fast etch rates (~1μm/min) and uniformity across the wafer. Using nitride as an etch mask provides very high selectivity. The major challenge in using a KOH etchant is to eliminate the chance of positive ion contamination into the oxide of the previously fabricated device, thus modifying the operating characteristics and potentially pushing the device to failure.

KOH has been determined to provide sufficient etch profiles and LPCVD nitride has been shown to act as a sufficient etch mask. A number of methods to protect front-side devices such as fitted holders, masking tapes, and black wax have been investigated.

II. THEORY

In any electrical device, each material, barrier, region, etc. in the conduction path of a device will contribute to the overall series resistance of the device. By lowering this resistance contribution, devices can be designed to consume less power and operate cooler due to a reduction in internal heating. This is also described as lowering the on state resistance \( R_{\text{on}} \).

Figure 1 illustrates the regions of a generic vertical device. Note the individual resistance contribution of each region to the total series resistance. If some of these individual resistances can be reduced, that in turn will lower the total contribution and in effect lower \( R_{\text{on}} \). It is possible that the contact metals could be replaced by less resistive alternatives, but this has the potential to limit current flow and cause devices to fail. Modifying the source or drain or channel would cause the electrical properties of the device to be modified, so this again is not desirable. That leaves only the substrate resistance to be modified and the easiest way of doing this is through reducing its thickness.

![Fig. 1. Series resistance contribution in a generic vertical device.](image)

In order to reduce this thickness a backside via etch in KOH etch has been proposed. KOH etches silicon relatively quickly along \(<111>\) planes, creating a 53° silicon etch angle. The concern of using KOH is that it has the potential to
contaminate previously fabricated devices. The positive ions contained in this solution have the potential to contaminate the gate oxide or wells of fabricated devices, thus shifting their electrical properties. Therefore a valid frontside protection method must be developed for this method to be introduced into a back end of line process.

III. EXPERIMENT

Previously manufactured 4-inch PMOS device wafers were obtained in order to test the viability of different frontside protection methods. The process steps of creating backside vias were divided between these device wafers and reclaimed scrap wafers so the fabricated devices would not be introduced to high temperature or plasma processing. All backside patterning and true via etching was done on scrap wafers, while the frontside protection was implemented on the PMOS wafers. Since the proposed process flow, as shown in figure 2 requires nitride as a KOH etch mask, actual vias could not be created because the high temperature LPCVD process would cause the Aluminum contact metal on the fabricated devices to melt, thus compromising the integrity of the working PMOS devices.

A. Protective Tapes

The viability of protective tapes was evaluated because of the ease of implementing this into a process flow. Masking the frontside of a wafer with tape will add little cycle time to the process and allow for wafers to be lot processed. A few different tapes including kapton, and wafer dicing tape were evaluated for their resistance to KOH.

B. Wafer Holder

The use of a stainless steel o-ring sealed wafer holder that had been developed for MEMS applications was also evaluated. By loading two wafers front-to-front into the apparatus and sealing, the fronts are protected, and the back sides exposed for the etch. This is a proven method, however, wafers can easily be broken when manually loaded into the holder and a single holder only allows two wafers to be processed at a time.

C. Black Wax

The third option that was evaluated was coating the front of the wafer with black wax. The in this experiment the wax was hand-painted onto the wafers by dissolving a small amount of the wax in Xylene, and then baking to remove the remaining solvent and to attempt to remove any pinholes in the coat. While this is a time-consuming process, the black wax could be further dissolved and spin-coated similar to a resist process.

IV. RESULTS AND DISCUSSION

Figures 3 and 4 illustrate the profiles of a KOH etch. These were obtained by etching a scrap wafer for about an hour with only a few hundred Angstroms of LPCVD nitride used as an etch mask. This illustrates the very high selectivity of
KOH between nitride and silicon.

Results from the backside etch of the patterned scrap wafers showed expected profiles with a silicon etch rate of around 1μm/min and a nitride etch rate of only about 50Å/hour. Using these rates, the 300μm targeted etch depth for incorporation into vertical devices will take somewhere around 5 hours and only around 250Å of masking nitride is required. Due to this long process time, it is very important that the frontside protection options allow for bulk wafer processing.

A. Protective Tapes

Mixed results were obtained from the attempt to use protective tapes. While the both the kapton and dicing tape held up to the KOH etch, there were adhesion issues with them sticking to the wafer. Shortly after introduced to the heated KOH bath, the tapes began to lift-off. With better selection of high-temperature adhesives or thicker tapes, this experiment may have produced better results. Therefore, this method should not be disregarded, but investigated further.

B. Wafer Holder

The wafer holder was shown to efficiently protect the frontside of the device, however, it was not used any further in this work because of the long loading times and its ability to only process two wafers at a time. This could be used as a valid option for a proof-of-concept, however, this solution could not be effectively implemented into manufacturing.

C. Black Wax

The best option for frontside protection was determined to be a coat of black wax. Figure 5 shows the ID-VG plot of a PMOS device measured before and after being exposed (with black wax protection) to a KOH etch. Note that there is no identifiable shift in the threshold voltage, indicating that the KOH did not contaminate the device.

These results are very promising since they indicate that black wax sufficiently protects frontside devices from positive ion contamination when introduced to KOH. However, when the device wafer was etched in this experiment, nearly 75% of the devices were destroyed because the KOH was able to get beneath the black wax and attack the devices, namely the aluminum contacts. This can be attributed to problems with the hand coating of the black wax. Even though the wafers were baked after coat, some visible pinholes still remained in the wax coat. This allowed the etchant to get under the wax at various locations and destroy the devices.

In order to prevent this, better coating techniques need to be developed. It is possible that the black wax can be completely dissolved into a liquid form in order to allow the material to be spin-coated similar to resist. This will allow for extremely better uniformity and the ability to control thickness.
V. CONCLUSION

This study was successful in demonstrating the ability for black wax to sufficiently protect frontside devices. In areas where the black wax did not lift off, devices did not exhibit any shift in $V_t$, indicating that there was no positive ion contamination into the gate oxide or device wells resulting from exposure to the KOH etchant. Better coating techniques remain to be developed in order to uniformly protect the entire front surface area of each wafer during the wet backside etch. This technique should also be applied to a true vertical device so that the advantages in the creation of a backside via for thinning purposes can be quantified by electrical characterization.

ACKNOWLEDGMENTS

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Michael E. Hathorn, originally from Kane, PA, received a B.S. degree in Microelectronic Engineering from the Rochester Institute of Technology in 2004. He obtained co-op work experience at Photronics in Allen, TX, and at Infineon Technologies in Richmond, VA.
Abstract—In this investigation and process development project, a novel method for directly connecting two computer chips together, both electrically and physically was developed. This process utilized several processes and materials that are already used in semiconductor manufacturing and packaging. By using these common materials and processes, it simplifies the implementation of the process, and removes several potential roadblocks. It was found that two chips could successfully be bonded together physically and connected electrically.

Index Terms—Bonding, Chip Bonding, Copper, Interconnect, Solder Sphere,

I. INTRODUCTION

In order to improve performance of high-end microprocessors, it will become necessary to target power consumption more intelligently, reduce the length of interconnects between sections of the microprocessor, and develop methods to make the manufacturing process more robust to transistor failures. By fabricating different subsystems of the chip individually, leakage can be targeted separately for each component. Individual sections, which are defective, such as SRAM, can simply be discarded without an entire processor being rejected. By then assembling the subcomponents using face-to-face connections, shorter path lengths with lower resistance and capacitance can be achieved, resulting in a three-pronged performance gain.

In this investigation, a novel chip to chip interconnect process was designed, fabricated and tested – direct, face-to-face chip interconnect without through-wafer etching. The connection is made between two copper interconnect layers which are standard in all high-end microprocessors. The process used many materials that are common to semiconductor packaging, and as such, are highly available. The interconnect layer makes use of a thick layer of negative photoresist in which a pad is exposed. The pad is then filled with solder, which is placed through standard solder sphere placement methods. A second chip is then mounted on top with a complimentary process. Additional investigation was made into alternative methods of connecting die without sacrificing packing density or requiring drastically different layout methodology.

II. PROCESS DEVELOPMENT AND DESIGN

A. Process Development

Each process step was developed in sequence, as the wafer progress through the line. When there were holdups, such as tools being down, process development was initiated on dummy wafers. Dummy wafers were also used for development of SU-8 coating, as no reclaim was possible. The key to this project was the process integration, which required in-situ analysis and process modification. When tool and facility issues required a deviation from the intended process, results that are “close enough” were accepted, to limit the scope of the project. An example of “close enough” was that copper polish was not possible, a wet etch process for copper was used. In the case of the wet etch, there was an over etch, as CD variation is not critical. Wafers were left behind at key process steps as backups and for process refinement. The design of the two chips allowed for a pair of die to be fabricated, diced, and then flipped, creating a functional pair that enabled a multitude of tests. Different test structures were included to verify electrical characteristics, reliability and manufacturability.

B. Chip Design

Test Chip A (Figure 1) has 2 sets of Cross Bridge Kelvin Resistors to allow for contact resistance measurements, a densely packed cluster of interconnects with the ability to test 64 consecutive interconnects, 32 interconnects, or 16 interconnects, as well as 4 isolated interconnect test structures.

Test Chip B (Figure 2) has the same dense interconnect structure; with the ability to test interconnect chains of the following lengths; 2, 4, 10, 12, 14, 16, 32, and 48. Test Chip B also has the 4 isolated structures seen on Test Chip A.

By flipping chip B horizontally, rotating 180 degrees,
aligning them with the verniers on each edge the two chips can be bonded together, creating the interconnects between the pair of chips (Figure 3).

![Figure 1: Test Chip A.](image)

![Figure 2: Test Chip B.](image)

![Figure 3: Test Chips A and B aligned.](image)

C. Process Flow

The process that was finally used was based on available equipment, materials and processes. Starting from a bare silicon substrate, silicon dioxide was grown using a wet thermal oxidation process. Ideally, a high quality, low temperature oxide would be deposited, as would be the case in a high-end microprocessor, but this process was not available until after it was needed. Copper was then sputtered onto the oxide. Ideally a damascene process would be used instead, however disposal of copper contaminated slurry was not a feasible option.

The wafers were then coated with Shipley 812 photoresist and patterned using a one-to-one contact aligner. The copper was etched using a wet etch solution of DI water, Hydrogen Peroxide, and Sulfuric Acid. The etch chemistry quickly etched copper by converting it from solid copper into a solution of copper sulfate. The photoresist was stripped using acetone and isopropyl alcohol, followed by a DI water rinse. See Figure 4 for cross section.

![Figure 4: Cross section after copper etch.](image)

The wafers were heated on a hot plate to drive off any water and then coated with SU-8 2050 using a low spin speed to achieve the desired thickness. The SU-8 requires long bake steps in order to remove solvents, which make the resist tacky. Allowing the wafers to cool and finish drying after the bake was complete also assisted in reducing the tackiness of the film. The SU-8 was patterned, also using contact printing. The resist was then baked in order to allow cross-linking and then developed. A hard bake was performed to strengthen the resist. The processing of SU-8 was based on the material brochure provided by the manufacturer. See Figure 5 for cross section.

![Figure 5: Cross section after SU-8 processing.](image)

The wafers were then coated with Shipley 812 photoresist and patterned using a one-to-one contact aligner. The copper was etched using a wet etch solution of DI water, Hydrogen Peroxide, and Sulfuric Acid. The etch chemistry quickly etched copper by converting it from solid copper into a solution of copper sulfate. The photoresist was stripped using acetone and isopropyl alcohol, followed by a DI water rinse. See Figure 4 for cross section.

![Figure 6: Final cross section.](image)
The wafers were then diced using a wafer saw, followed by a cleaning process and a removal of the protective tapes. The chips were then individually processed, applying solder spheres and heating. The second chip was then placed on top, both chips were heated and force was applied to achieve better contact. This process connected the two chips, both electrically and structurally. See Figure 6 for cross section.

II. RESULTS

Each process was successfully developed and processed in sequence. There was significant yield loss from SU-8 adhesion issues and solder sphere placement. While bonding was proven, the electrical connection on the device chips could not be verified due to an insulating layer over E-test pads. The insulating layer was most likely due to copper oxidation. In order to prevent this, all thermal processing after SU-8 development would need to be preformed in an inert ambient. It was proven experimentally that a copper film, heated in an ambient containing oxygen and water would become insulating.

IV. CONCLUSION

If further work is to be done in this area, there are several ways to improve the processes. Some were not used due to time and financial limitations. Such improvements include developing some sort of method to align the chips. This could be accomplished easily through modification of a microscope stage, as it has control over the x-axis, y-axis, z-axis and theta-axis. A robust stage could also apply the force needed to bond the chips. This system would need to be contained within a simple environmental chamber that could be filled with nitrogen as an ambient, using a simple hotplate for heating the chips.

Film adhesion could also have stood some improvement. The copper adhesion to oxide was poor, but strong enough. This could have been improved though an adhesion layer, however the etch process would have been more complicated. Ideally, TaN would be used with a CMP process, removing the need to etch two metals. The adhesion of the SU-8 to the oxide proved to be an issue that could keep this process out of manufacturing. The adhesion could be improved through further investigation. The limitation to investigating the adhesion failure is that it is not apparent until after wafer dicing, creating a slow feedback loop.

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Jeffrey A. Steinfeldt will graduate from the Microelectronic Engineering Department at Rochester Institute of Technology in May of 2004. J. A. Steinfeldt has accepted a full time job with Intel Corporation in New Mexico. J. A. Steinfeldt completed all of his co-op requirements with Intel Massachusetts, a wholly owned subsidiary of Intel Corporation.
Silica Waveguide Design and Fabrication using Integrated Optics: A Link to Optical VLSI Photonics Integration for Semiconductor Technology

Anthony G. Navarro, Student Member, IEEE

Abstract — The hardmask NiCr, has shown to be the optimum alloy in reducing sidewall roughness (SWR) in planar waveguide geometries. Within this study, the NiCr hardmask has been demonstrated using a lift-off of NiCr. In comparison, a NiCr etchant from Transene™ is used to compare how well sidewall roughness is reduced, and how the RIE - CHF₃/O₂ gas mixture improved anisotropy. From the results obtained, NiCr is a robust material that reduces sidewall roughness, and is the best metal to use, with the least amount of transferred striations. The CHF₃/CF₄ gas mixture in the AME-P5000 RIE tool proved to have better anisotropy and selectivity with respect to TEOS/Si₃N₄/Thermal Oxide (5000 Å/layer) respectively.

Index Terms — NiCr hardmask, SWR, planar waveguide geometries.

I. INTRODUCTION

Integrated optics are widely research for military and communications applications. Hybrid devices in optoelectronics have improved the versatility of what can be designed, and fabricated all in one intra-chip application. As indicated by the 2003 ITRS roadmap, one major limitation to the speed of CMOS devices is capacitive coupling due to interconnects [4]. Photonic devices integrated onto silicon substrates are one means of alleviating this problem. For example, optical interconnects pass through free space at a much higher rate than traditional interconnects.

In order for a waveguide to be practical, the signal attenuation or optical loss must be engineered to a value below 1 dB/cm. The primary source of loss in waveguides stems from light scattering due to sidewall roughness of the waveguide. Even a sidewall roughness of 50 nm can result in high loss. For this reason, the targeted sidewall roughness is < 10 nm. This paper will explain the mechanisms underlying sidewall roughness. The particular Si-compatible structure examined herein will be an oxide/nitride/oxide structure.

II. THEORY

A) Electromagnetic Principles of Optical Waveguide Theory

The basic idea of a waveguide is a media configuration that guides electromagnetic waves through a fixed path. In particular, the guides that are of interest in this project pertain to “closed waveguides”.

B) Waveguide Geometries and Media Configurations

The geometries that will be designed for the project at hand are the following:

(a) straight waveguides
(b) bended Waveguides
(c) tapered waveguides

Straight waveguides can be represented in a Cartesian (x,y,z) coordinate system. A cross-section of a basic planar guide can be represented in the following figure implementing the [SiO₂/Si₅N₄/SiO₂/Si (substrate)] configuration illustrated in Fig. 1.
The core and cladding layers will give appropriate scatter ratio to release an effective index of refraction difference $\Delta n$. The actual index of refraction values for proposed media via experimentation is:

<table>
<thead>
<tr>
<th>Actual Material Properties for Silica Waveguide Materials</th>
</tr>
</thead>
<tbody>
<tr>
<td>Materials</td>
</tr>
<tr>
<td>SiO$_2$</td>
</tr>
<tr>
<td>SO$_2$</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
</tr>
</tbody>
</table>

To better understand this concept, the nitride layer shall carry most of the photonic density. At the same time, the oxide layers will confine the light in the nitride, as well as the air interfaces on both sides of the strip. The interface should give a relatively high index between 0.1-0.5.

Looking at the bend in Figure 2, it must be said that the internal reflection of a straight waveguide is disproportional by a radial dependence. On the other hand, a tapered waveguide is a fan shaped guide that takes either a large or small density of light and outputs smaller or larger light propagation respectively.

III. EXPERIMENT

The design parameters at hand depend on the refractive index difference at the oxide / nitride interface. One wants to ensure that there is no oxy-nitride interface that will cause the light to flood into the oxide boundaries. Therefore, there must be satisfactory process control for this. Another issue, perhaps the most influential, is the line-edge roughness of the waveguides. In order for the guides to work at all, the sides have to be extremely smooth. A very careful etch process must be made to minimize roughness at all costs. In order to pattern these waveguide structures, there has been a recommendation of a “lift-off” process [1]. The end product should allow clean sides of the guide regardless of its geometry.

The issue in Figure 4, pertained to the particular etch mask used, resist material, or even the gas composition used in the RIE process. These are part of the fabrication process needed to successfully
fabricate a working waveguide as mentioned briefly in earlier parts of this proposal.

The sidewall roughness of a waveguide must be $<$ 10 nm for this application. In particular, Figure 4 uses InP and InGaAsP materials for the bended waveguide fabrication. Also, it is important to mention that NiCr was chosen due to small grain boundary size.

Several wafers were supplied by RIT SMFL for the project as N-Type $<$100> plane / $\Omega$ = 10-15 $\Omega$-cm resistivity. The earliest experiments involved the proper dose characterization of the polymer to enhance the lift-off phenomena. Before getting into this effect, it must be shown exactly what device wafers received what thickness of dielectric media. Blanket depositions of SiO$_2$ and S$_6$N$_4$ were organized into a split order of:

<table>
<thead>
<tr>
<th>Device Wafer</th>
<th>Waveguide Process Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1-D4</td>
<td>Target $T_x$ = 5000 Å - (TEOS/SiO$_3$N$_4$/Wet OX)</td>
</tr>
<tr>
<td>D4</td>
<td>Wafer taken from D1-D4 split for VASE Analysis / RIE DOE</td>
</tr>
<tr>
<td>D5-D6</td>
<td>$T_x$ = 1000 Å - (LTO/Si$_3$N$_4$/Bare Si)</td>
</tr>
<tr>
<td>D7-D10</td>
<td>$T_x$ = 1000 Å - (LTO/Si$_3$N$_4$/Wet OX)</td>
</tr>
</tbody>
</table>

Figure 6: Waveguide Process Split Description - Cladding / Core layer implementations

- Blanket Deposition 1000 Å SiO$_2$
- Blanket Deposition 1000 Å Si$_3$N$_4$
- LEVEL 1 AZ5214E-IR Resist Coat

Figure 7: Blanket Deposition of Waveguide dielectrics. Top Layer SiO$_2$ cladding layer is 1000 Å LTO for wafers D5-D10. SMFL Factory Si$_3$N$_4$ is used as base core layer for all device wafers (D1-D10). A table will be supplied for all thickness variations.

A) Waveguide / Image Reversal & Lift-off Process Flow

1) 6" ASM LPCVD - 4" Blanket Depositions followed by manual dispensing of AZ5214E-IR resist on the SVG Track:
2) Waveguide VLSI g-line Photolithography

Figure 8: Level 1 g-line Photolithography using AZ5214E-IR resist. GCA g-line exposure time is \( t = 0.26 \text{ sec} / 36.25 \text{ mJ/cm}^2 \). Softbake temperature is 105°C, Post-Exposure Bake (PEB) is 120°C. Karl Suss™ flood exposure is 400 mJ/cm².

Within the three vertically stacked arrays, there are straight, bended, and tapered geometries. The widths of the straight layers \( \Delta L_{\text{eff}} \) vary in a series of 0.2, 2.0 \( \mu \text{m} \) increments. Length of the taper fan-in/fan-out is 100 \( \mu \text{m} \), followed by tapering lengths of 20 and 200 \( \mu \text{m} \) varieties that are then adjoined into a straight waveguide. In conjunction, the straight waveguide is merged into an identical fan-out taper at the opposing end.

4) NiCr Lift-off Integration

NiCr was sputtered using the CVC601. The chamber is arranged to hold multiple 4” or 6” substrate on a metal platen that is mounted on an axle that is controlled by...
the rotostrate mechanism. In this regard, substrates could also be cleaved and taped on the aluminum dummy wafers face down on the platen hub. Teflon tape is used as an adhesive to bond the sample to the dummy wafer. A 4" NiCr Alloy \{80 – 20 wt%\; 0.25 in thick\} was utilized. Since direct line-of-sight is used to avoid sidewall coating during sputtering, this allows the unwanted metal to dislocate around the transferred image (5X reduction).

Similarly, the CHA Evaporator is also exploited to do the same procedure. The metal alloy deposition has completely different physics involved to perform the comparison. A steel bell jar is used to harness the pressure to suspend the melted alloy droplets that propagate through the low pressure ambient. A tungsten boat is used to hold the NiCr pellet, and is tightened down between two electrodes, which will conduct current in a circuit. Importantly, the samples are to be mounted on additional 4" aluminum dummy wafers, and two metal rods are to be placed in parallel to hold the dummy flat directly above the evaporating source (direct line-of-sight).

IV. RESULTS AND DISCUSSION

After careful process optimization, lift-off of NiCr was successfully achieved (Fig. 11).

Figures 11-12 denote some observable roughness at the edges. Some of the metal has truly experienced lift-off in some regions, but in others, there was some oval notching due to MEBES mask loading effects. Periodic fracture lines are apparent to where the sampled direct-write functions have merged the polygons that created the waveguide features (NWAVE690.gds file conversion). Since NiCr has a small grain boundary size, the reactive-ion etch (RIE) could be optimized to balance the surface roughness in many regions. Now that nickel chrome (80 – 20 wt %) has been developed for RIE, other hardmasks such as Cu and Al will be compared to the preceding results.

The result from Figure 11 ensures that planar waveguides can be fabricated in the cleanroom without any residual layers forming in the ASM 6" LPCVD tube furnace. If also available, the PECVD chamber in the AME – P5000 tool, could yield better film uniformity for additional comparison.

The reactive ion etch performed for sample dies cleaved from D7 were sputtered with 1000 Å of NiCr alloy that was subsequently lifted off.
In Figure 13, we can see that the micrograph shows that significant roughness has transferred from the NiCr hardmask (Lift-off). There is also some "grassy" polymer build-up around the perimeter. This situation is being caused by the CHF$_3$ / O$_2$ gas mixture being used.

It was determined that the Drytek Quad RIE had its limits to improving the etch selectivity of the dielectric layers. Sample D7-B was prepared with just O$_2$ increased to 20 sccm. No discernable improved was observed. Sidewall roughness ranged in between 50 – 100 nm range through the waveguide array.

Finally, Figure 15 depicts that there is substantial polymer buildup around the feature. Anisotropy is greatly improved, but much work is needed to optimize a custom recipe. The AME P-5000 is a promising alternative to using the Drytek Quad tool. Contamination could also be present due to the fact that the chambers need longer seasoning in between recipes. It is also important to note that there is no O$_2$ line that goes into the tool. This could also be a useful upgrade to enhance RIE performance.

V. CONCLUSION

Anisotropic etching of SiO$_2$/Si$_3$N$_4$/SiO$_2$ waveguides was successfully demonstrated. The etch mask, NiCr, was also found to successfully lift-off via AZ5214E resist when a line-of-sight deposition was performed. The resulting
sidewall roughness was on the order of 50-100 nm. Further work must be performed to limit the effects of micromasking due to polymer deposition on the substrate during etching.

VII. ACKNOWLEDGMENTS

The author would like to personally thank Branislav Curanovic, Stephen Sudirgo, and all technical staff for their outstanding assistance in RIT Semiconductor and Microsystems Laboratory. Also, a strong recognition is reserved for Dr. S.L. Rommel and Dr. S.K. Kurinec for project advisement and/or assistance on the LEO SEM EVO 50 workstation.

VIII. REFERENCES


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[19] VASE™ analysis was performed by Jianming Zhou

Anthony G. Navarro (S’02) is originally from Basque-Cuban origin, and was born in Rahway, NJ in 1979. His ultimate drive is to become a research scientist in nanophotonic interconnect embedded in semiconductor nanosystems. A former research internship has been performed in the Department of Electrical Engineering in Rochester Institute of Technology, and also an internship in Integration Engineering at National Semiconductor in South Portland, Maine. He has received a B.S. in Microelectronic Engineering in May 2004 at Rochester Institute of Technology. Current prospects involve completing an M.S. degree in Imaging Science there also.
Investigation and Development of Air Bridges

Jay Cabacungan

Abstract — A study was done in order to develop a fabrication process for creating air bridges at RIT's Semiconductor and Microsystems Fabrication Laboratory (SMFL). Process development looked at three key factors (i) a robust lithography process that would produce the necessary rounded profile for fabricating air bridges (ii) sputter deposition vs. evaporation as metal deposition techniques (iii) the strength of the structures by testing the maximum distance an air bridge could span, the minimum and maximum thickness the structure could support, and the dimensions of the support posts. Several samples were fabricated testing the three different factors studied and SEM micrographs of the structures were taken for analysis. A baseline fabrication process was then created for use at RIT's SMFL.

Index Terms — air bridge, MEMS, free standing microstructures, high speed interconnects.

I. INTRODUCTION

The development of MEMS devices and the growing need for high speed interconnects in integrated circuit applications have called for the development of free standing microstructures known as air bridges. Many MEMS devices have facilitated the use of such structures in their design, while the need for lower frequency response in high speed integrated circuits make air bridges perfect candidates for simple interconnect systems due to the use of air as the separating dielectric medium. The ability to fabricate such structures are crucial in MEMS and high speed analog devices and thus the development of such a process will allow RIT and SMFL to further research in MEMS and high speed analog devices. Furthermore the low frequency response of air bridges due to the lowered capacitance in the line makes such structures viable candidates for high speed digital interconnects.

Simplicity is the key to process development as a simple process not only reduces the time required for fabrication, but also produces the most robust process due to the reduction in error in processing from a reduced number of steps.

For the process developed at SMFL a simple two level lithography process was chosen. Several factors were of interest during development. Of particular interest to development were the strength of the bridge with respect to the bridge size and metal thickness and the lithography process used to define the shape of the bridge. A small DOE was conducted in order to determine how these process steps and structural characteristics affected the overall process. Development of this process will eventually be integrated into device fabrication.

II. THEORY & PROCESSING CHALLENGES

A. Bridge Theory

Continuing on the theme of simplicity the basic design of an air bridge is based on the simplest of all bridges, the arch bridge. Arch bridges have great natural strength and the simplicity of the design makes it ideal for microstructure fabrication. The physics of an arch bridge, which the design of the air bridge is based on, is the distribution of force throughout the bridge. There are several forces that act on a bridge that both work to keep the bridge standing and to bring the bridge down. A simple diagram of the fundamental forces acting on a bridge can be seen in Figure 1 [1].

![Figure 1: Basic Force Distribution on a Bridge](image)

In order for the bridge to remain standing, an equal distribution of forces must be achieved. In other words the sum of all the forces acting on the bridge must be in equilibrium. Looking at Figure 1, there is a downward force, F, applied by the load of the bridge. This downward force is translated to the supports of the bridge, R1 and R2, which in turn exerts an opposing force to the force applied by the load of the span. As long as the force applied by the load is equal to the sum of the forces applied by the supports, the bridge will stand. This is mathematically illustrated on the following page.
The fundamentals of the distribution of force in a bridge can be applied to any type of bridge made, and can easily be applied to the forces acting on an arch bridge, which the air bridges being fabricated are based on. In an arch bridge the weight of the span exerts a downward force on the bridge. This force is transferred along the span of the bridge and eventually translated over to the supports of the bridge. This force is then conveyed into the ground. In terms of the air bridge the downward force of the load will be translated into the substrate.

Newton’s Third Law of Motion states that for every action there is an equal and opposite reaction. It is this fundamental law that keeps the bridge up for the downward force of the span working to collapse the bridge is met by an upward force of the substrate acting in opposition. This force is transferred from the substrate onto the support posts, which in turn translates the force onto the span. This force is applied in the opposite direction relative to the force applied by the load and works to keep the bridge standing. This is illustrated in Figure 2 [2].

![Figure 2: Force distribution in an arch bridge. (a) The load exerts a downward force on the bridge that is translated onto the supports. (b) The substrate exerts an equal but opposite force onto the supports (c) that is transferred to the span of the bridge and works in opposition to the downward force of the load.](image)

The strength of an arch bridge comes from the arch itself. The ability for the bridge to translate the downward force on the span to the supports and the consequent upward force from the substrate to the span is made easier by the gradual change from span the support present in an arch structure. This, in turn, is what gives the bridge strength. It is this and its simplicity that made arch bridges the perfect candidate to base the air bridge design on.

### B. Processing Challenges

Lithography presents one of the major processing challenges in fabricating air bridges because it is used to define the shape of the bridge. Since the air bridges being fabricated are based on an arch bridge, it is necessary to develop a resist process that produces a rounded sidewall profile that will define the arch of the air bridge. This is contrary to conventional resist processing that demands high angle straight walled resist profiles. In order to obtain the rounded profiles necessary for air bridge fabrication the first level photoresist, which defines the shape of the support posts, must be rounded by reflowing the resist and this is done through heating.

Heating photoresist may not present problems early on in the process flow, as several bakes are necessary to prepare the resist prior to exposure, but heating necessary for a rounded profile can present problems further in the process. The basic lithography process consists of six main steps.

1. Dehydration Bake & Adhesion Promotion
2. Photore sist Coating
3. Soft Bake — Solvent Removal Bake
4. Exposure — Patterning Resist
5. Develop
6. Hard Bake — Harden Resist

Of particular interest, especially in further process steps are the dehydration bake, soft bake, and hard bake. While these bakes may be necessary to round the resist profile, they also have other adverse effects that could, especially after metal deposition.

The pre-bake also known as the soft bake is the physical process of conversion of a liquid-cast resist into a solid film [3]. This is done by heating the resist to above evaporation point of the casting solvent, but not high enough to degrade the photosensitive chemicals in the photoresist. During this stage of lithography a huge amount of solvent chemistry is out-gassed from the resist. This out-gassing of solvent could prove problematic after deposition of the metal film that is placed on top of the first layer of resist. While most solvents are evaporated during the soft bake some solvents still remain and when baked will continue to out-gas possibly deforming the metal film now covering the first layer of resist. This problem is also of concern for the second level dehydration bake that is done at a much higher temperature than the soft bake. The problem of solvent out-gassing after metal deposition will limit the thermal budget of the process after metal deposition.

In order to leave free standing structures the underlying layer of resist that supports the bridge to the final fabrication step must be easily removed. This is another step where previous bake could prove problematic to the outcome of the entire process. Baking resist at high temperatures invokes a thermochemical reaction in the resist where the resin, sensitizer, and/or solvents present in the film become hardened [4]. This step is critical in conventional resist processing as it prepares the resist for subsequent process steps where the resist acts as a type of masking layer, but is detrimental the air bridge fabrication because it makes removal of resist in the final step more
difficult. Hardening of resist can be a problem in high temperature bakes such as the dehydration and hard bake. Alignment is another crucial factor in the fabrication process and could present problems of its own. Alignment is critical as improper alignment could lead to a partial or even total collapse of the bridge structure. Second level lithography must be aligned precisely so that the resist masking the metal film and defining the span of the bridge also covers the support posts. If this does not occur part of the supports could be etched away in the subsequent metal etch step weakening the structure. The three layer film stack consisting of the first layer of resist, metal, and second layer of resist could also cause the loss of the alignment marks. With the importance of alignment on the structural strength of the bridges, the loss of alignment keys is an undesirable side effect to the process, and thus methods of maintaining the alignment keys under three film layers is critical to the process.

III. EXPERIMENTAL DESIGN

The goal of this project was to develop and optimize a process for fabricating air bridges using the available toolset at SMFL. In order to do this several key factors in the fabrication process were selected and studied in order to optimize and test the limits of the process. Resist processing is critical in the fabrication of air bridges as it defines the shape of the bridge. This is especially important in the first level lithography where the shape of the resist profile will determine if the air bridge will have an arch shape critical for support or not. The significance of resist processing in the fabrication process developed required the need to look at two candidate resist processes for fabrication. The two resists considered were Shipley 812™ Positive Resist and AZ5214E-IR™ Resist. The Shipley 812™ process is the standard positive tone process used for g-line lithography at SMFL. AZ5214E-IR resist is often employed in image reversal processes and was used as a candidate process to test against the standard process.

Metal deposition technique and metal thickness were other factors studied during process development. Two different metal deposition techniques, evaporation and DC sputtering, were placed under consideration. The conformal coating of sputtering as well as heating that occurs due to the plasma make DC sputtering the perfect candidate for fabricating strong support structures as well giving the resist an extra chance to reflow during metal deposition enhancing the arch of the bridge. On the other hand, excessive heating during sputter deposition could harden the resist further making it more resistant to resist stripping chemistry. Opposite to DC sputtering is evaporation, where the resist is not heated solving the concerns of hardened resist. The nature of evaporation however could affect the conformity of the film, particularly the sidewall coverage. This is because film coverage using evaporation is based on the substrates line of sight to the target. Sidewall coverage is crucial to the structural strength and stability of the air bridge as the metal that covers the resist profile will define the supporting structure of the air bridge. The enhanced rounding effect due to extra heating during sputter deposition will not be present during evaporation.

Several metal film thicknesses were studied as well in order to determine the maximum and minimum metal thickness that the structures could support. Thick metal films could present too much load force on the bridge while thin metal films may not give the bridge enough support to remain standing. Three metal thicknesses were picked to represent the minimum, mean, and maximum metal thicknesses. These thicknesses were 2000Å, 5000Å, and 10000Å. Aluminum was chosen as the metal film due to its wide use at SMFL. Other metal films could be used, but further investigation is needed.

In order to examine the structural strength of the air bridges a mask was designed that would test distance an air bridge could span as well as the width of the bridge. Of particular interest to development was to see if the distance spanned by the bridge was a function of the width of the support posts/bridge. A small experiment was designed into the mask in order to investigate these factors. Four support/bridge width thicknesses were chosen and the mask broken up into four cells. The basic mask design is depicted in Figure 3.

![Figure 3: (a) Basic Mask Layout. (b) Bridge Schematic](image-url)
As seen in Figure 3a, the mask was divided into four different cells each with a different support size/bridge size. With in each cell are five bridges of the same basic design as seen in Figure 3b. The distance between each posts, that defined the span of the bridge was repeated several times to ensure the repeatability of fabricating a bridge at a given span. Each span was in turn incremented in order to examine the structural strength of the bridge as the span increased and to determine at what span distance for a given support post width and metal thickness the bridges start losing structural integrity. Table 1 shows the initial and final span for each bridge, span increments, and number of support posts per span.

<table>
<thead>
<tr>
<th>Bridge Num.</th>
<th>Initial Span (µm)</th>
<th>Final Span (µm)</th>
<th>Increment (µm)</th>
<th>Posts per Increment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell 1 (2µm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I</td>
<td>2.00</td>
<td>10.00</td>
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</table>

Mask was designed using Mentor Graphics IC Station™.

Of final importance to process development was to determine the best resist stripping procedure for removal of resist at the final step of the fabrication process. Two methods were looked at. A wet etch method using acetone followed by a clean in isopropyl alcohol (IPA) and a dry etch process using oxygen plasma were studied. As with the two metal deposition techniques each method presented its own advantages and disadvantages. The wet etch approach using acetone is more gentle than the dry etch method and would present less chance of damaging or deforming the air bridges during the last step of fabrication. However, acetone may not be aggressive enough to remove all of the resist leaving structures that are still partially supported by photoresist. Complete removal of photoresist while leaving the air bridges undamaged were necessary characteristics in this last step of the process.

IV. PROCESS DEVELOPMENT

In order to simplify the fabrication process, a two level lithography process was designed to fabricate the air bridges. The basic fabrication process is begins with the first level lithography in which the support posts of the bridge is imaged into the first layer of photoresist and developed. This process step is one of the most crucial steps in fabrication as this first layer of resist not only defines the support infrastructure of the bridge, but also supports the bridge throughout the entire fabrication process. Metal deposition follows first level lithography in which a film of aluminum is blanket coated on top of the first layer of resist. The bridge span defined by second level lithography. The patterned photoresist is then used as an etch mask and aluminum that is not part of the air bridge is etched away. The final step in the fabrication process is to remove the resist layers leaving a free standing aluminum air bridge. The basic process flow is illustrated in Figure 4.

First Level Lithography: Post Definition

![Figure 4](a) First level lithography. (b) Aluminum deposition. Second level lithography and etch (c) top down view (d) cross-section. (e) Aluminum air bridge.
As stated in the Experimental Design section the factors under investigation were resist process, metal thickness, bridge dimensions, and resist stripping process. In order to optimize the process these factors were thoroughly examined during development. The process steps defined in Figure 4 (a-e) were used in fabrication.

The resist process used for first level lithography was the Shipley 812© Positive Resist process. Wafers were coated on the SVG88 Coat Track using standard recipe settings. Two wafers were coated for each of the three aluminum film thicknesses studied during this experiment. One wafer would have aluminum deposited via evaporation and the second via DC sputter deposition. Wafers were exposed using the GCA6700 g-line stepper followed by a develop step and hard bake on the SVG88 Develop Track. For first level lithography the standard develop and hard bake recipe was used. The samples were then loaded in their respective deposition tool, the CVC Evaporator for the evaporated sample and the CVC601 for the sputtered sample, and the desired metal thickness was deposited onto the wafer. For evaporation the metal thickness was determined by the Inficon Gauge located on the tool and the deposition stopped when the desired thickness was reached. The desired thickness using sputter deposition was reached by setting the correct deposition time based on the deposition rate for the 2000W aluminum deposition recipe. Deposition rate was found empirically by SMFL Process Engineer. In both cases a glass slide was placed in the deposition chamber with the sample wafers. The glass slides were used to determine the actual thickness of the aluminum film using the Tencor P2 Profilometer.

After aluminum deposition the wafers were then recoated with photoresist for second level lithography. Coating was once again done on the SVG88 Coat Track. Due to concerns of out-gassing from the first layer of photoresist, now underneath the metal, deforming the aluminum film no HMDS prime was used for second level lithography. These concerns were verified when a sample was accidentally run through the HMDS coating process and the aluminum film deformed. Fortunately the bake temperature for this step cannot be modified due to the sensitive nature of this particular step in the image reversal process. Results will be discussed more in the following section.

V. RESULTS & ANALYSIS

Samples processed were cleaved for SEM analysis. Analysis was done on the LEO EVO50 SEM.

One set of samples were set aside to test the effectiveness of the AZ5214E-IR© Image Reversal process as a second level etch mask. Shipley 812© was strictly used for the first level lithography due to its effectiveness at achieving the necessary rounded profile. Further investigation could be done to determine the viability of using AZ5214E-IR© in both positive tone and image reversal for first level lithography.

Samples processed with AZ5214E-IR© resist for second level lithography were processed using similar process steps as samples prepared using Shipley 812© for second level lithography. Wafers were coated with Shipley 812© resist on the SVG88 Coat Track and first level imaged on the GCA6700 g-line stepper. A 5000Å aluminum film was then deposited on the samples. Following the process flow of the previous samples one wafer had aluminum deposited via evaporation and the second via sputter deposition.

The image reversal process diverges from the standard Shipley 812© process with the second level lithography. HMDS priming was once again not used, but AZ5214E-IR© resist was manually dispensed onto the wafer at a spin speed of 4200RPM. Soft bake temperature, as in the Shipley 812© process was set to 105°C. Coating process was done on the SVG88 Coat Track. Wafers were then exposed on the GCA6700 stepper using a dark field mask (opposite that of the mask used in Shipley 812© processing) followed by the image reversal bake set to 123°C on the Fairweather TPS1010 Hotplate. Wafers were then flood exposed on the Karl Suss MA150 Contact Aligner at an exposure dose of 200mJ/cm². Wafers were then developed on the SVG88 Develop Track, with a develop time set to 1:15 min over the standard 0:45 min used in Shipley 812© processing. No hard bake was used. Aluminum was then etched using wet aluminum etch chemistry at 50°C and resist removed using the Branson 3200 Oxygen Plasma Asher. Initial results showed that out-gassing during the image reversal bake cause the aluminum film to deform. Unfortunately the bake temperature for this step cannot be modified due to the sensitive nature of this particular step in the image reversal process. Results will be discussed more in the following section.

Figure 5: Scanning electron micrograph of an air bridge with post width = 16um, length = 64um, and metal thickness = 1um.
Figure 5 is an SEM micrograph of an air bridge with a width of 16µm and a span of 64µm. The thickness of the aluminum film is approximately 1µm. This sample demonstrates the ability for an aluminum air bridge to support a relatively huge load and remain free standing and is a prime example of the strength of an air bridge.

Figure 6: Scanning electron micrograph of an air bridge with post width = 16µm, length = 58µm, and metal thickness = 2000Å.

Figure 7: Scanning electron micrograph, center span of air bridge shown in Figure 7. This bridge is suspended, but is bowed at the center.

Figure 6 and 7 show an air bridge with a span of approximately 58µm. This particular air bridge has mask post dimensions of 16µm and has an aluminum film thickness of 2000Å deposited via sputter deposition. Figure 7 is an enlarged picture of the center span of the bridge. There is a slight drop in the height of the span indicating that the bridge is close to the limits of its structural strength, but with a film thickness of only 2000Å and a span of 58000Å (58µm) this is another prime example of the strength of the structure.

Figure 8 shows the results of the rounded resist profile indicating the effectiveness of the Shipley 812™ resist process in fabricating air bridges. Metal was sputtered on this sample also supporting the hypothesis that sputter deposition would be the optimal deposition process for fabrication of air bridges using the developed process. Furthermore, when comparing this image to the micrograph shown in Figure 9 the film thickness at the support in Figure 8 is more conformal and thicker than the support shown in Figure 9 indicating the greater strength of sputtered air bridges over evaporated air bridges, however further samples will need to be fabricated in order to verify this hypothesis.

Figure 8: Scanning electron micrograph of the support post of an air bridge. Metal was deposited via sputter deposition. Notice arch profile.

Figure 9: Scanning electron micrograph of the support posts of another air bridge. Metal was deposited via evaporation. Notice the thinning metal at the supports caused by the non-conformal coating that comes with evaporation.

Figure 10: Scanning electron micrograph of an air bridge that was misaligned. Notice the outward projecting lip gives the bridge extra support. This micrograph can be compared to Figure 11 that shows the same bridge but from the other side.
Figures 10 and 11 are an excellent example of the importance of alignment on the structural integrity of air bridges by showing a misaligned air bridge from both sides. Looking closely at Figure 10 shows a slight outward overhang, relative to the picture, and only a slight dip in the bridge towards the center span. When looking at the same bridge from the other side, as shown in Figure 11, it is observed that the same outward overhang is not present and the bridge is partially, though not fully, collapsed. The overhang present in Figure 10 and not present in Figure 11 is due to a misalignment of the masking resist layer resulting in a bridge with a span slightly off center. The extra support from the overhang on one side of the bridge allows the bridge extra strength while the lack of an overhang on the other side weakens the structure. Better alignment or a bridge with wider dimensions, compared to the support post width, is needed to evenly distribute to the span giving stronger bridge.

Figure 12 shows an early sample that used acetone to remove the underlying layer of resist at the end of the fabrication process. Residual resist can clearly be seen underneath the bridge span indicating that acetone was not a viable solution to the resist stripping problem. These micrographs called for the experimentation for more aggressive oxygen plasma etch in order to remove the photoresist at the end of the developed process. Concerns of damaging the air bridges by ashing the wafers at the end of fabrication were wrong as all samples imaged other than that shown in Figure 12 survived the ashing process.

Figures 13 and 14 show the results of damage to the aluminum film due to out-gassing of solvents after deposition. These images were taken from the image reversal sample where a “high” temperature post exposure bake is needed to cause the image reversal effect in AZ5214E-IR™ resist. Figure 13 shows that out-gassed solvents slightly raised the metal film close to the left support. An expanded view of that support posts show a break in the support producing a weakened structure.
Figure 15: Scanning electron micrograph of the “perfect” air bridge.

Contrary to the images shown in Figures 13 and 14, the image reversal process has appeared to produce the best air bridges as seen in Figure 15. Though several factors could have played a role in the “perfect” fabrication of the air bridges seen in Figure 15, including better alignment, the results from this image indicate the need for further investigation into the use of AZ5214E-IR™ resist for fabrication of air bridges.

VI. CONCLUSIONS

Based on the process development process undertaken during this project the following process parameters were found to be optimal in fabricating air bridges at RIT’s SMFL:

1. Etch alignment marks into substrate. Alignment keys for second level lithography may be loss due to the thickness of the films placed above alignment keys.

2. Coat wafer for with Shipley 812™ for 1st Level lithography Wafer coated on SVG88 Wafer Track, coat line using Recipe (1,1,1) with soft bake temperature set to 115°C.

3. 1st Level lithography done on GCA6700 g-line stepper. Exposure time is dependent on starting substrate, but for silicon substrate an exposure time of 0.45 sec is recommended. This exposure time may change the after the next scheduled bulb change on the stepper or as the bulb reaches the end of its usable lifetime.

4. Exposed wafer is developed on the GCA88 Wafer Track, develop line using recipe (1,1) and a hard bake temperature of 125°C.

5. Metal is then deposited on top of patterned wafers. Sputter deposition is the preferred deposition method since it provides a more conformal coat, critical in creating stronger supports, and heating during the deposition sequence could further round the resist profiles (this has not been determined). Limitations of the evaporation tools at SMFL will require sputter deposition for film thicknesses greater than 7000Å.

6. Wafer is prepared for 2nd Level lithography. Wafer is recoated with Shipley 812™ resist using the SVG88 Wafer Track, coat line. Recipe used is (5,1,1), no

HMDs prime is used to prevent hardening and out-gassing of the first layer of resist. Soft bake temperature is reduced to 105°C.

7. Exposure is done on GCA6700 g-line stepper. Recommended exposure time for aluminum is 0.95 sec though, as with 1st level lithography, this exposure time may need to be optimized from time to time.

8. Wafer is developed after exposure using SVG88 Wafer Track, develop line using recipe (1,1). No hard bake is used in this develop step due to limited thermal budget.

9. Wafer is then etched using Aluminum Wet Etch Bench with bath temperature set to 50°C. For smaller bridge widths an anisotropic etch using the LAM4600 may be needed. This was not tested because the tool was down, but indications from process development showed that undercutting from the isotropic wet etch process caused the loss of the 2μm width bridges in a majority of the fabricated samples.

10. Resist is removed using the Branson 3200 Oxygen Plasma Asher. Recipe used was the 4th Hard Ash Recipe. Acetone proved to a bad process for resist stripping, but may be a viable solution using ultrasonic agitation. This will have to be investigated further.

A baseline process was developed for fabricating air bridges using SMFL’s g-line lithography tools. The process proved to be a robust process for fabricating air bridges producing air bridges that spanned distances greater than 50μm with both thin and thick metal films. Further optimization of the process could be done by investigating the use of AZ5214E-IR in both image reversal and positive tone as initial results show that this resist process has promise in fabricating air bridges. Other metals can also be used in air bridge fabricate and require further study before implementing into the developed process.

ACKNOWLEDGEMENTS

The author thanks Dr. S. Rommel as advisor for the project, Dr. K. Hirschman, Dr. S. Kurinec, and Braniislav Curanovic for their help and advice throughout this project. Also Charles Gruener for the mask set used in development, Sean O’Brien for process information, and the entire SMFL Staff. Finally special thanks to NSF for the LEO EVO50 SEM (Grant #0320869).

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Jay Cabacungan, originally from East Harlem, New York City, received a BS in Microelectronic Engineering from RIT in May 2004. He attained co-op work experience at SMFL working on developing an image reversal process and with RIT’s Electrical Engineering Department developing thin film ultrasound calibration targets. He plans to complete his co-op requirement at SMFL under the supervision of Dr. S. Rommel and continue his education at RIT by obtaining a Masters in Microelectronic Engineering with an interest in device physics and lithography.
Design and Fabrication of a Micro-size Thermionic Ionization/Flame Ionization Detector for Gas Phase Chemical Analytes

Robert Manley, Student Member, IEEE

Abstract—A simple, MEMS base micro-chemical detector utilizing the principles of gas ionization, has been designed and fabricated. The device contains a polysilicon micro air-bridge heater structure with integrated polysilicon electrodes. The design of the devices allows it not only functions via thermionic emission, but also via chemi-ionization if a proper Pt catalyst is applied and it is operated in an environment containing hydrogen.

When properly biased the device has been shown to heat to high temperatures where thermionic emission can begin to occur. Hydrocarbon chemicals in the gas phase have shown to ionize, via thermionic ionization and have been collected, producing a measurable current signal.

Index Terms—Chemical detection, gas chromatography, ionization, MEMS, micro-heater, sensor.

I. INTRODUCTION

The need for portable chemical detection has grown more important in our world today. A device that is sensitive to multiple chemical analytes is important when analyzing unknown substances and would be useful in national security, detective forensics or the food and health industry. MEMS based technology has made such sensor feasible to fabricate.

The design, fabrication, and testing of a micro-sized gas phase chemical detection sensor that can operate either via thermionic emission or flame ionization has been designed and fabricated. The thermionic ionization detector (TID) or flame ionization detector (FID) could be used in portable chemical detection systems, involving gas chromatography. A micro-size sensor of this sort requires less power while possibly providing nearly the same sensitivity of chemical detection as compared to its conventional, macro-sized counterparts. Also, the development of such a device, using silicon-based micromachining techniques, shows the feasibility of a mass production of the sensor.

The two modes of the sensor are similar in operation. The TID operates under the principles that when a filament is heated to high enough temperatures, thermionic emission of electrons will occur. When in the presence of a gas analyte the properties of the emission will change, causing ionization, creating a detectable signal. Coatings or catalyst can be used to change the sensitivity of the device. Typical the TID is most sensitive to nitrogen or phosphorus containing compounds. The FID works in the presence of air and hydrogen. When the heater filament is coated with a catalyst, an oxy-hydrogen flame is produced. When gaseous analytes pass through this flame, they are ionized. The ions are then collected by the electrodes producing a measurable signal. Because of the oxy-hydrogen flame FID is extremely sensitive to hydrocarbons.

II. GAS CHROMATOGRAPHY

Gas chromatography (GC) is the method use to separate gaseous mixtures. A GC process of separations is typical some sort of column, often a glass capillary, which a gaseous mixture flows through. Three main factors determine the separation of a mixture: column length, time, and a molecules affinity to the column material (the stationary phase). The molecules affinity will actually cause the separation. Its affinity is how well the molecule adsorbs and desorbs for the column walls. The column length and time which the molecule passes through the column will help to separate the distance between the species and the leave the column, allowing for more discrete detection. Often times these column walls are coated with a film or pack with beads to help to change the affinity properties.

By speeding up the separation process the peaks of the GC output will not be as defined. The spread of the peak will be larger and overlap with other molecules in the mixture. Thus, a fast response detector is required; if the high speed chromatography is to be done.

III. THEORY

A. Thermionic Ionization Detector (TID)

When a material is heated to very high temperatures, enough energy can be imparted to cause emission of electron. Because of the large amount of thermal energy, surface molecules, on
the heated substance, may absorb that energy and use it to emit an outer shell electron. Thermionic emission current is governed by several parameters, including temperature, \( T \), work function or ionization potential of the material, and a emission constant, \( A \) (Richerson’s constant).

\[
J = AT^2 e^{-\frac{q}{kT}}
\]

(1)

If a gaseous analyte is in the presence of a hot surface that is emitting electrons via Thermionic emission, it can be ionized. The emitted electrons can collide with the analyte, removing an electron. In order to do this, the electron emitted must have a higher energy than the binding energy that is holding the electron on the analyte molecule.

Thermionic ionization may also occur of a gaseous analyte via other mechanisms. If the temperature is high enough, a molecule brought into the presence of the high temperature may self ionize. Essentially, the larger amount of thermal energy will be adsorbed by the molecule, causing it to emit an electron.

Once an analyte is ionized, it has net charge associated with it, making it susceptible to an electric field. Thus, if the ionized molecule is in-between to electrodes, one with a bias, a force can be imparted on it. On of the plates can be left floating and used for collection. Depending on the bias on the other electrode, electrons or ions can be forced to the collection electrode. This creates an ionic current which can be measured. As GC eluents become present to the detector, they become ionized and the biased electrode forces the ionized gas to a collector creating ionic current. This current can be measured, denoting a signal of a chemical species being present. Figure 1 shows the general schematic of the TID.

The longer the ions take to reach collector electrode, the more recombination takes place. Thus, the greater the distance the electrodes are from one another, the lower the voltage produced for signal (Ref. [1]). The applied voltage needs to be adjusted depending on electrode spacing. Performance is not necessarily improved or comprised because electrode spacing as long as the voltage is adjusted.

Though theoretically the TID can detect any gaseous chemical substance if enough energy is present, it is typically most sensitive for hydrocarbons, nitrogen, and phosphorus containing compounds.

An alternate mode of the TID is the flame ionization detector. It works on the same principles as the TID, but the method of ionization differs. If the heat source of the of the TID is coated with platinum or a platinum base coating and put in the presence of a hydrogen ambient, catalytic combustion will occur. If a GC eluent is passed through the combustion zone, ionization of that species will occur. This mechanism is know as chemi-ionization. This form of ionization is very sensitive to hydrocarbons. This is the result of the reaction of CH with O as shown below:

\[
\text{CH} + \text{O} \rightarrow \text{CHO}^{*} \rightarrow \text{CHO}^{+} + \text{e}^{-}
\]

The FID is characterized as having very high sensitive of these types of molecules and a working range of many orders of magnitude.

IV. DETECTOR DESIGN AND FABRICATION

For the detector design, MEMS surface micromachining techniques were incorporated to fabricate a simple micro polysilicon air-bridge heater filament with integrated polysilicon electrodes. The heater was design to operate at relatively low voltages, around 15 to 20 V and produce temperatures upwards of 900°C. Electrode spacing from the heater varied from 50 to 500 \( \mu \)m. Spacing was arbitrarily chosen because biasing would determine collect of the ions. Aluminum was used for contact to the polysilicon.

Fabrication of the device consisted of three mask levels. First a LPCVD SiN\(_x\) film was deposited to create an insulating barrier from the silicon substrate. Then 3\( \mu \)m of PECVD oxide was deposited and patterned. This layer is used as the sacrificial layer. Two microns of LPCVD polysilicon was then deposited.
and doped using N-type spin-on-glass. Aluminum was deposited on top of the polysilicon and patterned with the heater and electrode structures. The aluminum was used as a hard etch mask to etch the polysilicon in RIE plasma system. The remaining aluminum was then pattern and etch to form contacts on the polysilicon heaters and electrodes. Finally the structures were released in a 49% HF etch.

Because the heaters were 3mm long, they often stuck to the surface after release. This was due to capillary forces from the rinse after the release. To alleviate this problem, a DI water / IPA / DI wafer / IPA rinse was incorporated followed by a 200°C bake on a hot plate to suspend the structures.

![Figure 3: Fabricated straight filament micro-heater with integrated electrodes. The filament is 3000μm by 300μm. The electrodes are 100μm from the heater. The dimensions of the die are 4.5mm by 6.5mm.](image)

V. TEST SETUP

A. Thermal Characterization

Once suspended structures were fabricated, thermal characterization was performed. This was done by measuring the change of resistance of the heater structures on with temperatures. Resistance was measured at various temperatures ranging from 20 to 325°C.

![Figure 4: Change in resistance versus temperature. Fluctuation in the resistance is due to both increased number of intrinsic carries and thermal expansion of the polysilicon.](image)

Resistance of 300μm Structure at Given Temperature

Resistance (Ω)

- Micro-heater 1
- Micro-heater 2
- Micro-heater 3

Temperature (°C)

0 100 200 300

Figure 4: Change in resistance versus temperature. Fluctuation in the resistance is due to both increased number of intrinsic carries and thermal expansion of the polysilicon.

Normally resistance is expected to increase with temperature. However, both increasing number of intrinsic carriers in the polysilicon and thermal expansion seem to cause a "tug-of-war" effect with the structure resistance. This causes the resistance to go up and down with temperature.

From the resistance data, the temperature coefficient of resistance (TCR) was determined. The average TCR was found to be 0.000209/°C for the 3000 by 300μm structures. Using this value and applying a 46V bias across the heater, an estimated temperature of about 78°C was determined. The bias used was larger the original designed because the resistivity of the polysilicon came out higher during fabrication than originally assumed.

B. Pneumatic setup

The Pneumatic setup for introducing chemicals to the micro TID is shown below.

![Figure 5: Setup for introduce a chemical analyte to the device under test](image)

Nitrogen was used a carrier gas to introduce chemicals to the detector. A stream of approximately 100mL/min was used. Acetone was the analyte chosen for the chemical detection test. A swab, soaked in acetone, was inserted into the nitrogen stream and the vapors were carried to the device. The device was heat up to above 800°C and a 100V bias was applied to one of the electrodes. A HP4145 parameter analyzer was used to both apply the electrode biasing and to measure the ionic current produced.

VI. RESULTS

Using the above test setups, acetone analyte peaks were measured, which simulated the output of a gas chromatograph column. Results of the first run can be seen in the figure 6 below:
Detection of an acetone peak, in figure 6, shows that a micro-sized TID can be used for analyze detection. The shape of the peak is similar to that of what is typically found in conventional GC setups. The time the analyze was present for detection is indicated on the plot. The time difference of when the analyze was present and the time for signal has not to do with the speed of the detector’s response but rather the time it took for the chemical to reach the detector.

In figure 7, it is seen that a signal for acetone was repeated. However, what is interesting to note is that there is an initial signal in the beginning of the plot. This initial peak occurred when the micro-heater was activated by turning on the power supply. Surface contamination on the heater filament itself ionized, and was collected by the electrodes creates an initial peak. However, after a few moments of warm up is it observed that the signal did settle down. After the acetone signal, it is further observed that the background noise becomes less. This may be link to the further removal of the initial surface contamination. It may be necessary for a few moments of temperature stabilization by the device. This could be done by just cycle heat the filament momentarily then the heating to the desired operation temperature.

VII. CONCLUSION

Successful fabrication, using MEMS micromachining techniques, of a micro thermionic ionization detector utilizing a polysilicon, air-bridge heater with intergraded polysilicon electrodes was accomplished. The device was shown to reach temperatures above 800°C when biased properly. Using a nitrogen carrier gas, detection of a significant acetone signal was demonstrated. The many signals attained had very similar characteristics to those attain from a conventional gas chromatography detector having a sharp rise and slightly slower fall off.

Further work will include demonstration of detection of multiple peaks when the detector is utilized with a gas chromatograph and to determine the lower detectable limit of the TID.

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Robert G. Manley, originally from Towanda, PA received a B.S. in Microelectronics Engineering in May 2004, from the Rochester Institute of Technology. He has attained work experience at Integrated Nano-Technologies, Rochester, NY, in the area of MEMS based DNA detection systems and at Sandia National Laboratories, Albuquerque, NM, in the area of MEMS based micro-analytical systems. He is currently pursuing a M.S. degree in the area of Microelectronics Engineering at the Rochester Institute of Technology with an interest in Microsystems and systems-on-a-chip.
Fabrication and Characterization of a Packaged MEMS Gas Flow Sensor

Vee Chee Hwang

Abstract—A surface micromachined MEMS gas flow sensor has been fabricated and tested. The fabrication process of the device was presented. The heater glowed red hot when a voltage of 27V was applied if the underlying LTO was completely etched away. Both the upstream and downstream resistors changed when temperature changed. A proof of concept showing that output voltage changes with gas flow was shown.

Index Terms—MEMS, LTO.

I. INTRODUCTION

Gas flow sensors are required to monitor and control the amount of gas going into wafer fabrication machines such as the Bruce Furnace and the Dry Tech Quad. The resistance differential gas flow sensor uses the principle that the gas flow will change the temperature of the resistors, hence their resistance values. A heater strip is used to cause a temperature difference between the upstream and downstream resistors. The sensor will be manufactured on the surface of a 5mm by 5mm silicon chip and does not require special fabrication tools.

The gas flow sensor consists of a heater strip and 2 resistors that act as temperature sensors (one upstream and one down stream) shown in Fig 1. Fig 2 shows the cross-section of the gas flow sensor. The heater strip and the resistors are suspended to prevent temperature loss to the substrate. A tube is attached to direct the gas to flow across the 2 resistors and heater. When there is no gas flow, the resistors will be at the same temperature and there will be no change in the resistors values. When there is gas flow, the downstream resistor will be at a higher temperature, causing an increase in the resistance value of that resistor, and the upstream resistor will be at a lower temperature, causing a decrease in the resistance value of that resistor.

By connecting the 2 resistors of the gas flow sensor to a Wheatstone bridge or potential divider (+6V to -6V) circuit and measuring the output voltage, the gas flow speed can be characterized. A constant heater circuit will be required to supply constant power to the heater so that the heater would not be cooled by the flowing gas.

II. DESIGN AND FABRICATION

3 lithography mask layers were used to fabricate the gas flow sensor. There are 16 different designs in the 2nd level mask and the masks were designed by students of EMCR890 (MEMS) in spring 2003. The length of the heater (800 um) and resistor (700 um) are identical for all designs. However, the width of the heater and resistor, and the gap between them varies. A list of some of the gas flow sensor design is shown in Table 1.

<table>
<thead>
<tr>
<th>Design</th>
<th>Gap (um)</th>
<th>Width (heater) (um)</th>
<th>Width (resistor) (um)</th>
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<tr>
<td>1</td>
<td>10</td>
<td>100</td>
<td>10</td>
</tr>
<tr>
<td>2</td>
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</tr>
<tr>
<td>3</td>
<td>8</td>
<td>100</td>
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</table>
A 4-inch silicon wafer was used to fabricate the devices. The quality of the wafer does not matter since a layer of insulating nitride will be deposited on top of the silicon substrate, and the substrate will not be used during device operation. Reclaim wafers, which were used to check the coating uniformity of the coater track, were used to manufacture the gas flow sensors.

After a RCA (Radio Cooperation of America) clean, a 3500A of silicon nitride was deposited on top of the silicon substrate using Low Pressure Chemical Vapor Deposition (LPCVD). This layer serves as an insulating anchor point for the two resistors and heater strip. Next, a 3um sacrificial low thermal oxide (LTO) was deposited. This sacrificial oxide will create the suspended resistors and heater strip once it is etched away at the last processing step. The first level lithography was performed on a g-line stepper. Unwanted LTO were etched away to form the release layer for the heater and resistors. A 2um LPCVD polysilicon layer was deposited and doped with N-250 spin on dopant. This layer will eventually become the two resistors and heater. 7500A of aluminum was sputtered. This aluminum will protect the underlying polysilicon during polysilicon etch, and will form the contact pads for the probes during electrical test.

2nd Level lithography was performed and the aluminum and polysilicon was etched away to form the 2 resistors and heater. After the polysilicon etch, a short test was conducted using a multimeter to check if polysilicon was completed removed. 3rd Level lithography was performed and the aluminum on top of the suspended resistors and heater strip was etched away. The wafers were diced and the sacrificial oxide on the diced gas flow sensor was etched away in 49% HF to form the air-bridge effect. The photoresist was removed in acetone and the device was ready for electrical test. Fig 3 shows the cross-sectional view of the processing steps. Fig 4 shows a photo of a finished gas flow sensor.

### RESULTS

A cross-sectional Scanning Electron Microscope (SEM) picture shown in Fig 5 was taken to check for the release of the heater and 2 resistors after the 49% HF etch. A multimeter was used to measure the resistance across the heater and 2 resistors after the release. The aluminum contact pads were unintentionally etched away during the air-bridge formation due to undercutting. However, electrical test could still be conducted on the underlying polysilicon.
After the heater and resistors were released, the structural integrity test was conducted on the device by blowing air across the gas flow sensor. It was observed that gas flow sensors with a resistor width of 10um suffered from poor structural ruggedness as shown in Fig 6. Gas flow sensors with a resistor width of 20um had a good structural integrity as shown in Fig 7.

When a voltage of 27V was applied across the heater, the heater started to glow red hot as shown in Fig 8. If the heater is not completed released, the heater will not be red hot since heat will be conducted to the substrate via the LTO, which has a thermal conductivity of 0.014Wcm⁻¹K⁻¹. Released heater also caused a bigger change in the resistors values compared to non-released heaters as shown in Fig 9. This is because released heaters are hotter and require less voltage to make it hot. However, it is not necessary to make the heater red hot as long as the heater could cause a substantial change in the resistors values.

Fig. 5. Cross SEM photo showing air-bridge formation

Fig. 6. 10um wide resistors, showing bending after LTO etch

Fig. 7. 20um wide resistors, showing no bending after LTO etc.

Fig. 8. 50um wide heater glowing red hot when a voltage of 27V was applied.

Fig. 9. Device VC7 heater was completed released, while device D9.1 heater was not. This shows that released heater caused a bigger change in the resistor values and required less applied voltage.
Fig 10 shows the increased in resistors values when a constant voltage of 33V was applied. The resistor value increased by 40 ohms within 15s, and stabilization time for the resistor value was 5 minutes. When a nitrogen flow of 6 lpm was flown, the upstream resistor value decreased by 20ohms over a period of 2 minutes as shown in Fig 11. By arranging the upstream and downstream resistors as shown in Fig 12, the output voltage can be calculated as shown in (1)

\[ V_{out} = \frac{(R_2 - R_1)6V}{(R_1 + R_2)} \]  

(1)

When there was no gas flow and the heater was on, the resistors values were identical (8.508k-ohms) and the output voltage was zero. When 6 lpm of nitrogen was flowing, the output voltage was 2.83mV. This is shown in table 2.

![Upstream Resistor Response](image)

**Fig. 11.** Upstream resistor response to 6 lpm nitrogen flow

**Fig. 10.** Resistor stabilization time

<table>
<thead>
<tr>
<th>Table 2</th>
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<tr>
<td><strong>Calculated output voltage vs Gas flow</strong></td>
</tr>
<tr>
<td>Gas Flow</td>
</tr>
<tr>
<td>0 lpm</td>
</tr>
<tr>
<td>6 lpm</td>
</tr>
</tbody>
</table>

**IV. CONCLUSION**

A surfaced micromachined MEMS gas flow sensor has been fabricated and tested. Both the heater and resistors worked...
after the LTO was etched away. The heater glowed red hot when a voltage of 27V was applied if the underlying LTO was completely etched away. However, it is not necessary for the heater to become red hot for the gas flow sensor to work. Both the upstream and downstream resistors changed when temperature changed. A proof of concept showing that output voltage changes with gas flow was shown. For more accurate measurements, the gas flow sensor has to be packaged so that detailed testing could be conducted.

APPENDIX

See Appendix A for detailed processing steps.

ACKNOWLEDGMENT

The author would like to thank his advisor Dr Lynn Fuller for his valuable advice for this senior project. The author would also like to thank Robert Manley and Mike Aquilino for their assistance and the staff of RIT SMFL for their technical support.

REFERENCES


Vee Chee Hwang is from Singapore and has obtained a diploma in Electronics and Computer Engineering from Ngee Ann Polytechnic, Singapore, in 1999. He will be receiving his B.S degree in Microelectronic Engineering and a Minor in Japanese Language from Rochester Institute of Technology in 2004.
Fabrication of Polysilicon Micro Valve Array

Jermaine White

Abstract: Valves are an essential part of pumping systems, which are used in a wide variety of applications including medical, automotive, gas sampling, and gas analysis. The objective of this investigation is to design and fabricate microvalve arrays. The valve consists of a polysilicon flap suspended over a through hole in the silicon. It is intended to allow airflow in one direction and inhibit airflow in the reverse direction.

The design requires only three mask levels, two on the front of the wafer and one on the backside. The front side masks are level: 1 Anchor and level 2: Flap. The backside mask is Holes. Backside alignment was achieved by placing shims between the Anchor and Holes masks, aligning the two masks to each other, and clamping them together. A double-sided polished wafer was resist coated on both sides and slipped between the two masks. Both sides were exposed using a flood exposure from a broadband mask aligner. The backside holes were masked by thermal oxide and etched using a 40% weight heated KOH solution. The wafers were diced and the valves were released.

I. INTRODUCTION

The advent of the microchip has made possible the physical reduction of almost every electronic device that followed. Through MEMS technology, mechanical devices are also being reduced in physical dimensions. Some of the most common MEMS devices range from accelerometers that deploy automobile airbags to gas flow and pressure sensors with a wide range of applications. Mechanical valves are essential parts of pumping systems that permit flow in only one direction. A simple mechanical flap valve is a device that allows flow (liquid or gas) in only one direction. Using bulk micromachining techniques, it is possible to fabricate a miniature version of this device. It would consist of a polysilicon flapper over a hole in the silicon. The hole sizes will be on the order of tens of microns and the same flow principles would apply as in the macro-sized device. The valve can be modeled as an orifice flowmeter allowing theoretical flowrate calculations to be made.

II. THEORETICAL MODEL

Flow through the valve would be most similar to flow through an orifice, which is governed by the following equation.

\[ Q = C_f A_o \sqrt{\frac{\Delta P}{\rho}} \]  

Where \( A_o \) is the area of region 1 in figure 1, \( \Delta P \) is the pressure difference between regions 1 and 2, \( \rho \) is the mass density of the fluid or gas, and \( C_f \) is the flow coefficient. \( C_f \) is experimentally determined and ranges from 0.6 to 0.9 for most orifices.

For this model, the valve will be oriented such that the back of the valve is toward region 1 in figure 1. The flap will partially obstruct flow, but it will be analogous to a sheet of paper over a hole and its effects on flow in the forward direction are negligible.
III. DESIGN

The flap will be approximately 2µm above the silicon and 2µm thick. When air pressure is applied to the backside, the flexible flap will bend up and allow airflow. When air pressure is applied from top surface, the flap bends down and closes the hole thus preventing airflow (see figure 2). Since the flap is intended to bend with operation, the effects of stress must be taken into account. The maximum stress on the flap will occur at the corner where it bends. The yield strength for polysilicon is about 1.2x10^6 Pascal. This value will be used as the upper pressure limit in equation (1) to estimate a theoretical maximum flowrate.

![Figure 2: 3D cross sectional view of conceptual valve.](image)

The design consists of three mask layers: Anchor and Flap (Front) and Holes (Back). It was decided to design for 1X masks because stepper systems often have Depth Of Focus issues when having to expose wafers with several microns of topography, as will be the case here. Thick films also cause stress on the wafer resulting in a deformed "potato chip" shape that makes it difficult for the stepper’s vacuum chuck to handle.

The through holes will be etched using a heated Potassium Hydroxide (KOH) solution. Assuming (100) wafers are used, KOH etches silicon along the (111) plane at a 54.7° angle to the surface. Given this angle and the wafer thickness, basic trigonometry was used to calculate the required hole size on the backside of the wafer to obtain the desired hole size on the front of the wafer. The design allows for four valve array types each with a different hole size ranging from 25µm x 25µm to 100µm x 100µm. The flap in each design completely covers the hole with an overlap of 75 µm. Top view schematics of the array and individual valve are shown in figures 3 and 4 respectively.

![Figure 3: Mentor Graphics layout of valve array.](image)

![Figure 4: Individual valve dimensions.](image)

Packaging consists of bonding a 4mm tube to each side of the die completely enclosing the valve array and holes. One end of the tube will be placed in an inverted, water filled, graduated cylinder. As air is forced through the valve and into the cylinder, water will be displaced. The flowrate will be the displaced liquid volume per unit time. The tubes will then be switched and the test performed again.
IV. PROCEDURE

Double sided wafers were required for this project but none were available so CMP was performed to polish the backside of the process wafers. The lot was washed and an RCA clean was performed before an oxidation step. The desired thickness was 3µm of oxide but recipe 430 on Bruce furnace yielded 2.5µm of thermal oxide. Next the wafers were coated on both sides with Shipley 1812 photoresist. All resist coating was done using the hand spinner and all development was done manually. To pattern the oxide, first level and backside lithography was performed by aligning those two masks to each other, clamping two ends together, slipping the wafer in between and flood exposing on the Karl Suss mask aligner. The oxide was then etched and an RCA clean was performed before depositing 2µm of polysilicon via LPCVD. Assuming a deposition rate of 235Å/min the run was done for the time needed to obtain 2µm of poly. A groove and stain was done on a control wafer after the poly deposition. Only 1.8µm of poly was deposited.

Next, the front sides of the wafers were doped n-type using spin on dopant N-250 and placed in Bruce furnace tube 3 running recipe 115. This was done to relieve stress from the film that might have occurred during deposition. The spin on glass was removed using a buffered oxide etch and a sheet resistance of 14 points per wafer was measured on the ResMap. The average measurement was around 33Ω/. The backside poly was then removed using the LAM490. About 7µm of AZ9260 was coated on the front side and second level lithography was done using the Karl Suss Mask Aligner. With such a thick masking layer, the front side poly was patterned on the LAM490 without having to worry about over-etching. Recipe 4inPoly was used for the poly etch.

A diamond like carbon film was deposited on the front side of the wafers using PECVD on the Drytech Quad. The recipe requires 45 sccm of CH₄ at a pressure of 50mTorr and a power of 200 Watts. Next, the through holes were etched in a 40% wt KOH solution heated to 72 degrees. These conditions result in a silicon etch rate of 40µm/hr and an oxide etch rate of 0.2µm/hr [4]. The wafers were etched for 12 hours and carbon film was removed with an O₂ plasma using the LAM490. Finally the release was done in BOE for 4 hours. Figures 5a and 5b summarize the process steps discussed above.

Figure 5a: Process Flow
V. RESULTS & DISCUSSION

Several issues occurred during the KOH etch that made it impossible to test the devices. The first problem occurred when the KOH solution undercut the oxide etch mask separating the holes in the array. This resulted in one large hole being etched to the surface. The partial merging of the etch holes is illustrated in Figure 6. The second problem was that adhesion issues with the carbon film resulted in the front side poly on some wafers being etched away.

A greater separation distance between the holes may have prevented the etch mask undercut. Using a nitride film as an etch mask would have been better since nitride has a very low etch rate in KOH on the order of angstroms per hour. The down side to using nitride is having to incorporate additional process steps.

An improved process would involve the through etch being done with a deep trench plasma etcher. It would offer the following benefits over the KOH etch:

1. Significantly shorter etch time
2. Greater packing density
3. More control over through hole size
4. Avoid need to align to cryptographic planes
5. Avoid need for backside alignment if holes are etched first

This improvement would require a redesign of the photo masks. The front side masks could still be used but the holes mask will have significantly smaller openings.

VI. CONCLUSION

Key flaws with the valve design came to light after the KOH etch. Had a nitride mask layer and greater hole separation distance been used in the project, it might have been successful. A complete redesign for a deep trench etcher would also significantly reduce processing time. This would give the flexibility to make changes to the planned procedure if unforeseen problems arise.

VII. ACKNOWLEDGEMENTS

The author would like to thank Dr. Lynn Fuller for his guidance and assistance on this project. The author would also like to acknowledge Sean O’Brien and the RIT Semiconductor and Microsystems Fabrication Laboratory staff for technical assistance and equipment support. Special thanks are also extended to everyone that assisted on this project.

VIII. REFERENCES


Abstract— A solar cell array to power a on board micro-
electromechanical polysilicon cantilever actuator was designed, 
fabricated and tested. The device composes of two solar cell 
arrays one array with 330 solar cells and another array with 300 
solar cells. The device also consists of several cantilevers. The 
fabrication process involved over fifty process steps including 
ine photolithography levels. To optimize the performance of 
the solar cell array the entire process was simulated using 
SILVACO SUPREM simulation software. Electrical 
examination using ATLAS software allowed for parameter 
extraction of the computer-generated solar cells. Modeling the 
extracted parameters with device physics equations allowed for a 
SPICE level-2 analysis that could be verified through electrical 
testing of the actual fabricated solar cells. Measurements were 
taken throughout the fabrication process. The completed devices 
were tested and pictures were taken of the cantilevers and solar 
cell array.

Index Terms—solar cell array, polysilicon cantilever actuator, 
Silvaco Suprem, Atlas.

I. INTRODUCTION

The purpose of this project is to investigate the possibilities 
of using a bulk silicon solar cell array as an on-board power 
source for electrostatic MEMS devices. To demonstrate the 
solar cell array as an on-board power source, an electrostatic 
polysilicon cantilever actuator will be fabricated and powered 
by the array.

The devices were fabricated on four inch P-type wafers with 
a resistivity of 5-15?/cm. Each die contains two solar cell 
arrays. The major solar cell array will consist of 330 solar cells 
connected in series to generate a final voltage of 99 volts. The 
minor solar cell array will consist of 300 solar cells connected in 
series to generate a final voltage of 90 volts. The difference in 
the two arrays is to test different cantilever devices as well as a 
protection plan incase the major array produces more voltage 
than 150 volts. The array is broken into several rows 
comprising of 30 solar cells per row. Each row will have a 
different aluminum contact design over the solar cell. This will 
help determine the optimal conditions for the solar cell array. 
The voltage generated will be used to create an electric field 
that will force the polysilicon cantilever actuator to move two 
microns towards the silicon.

The solar cells and polysilicon cantilever actuator will be 
fabricated simultaneously on a P-type silicon wafer. To help 
sure success of the project, the process of the device was 
simulated using Silvaco Supreme a microelectronic device 
simulator. The simulation helped in determining times and 
temperatures of key process steps as well as simulated result 
for current and voltage that could be compared with the 
fabricated array. During the fabrication of the device the 
process flow changed.

II. MOTIVATION

In today's fast growing micro-electromechanical systems 
(MEMS) industry self-contained power supplies are necessary. 
The power requirements of micromachined devices are very 
different from conventional circuits. Many devices need large 
amounts of voltage to create forces and use external power 
connections. For many MEMS devices, this conventional 
method is preferable, but for some operations, like space-based 
MEMS or free-moving microrobotic systems, a self-contained 
on-board power supply is desirable.

III. THEORY

Solar cells directly convert light into electricity, and use 
similar physics and technology as that used in the 
microelectronics industry. The direct conversion of sunlight 
into energy using solar cells is called the photovoltaic effect. 
The word photovoltaic is a combination of the Greek word for 
light and the name of the physicist Allesandro Volta. The 
conversion process is based on discovery by Alexander 
Bequerel in 1839. The photoelectric effect describes the release 
of positive and negative charge carriers in a solid state when 
light strikes its surface.

The first step in the conversion of sunlight into electricity is 
the absorption of light. The absorbed light causes electrons in 
the material to increase in energy, at the same time making them 
free to move around in the material. However, the electrons 
remain at this higher energy for only a short time before 
returning to their original lower energy position. To collect the 
carriers before they lose the energy gained from the light, a pn 
junction is typically used.

A pn junction consists of two different regions of a 
semiconductor material, with one side called the p-type region
and the other the n-type region. In p-type material, electrons gain energy when exposed to light but also readily return to their original low energy position. However, if they move into the n-type region, then they can no longer go back to their original low energy position and remain at a higher energy. The process of moving a light generated carrier from where it was originally generated to the other side of the pn junction where it retains its higher energy is called collection. To help better understand how collection works see figure one.

Once a light generated carrier is collected, it can be either extracted from the device to give a current, or it can remain in the device and give rise to a voltage. For this project it is important to acknowledge that the voltage is weakly dependent on light radiation; it is the current intensity that increases with higher luminosity. In this project, the amount of current needed is negligible to the 100 volts that needs to be generated. The usable voltage from solar cells depends on the semiconductor material. In silicon it amounts to approximately 0.5 V. A lower voltage of .3v is going to be assumed for this experiment.

For this experiment a P-type wafer is used to isolate the N-type well and an inner P+ well. These wells are designed to always be biased positive with respect to the p-type wafer. This ensures that the pn junction that is formed is in forward bias, and there is no current leaking to the substrate. Current will flow from the P+ region to the N+ region and then over the aluminum to ground. The electric field will travel in the opposite direction. The I-V characteristic follows Ohm’s Law: $I = \frac{V}{R}$. See figure two for a visualization of the solar cell array.

In order to make the appropriate voltages, single solar cells are interconnected to form larger units. Cells connected in series have a higher voltage, while those connected in parallel produce more electric current. The array in this project will consist of 330 solar cells connected in series to achieve a minimal voltage of 99 volts. Typical arrays are interconnected solar cells embedded in transparent Ethyl-Vinyl-Acetate, fitted with an aluminum frame and covered with transparent glass on the front side. The array in this project will have each of the solar cells embedded in the bulk substrate and connected with aluminum.

The level of efficiency expressed as ? indicates how much of the radiated quantity of light is converted into useable electrical energy. Increasing the level of efficiency will lower the costs of solar cells. However, different loss mechanisms set the limits. The theoretical maximum level of efficiency is approximately 28% for crystal silicon. Some of the loss mechanisms are optical losses, such as the shadowing of the cell surface through contact with the surface or reflection of incoming rays on the cell surface, electrical resistance losses in the semiconductor and the connecting cable, and the disrupting influence of material contamination, surface effects and crystal defects are significant. In this experiment the junction depths of the regions will be looked at to maximize the open circuit voltage of the circuit. Silvaco SUPREM simulation of the device will accomplish this. Also, the placement of the aluminum contacts will be varied to identify what finger pattern collects the most electrons.

Below are the equations used to determine the open circuit voltage (Voc) of the solar cells, the short circuit current (Isc) and the efficiency (?) of the solar cell. Voc is maximized by minimizing $I_0$.

$$V_{oc} = \frac{kT}{q} \ln \left( \frac{I_{sc}}{I_0} + 1 \right)$$  \hspace{1cm} (1)

$V_{oc}$ is the open circuit voltage $k$ is Boltzmann constant $T$ is the absolute temperature of the cell (K), $q$ is the charge of an electron, $I_{sc}$ is the short circuit current.

$$I = I_0 \left( e^{\frac{qV_{oc}}{kT}} - 1 \right) I_L$$  \hspace{1cm} (2)

$I_i$ is the light current generated current. $I_{sc}$ is at very low current densities. $I_0$ is dark reverse saturation current of the diode $I_0$ can range from $10^{-11}$ to $10^{-14}$ A/cm$^2$ and also equals equation three.

$$I_0 = \frac{q\mu_n D_n}{N_a L_n}$$  \hspace{1cm} (3)

$$L_n = \sqrt{D_n q_n}$$  \hspace{1cm} (4)

$$D_n = \frac{\mu_n kT}{Q}$$  \hspace{1cm} (5)

Solar cell efficiency (?) can be determined from equation six

$$I_n V_n = FF * I_{sc} * V_{oc}$$  \hspace{1cm} (6)
FF is a fill factor which is the optimal power setting which equals equation 7.

\[
FF = \frac{V_m \cdot I_m}{V_{oc} \cdot I_{sc}} \quad (7)
\]

The cantilever will move from the electrostatic forces. An electrostatic force is the force created by a voltage difference between two points. As the voltage between two points increases, the electrostatic force becomes more intense. By applying a voltage to the top of the cantilever a capacitance charge will build up and pull the cantilever toward the substrate actuating as ground.

The cantilever actuator is 150 micron long, 5 micron wide and 2 micron thick with stress relieving dimples. The cantilever actuator will move 2 micron down toward the substrate. Two microns was chosen because the movement can be easily observed under a microscope.

To determine the voltage necessary to move the cantilever actuator, first the mechanical force needed to move the silicon two microns must be found. This force is then used in order to determine the voltage. The equations below were used in determining the voltage necessary to move the cantilever.

The parallel plate capacitor is the most fundamental configuration of capacitive sensors. The definition of capacitance is given in equation eight. The \( C \) represents capacitance, \( Q \) is the stored charge, and \( V \) is the electrostatic potential.

\[
C = \frac{Q}{V} \quad (8)
\]

The stored electrostatic energy is expressed in equation nine.

\[
E = \frac{1}{2} CV^2 = \frac{1}{2} \frac{Q^2}{C} \quad (9)
\]

Neglecting the fringe electric field, the field lines are extended uniformly through the capacitor plates. According to Gauss's law, the magnitude of the electric field, \( E \), is related to \( Q \) by equation ten.

\[
E = \frac{Q}{\varepsilon A} \quad (10)
\]

Setting equations nine and ten equal to each other equation eleven is obtained. Equation eleven

\[
C = \frac{Q}{V} = \frac{\varepsilon A}{d} \quad (11)
\]

is the fundamental expression for the capacitance. The magnitude of the capacitance is related to the distance between the two surfaces and the area that overlap this distance. The equation is also a function of the electric permittivity, which is subject to many influences.

The electrostatic energy from the capacitance creates forces in many directions the magnitude of these forces can be expressed as equation twelve.

\[
F = \frac{\partial E}{\partial x} = \frac{1}{2} \frac{\partial C}{\partial x} V^2 \quad (12)
\]

In the equation \( x \) is the coordinate of interest. The force is perpendicular to the plates this and is the force that pulls the cantilever actuator to the substrate and the magnitude is expressed in equation thirteen.

\[
F = \frac{\varepsilon \varepsilon_0 AV^2}{2d^2} \quad (13)
\]

This force can now be compared to the physical mechanical force needed to move the cantilever. The equation will identify the force required to move a bar of a certain composition in one direction.

\[
F = \frac{Y_{max} 3Eb h^3}{12L^2} = \frac{\varepsilon \varepsilon_0 AV^2}{2d^2} \quad (14)
\]

In the equation above \( Y_{max} \) is the movement in the \( y \) direction, \( E \) is Young's modulus, \( b \) is the width of the cantilever actuator, \( h \) is the height of the cantilever actuator and \( L \) is the length of the cantilever actuator. The \( 3bh^3/12L^2 \) is determined from the inertia of a bar. It is understood that this is simplifying the cantilever actuator structure and because of the dimples less force will actually be needed to be to move the fabricated cantilever actuator. This equation was used as a safe guard to ensure that enough voltage will be applied to the cantilever actuator because the actual dimensions of the final cantilever structure will be unknown until fabrication is complete. The dimensions of the cantilever along with an estimated area between the surfaces to be 25 \( \mu m \) a voltage of 90.2 was determined.

Below is a visual representation of the cantilever actuator.
Figure 3: The green layer is the substrate, the blue is an oxide level, and the yellow is a nitride level. The nitride is needed as a dielectric to force the voltage applied to go the end of the cantilever and then to ground.

Silvaco SUPREM Simulation

To allow for optimal solar cell performance, the junction depth that is the length that the doped wells travels into the silicon substrate is critical. The doping travels into the silicon substrate by diffusion at high temperatures. For simple doping profiles, hand calculations can be used, but for complex process flows, simulation can give results with more accuracy.

**Doping Profiles**

![Doping Profiles](image)

**Electric Field**

![Electric Field](image)

**Processes Steps**

<table>
<thead>
<tr>
<th>Steps</th>
<th>Technical Info</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Scribe wafers</td>
<td>Use 4pt probe station</td>
</tr>
<tr>
<td>2. 4pt probe wafers</td>
<td></td>
</tr>
<tr>
<td>3. RCA Clean</td>
<td>Done in RCA bench standard process see appendix RCA</td>
</tr>
<tr>
<td>4. Grow 5000Å of oxide</td>
<td>Use Bruce Furnace</td>
</tr>
<tr>
<td>Step</td>
<td>Description</td>
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<td>------</td>
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<tr>
<td>5.</td>
<td>Measure using nanospectrometer</td>
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<td>6.</td>
<td>Deposit 3500 Å silicon Nitride</td>
</tr>
<tr>
<td>7.</td>
<td>Measure using nanospectrometer</td>
</tr>
<tr>
<td>7.</td>
<td>1st Lithography</td>
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<tr>
<td>8.</td>
<td>Etch Nitride layer</td>
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<td>9.</td>
<td>Strip resist</td>
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<td>10.</td>
<td>2nd Lithography for N well (Base)</td>
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<td>11.</td>
<td>Etch Oxide</td>
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<td>12.</td>
<td>Base Implant</td>
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<tr>
<td>13.</td>
<td>Strip resist</td>
</tr>
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<td>14.</td>
<td>Etch Oxide</td>
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<td>15.</td>
<td>RCA Clean</td>
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<td>16.</td>
<td>Base Drive in and 500 Å oxide growth</td>
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<td>Deposit oxide</td>
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<td>18.</td>
<td>3rd Lithography for N+ region for Omic contact</td>
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<td>19.</td>
<td>Etch Oxide</td>
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<tr>
<td>20.</td>
<td>Implant for Omic contact</td>
</tr>
<tr>
<td>21.</td>
<td>Strip resist</td>
</tr>
<tr>
<td>22.</td>
<td>Remove oxide</td>
</tr>
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<td>23.</td>
<td>RCA Clean</td>
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<td>24.</td>
<td>Deposit oxide</td>
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<td>25.</td>
<td>4th lithography create dimples in cantilever</td>
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<tr>
<td>26.</td>
<td>Etch into Oxide to make dimples</td>
</tr>
<tr>
<td>27.</td>
<td>Strip Resist</td>
</tr>
<tr>
<td>28.</td>
<td>5th lithography anchor window and removal of oxide for P+ emitter in solar cell array and high voltage break down stop.</td>
</tr>
<tr>
<td>29.</td>
<td>Etch Oxide for anchor and P+ Emitter</td>
</tr>
<tr>
<td>30.</td>
<td>Strip Resist</td>
</tr>
<tr>
<td>31.</td>
<td>RCA CLEAN</td>
</tr>
<tr>
<td>32.</td>
<td>Dope P+ silicon</td>
</tr>
<tr>
<td>33.</td>
<td>Deposit 2 um Polysilicon</td>
</tr>
<tr>
<td>34.</td>
<td>Dope N+ Polysilicon</td>
</tr>
<tr>
<td>35.</td>
<td>6th lithography cover Cantilver strip poly and oxide off of solar cell array</td>
</tr>
<tr>
<td>36.</td>
<td>Etch unwanted polysilicon</td>
</tr>
<tr>
<td>37.</td>
<td>Etch unwanted oxide</td>
</tr>
<tr>
<td>38.</td>
<td>strip resist</td>
</tr>
<tr>
<td>39.</td>
<td>Drive in dopants and Grow 500 Å of oxide.</td>
</tr>
<tr>
<td>40.</td>
<td>Deposit 10,000 Å oxide LTO</td>
</tr>
<tr>
<td>41.</td>
<td>7th Lithography for Contact cut and removal of oxide from cantilever</td>
</tr>
</tbody>
</table>
22\textsuperscript{nd} Annual Microelectronic Engineering Conference, May 2004

<table>
<thead>
<tr>
<th>42. Etch Oxide</th>
<th>BOE or buffered oxide etch is used</th>
</tr>
</thead>
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<tr>
<td>43. strip resist</td>
<td>Branson Asher use Hard ash recipe</td>
</tr>
<tr>
<td>44. RCA Clean</td>
<td>Done in RCA bench standard process</td>
</tr>
<tr>
<td>45. Deposited aluminum on the wafer</td>
<td>The aluminum is used as a hard mask for the polysilicon actuator the aluminum should be 2 \textmu m. Deposited with the CVC evaporator</td>
</tr>
<tr>
<td>46. 8th Lithography for aluminum create contact cuts and hard mask for actuator</td>
<td>Lithography using SVG track and GCA Stepper.</td>
</tr>
<tr>
<td>47. Aluminum etch</td>
<td>50 C aluminum etch in phosphoric acid</td>
</tr>
<tr>
<td>48. strip resist</td>
<td>Branson Asher use Hard ash recipe</td>
</tr>
<tr>
<td>49. Etch unwanted polysilicon</td>
<td>Could use Drytech Quad SF6 30 sccm CHF3 30 sccm 40 mTorr 200 watts Rate 1900 Å/min 12 min/wafer</td>
</tr>
<tr>
<td>50. Release actuator with Oxide etch</td>
<td>Use HF + HCl etch until structures are released. Time about 20 min.</td>
</tr>
<tr>
<td>51. strip resist</td>
<td>Branson Asher use Hard ash recipe</td>
</tr>
<tr>
<td>52. Al sinter</td>
<td>Use Bruce Furnace</td>
</tr>
<tr>
<td>53. Test</td>
<td>Shine light onto solar cell region record voltage</td>
</tr>
</tbody>
</table>

IV. FABRICATION

During fabrication of the devices the nitride level started to lift off severely after the second implant. This was due to an uneven and excessive nitride deposition. During the nitride deposition the gasses were accidentally shut off. Bruce Tolleson was there and was able to turn on the gasses so the deposition could continue. When recalculating how much time was left on the run I did not account for the time that the gas was shut off. But even though the gas was shut off there was still gas in the lines. This gas continued depositing onto the wafers. This excessive nitride deposition along with the poor uniformity of the nitride film created enough stress for the film to lift off.

When the film lifted off I consulted Dr. Fuller with what I should do and he told me to remove the old nitride layer using a hot phosphors etch remove the base oxide layer and then grow a new oxide and redeposit nitride. The problem with this line of action was that I had decided to make the nitride film my photo alignment layer. Meaning the nitride layer contains the alignment marks that all of the other photo lithography steps align to. If I were to just remove the nitride layer and grow another one my alignment would not be correct and I would probably not have working devices. Dr. Fuller then suggested to grow a thin layer of oxide etch and then continue on. This extra oxide growth should create a step because oxide grows at a different rate over a doped region compared to the silicon substrate.

I proceeded as Dr. Fuller had instructed. This plane of action did have one problem left and that was thermal budget. The original simulation did not account for all these extra thermal steps. The two oxidation growths and the nitride deposition all are done at temperatures that will diffuse the phosphorus already implanted deeper into the substrate. There also was a time restraint on the rework. I needed to complete all the work in one day in order to deposit my 3 um of oxide using the P5000. The P500 converts from a six inch tool to a four inch tool and was only going to be at four inches for a couple of days. The oxide deposition being performed in the P5000 was crucial because the oxide that it deposits is more uniform than the low temperature oxide done in the LPCVD. Also if the 3 um of oxide was done in the LPCVD it would take over 8 hours compared to 2 hours for the P5000.

The rework was done in time to deposit the 3 um of oxide by the P5000. Unfortunately there was not enough time to do any photo lithography before the oxide deposition. This created a complex series of lithography steps to get back on track. Also the alignment marks were there but very blurry. The alignment of all remaining photo steps was not great, the alignment was usually of a micron or two in either x or y and sometime both but there was nothing to do to eliminate this problem.

Do to time restraints and tool availability the wafers were split into two lots. The first lot would be the wafers that would undergo the steps necessary to create the solar cells. The other lot would undergo the necessary steps to create the cantilevers. This allowed me to save time and be able to work on either lot depending on what was available.

This strategy worked I was able to complete both lots and begin testing. The complete new process flow along with data for depositions and growths is located inside my lab notebook.

V. ANALYSIS

The solar cell array was tested by a multimeter to determine the open circuit voltage (VOC). A probe was placed at both ends of the cell and a voltage was recorded. There were very few cells that worked. Only five working cells total were found. They have an average VOC of .058 V.

One array was discovered consisting of two solar cells. The overall voltage produced by the array was 108.5 mV. One cell had a voltage of 55.7 mV and the other 53.4 mV. This showed a
small voltage loss across the two cells but is probably due to resistance caused by poor alignment. A third cell was tired in the array but the overall voltage dropped to 80 mV showing that it was not working device. It was resisting the flow of electricity. The voltage obtained from the solar cells is less than the expected .3 volts per cell. I believe this is due the fact the junction depths of the solar cell are too deep for optimal performance. Also the alignment problem could have created bad contacts increasing resistance or no contacts at all. A new simulation was done to identify what the new voltage of the solar cells should be. The simulation results were not believed to be accurate. The cross-sectional view of final the junction depths are not correct. When running a simulation the mesh or the amount of data points taken and where they are taken is crucial if the mesh is not done correctly the results will not be accurate. For the first simulation it took several days adjusting the mesh to create acceptable junction profiles. I was unable to identify a proper mesh for the new simulation. The images below are of that array.

The cantilevers were also successfully tested. Several cantilevers were tested and would pull down to the substrate. There was a problem though the force to pull the cantilevers down to the substrate seemed to bend many of the cantilevers. This bend would not allow the cantilever to return to its original position. I believe this bending might be due to a larger distance between the wafer and the cantilever than calculated or the polysilicon cantilevers are either molecularly weak or too thin. The polysilicon was deposited over two runs and this might have created polysilicon that is not as strong as expected. The polysilicon deposited the first run might not be bonding well with the polysilicon of the second run. These multiple runs also create uniformity issues where there might be areas that are too thick or too thin. Below is a picture of 200 um long cantilever being deflected by 80 volts of electricity. The movement of the cantilever can be seen by the change in color from black to a shiny white.
VI. Conclusion

The solar cell array and cantilever actuator were a success despite complications during fabrication a working array was discovered comprised of two solar cells with a VOC of 108.5 mV. Several cantilevers were successfully tested. For future work the process that was used to fabricate the solar cells should continue to be resimulated and compared to the results. Further electrical testing should be done on the working solar cells such as a diode sweep to help better understand there behavior.

VII REFERENCES


Fabrication of a Magnetically Actuated Torsional Beam

Gary A. Fino

Abstract – A mesoscopic magnetic beam contained in a silicon frame attached to the bulk of a silicon wafer with pivoting hinges will be used to show the affects of magnetic fields on movable magnetic structures. The pivoting hinges will be etched out of silicon using a Deep Reactive Ion Etcher (DRIE) system and the dimensions of the hinges will determine the force required to deflect the beam. Below each end of the beam will be large copper inductor coils fabricated on a separate wafer. When a current is applied to the coil, the magnetic field generated will attract the beam towards it. The critical component of the pivoting magnetic structure will be the silicon frame that supports the magnetic material.

Index terms – Magnetically actuated devices, pivoting silicon, DRIE

I. INTRODUCTION

In the field of Microsystems Technology components often contain surfaces that are magnetically attracted to devices that generate magnetic fields. The surfaces may be accidentally attracted or the field can be used to activate a device such as a MEMS actuator. One method to demonstrate the strength of magnetic fields to attract a surface is to position large copper inductors near movable parts. Currently at RIT research is ongoing on the affects of inductors and ways to make coils smaller and just as effective. A magnetic beam supported by a pivoting frame of silicon is an effective way to show the affects of a magnetic field produced by an inductor on movable structures.

The objective of this investigation is to design and fabricate a magnetic structure that requires a known amount of force to move or pivot. The structure will then be placed over a set of copper inductors, which will attract the magnetic material when a current is applied creating a magnetic field. The critical component of the pivoting magnetic structure will be the silicon frame that supports the magnetic material. By applying a current to the inductor below the end of the magnetic beam, a magnetic field will be created and interactions of the beam and the magnetic field can be studied.

The copper inductors were fabricated using a Deep Reactive Ion Etching (DRIE) system, copper electroplating, and Chemical Mechanical Planerization (CMP) techniques. Also, the frame of silicon was created using different thicknesses of oxide as masking layers to fabricate a multilevel frame of silicon using one DRIE etch. Following the etch, the frame was filled with a magnetic epoxy and the magnetic beam was placed over the copper inductors. The magnetic beam should be deflected from the resting position with an applied current to the inductors.

II. THEORY

The mechanical force required to tilt the magnetic beam must be less than the generated magnetic force created by the copper inductors for the beam to tilt. First, to simplify calculations the force was assumed to be applied at the end of the beam. The mechanical force required to tilt the beam can be found by calculating the torque. To find torque, constants ?, G, a, b, and K must be calculated.

\[
\theta = \tan^{-1}\left(\frac{\text{Beam Deflection}}{\text{Half Length of Beam}}\right)
\]

\[
G = \frac{\text{Young's Modulus}}{2*(1 + \text{Poisson's Ratio})}
\]

\[
a = 0.5*\text{Cross Sectional Length}
\]

\[
b = 0.5*\text{Cross Sectional Width}
\]

\[
K = a\left(b^4 + 3.36\left(\frac{b}{a}\right)^{1.5}\right)
\]

\[
\text{Torque} = \frac{2*\theta*G*K}{\text{Hinge Width}}
\]

The net mechanical force required to tilt the beam is the Torque * Half Length of the beam. [1]

The magnetic force to tilt the beam is calculated by finding the difference in field strength from the top and bottom of the beam. The magnetic force of the coils can be found by calculating the B field at the top and bottom of the beam. The net magnetic force is the force at the bottom of the beam minus the force at the top of the beam. B must be found for each ring of the coil and then summed for the distance at the bottom and top of the beam. The number of times to find B depends on the number of coils in the inductor. [2]

\[
B = \frac{\mu_0*(\text{coil spacing})*\text{(coil radius)}^2}{2*\left((\text{coil radius})^2 + (\text{beam distance from coil})^2\right)^{3/2}}
\]

\[
\text{Force} = \text{Beam Width}^2*M_s*B_{real}
\]

Net Force = (Force at Bottom of Beam) – (Force at bottom of beam)

The formulas and amount of book keeping involved to calculate these figures requires the use of a spreadsheet program. Data can then also be plotted to analyze data such as in table 1. See figure 7 for table and hinge dimension key.
III. DEVELOPMENT/SIMULATION

Computer rendered images of the silicon frame design can be seen in figures 1-3 to understand the frame structure. Once all formulas were entered into a spreadsheet the mechanical force was found depending on the dimensions of the hinges. Also, the magnetic force generated was found depending on the dimensions of the coils, wire width, depth, and spacing. The mechanical force was then plotted against varying hinge size ranging from 10 - 100μm. Results can be seen in Table 1. An increase in hinge length and width did not have a dramatic impact on force while a change in height drastically increased the force required to tilt the beam. The height measurement is determined by etching, not lithography, meaning careful measurements needed to be made to make the DRIE etch accurate. After hinge and coil dimensions were simulated, sizes were found and can be found in table 2. By using these numbers theoretically the force generated by the coil should be able to tilt the beam.

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Size (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beam length</td>
<td>5000</td>
</tr>
<tr>
<td>Beam width</td>
<td>1000</td>
</tr>
<tr>
<td>Hinge width</td>
<td>40</td>
</tr>
<tr>
<td>Hinge height</td>
<td>20</td>
</tr>
<tr>
<td>Hinge length</td>
<td>10-60</td>
</tr>
<tr>
<td>Coil Width, Spacing, Depth</td>
<td>20</td>
</tr>
<tr>
<td>Coil distance from bottom of beam</td>
<td>400</td>
</tr>
<tr>
<td>Coil distance from top of beam</td>
<td>500</td>
</tr>
<tr>
<td>Coil length</td>
<td>3000</td>
</tr>
<tr>
<td>Number of turns</td>
<td>25</td>
</tr>
</tbody>
</table>

IV. FABRICATION

Fabrication of the beam and copper coils were done simultaneously and concluded about the same time. Once both pieces were fabricated the two structures were brought together for actuation.

The coils and beam frame were fabricated using standard photolithographic processing on Shipley 812 photoresist 1μm thick. The coil pattern was etched 20μm into the silicon using the STS DRIE system and the photoresist was removed. Next a thin oxide of 1000Å was grown and the inductor wafers were ready for metal. Without breaking vacuum a 500Å layer of tantalum was sputtered followed by a 1000Å layer of copper to act as a seed layer. Copper does not adhere well to silicon so a thin layer of tantalum helps with adhesion issues between the silicon wafer and copper. Tantalum adheres very well to silicon and by not breaking vacuum the copper layer can adhere very well to the defect free, non-oxidized surface of tantalum. After the seed layer was blanket coated completely over the surface of the wafer was ready for electroplating. A solution of cupric sulfate and sulfuric acid was prepared and the wafers were electroplated until the 20μm patterns were not visible. The wafers were then polished back using CMP processes until the copper coil was the only conducting objects on the wafer.

The processing for magnetic beam started with patterning oxide and depositing another oxide layer over it. The new layer was also patterned so there were two thicknesses of oxide and bare silicon visible. Last a 1μm layer of TEOS was deposited and patterned, now 3 levels of oxide and bare silicon were visible. Last an 8μm layer of TEOS was deposited on the backside of the wafer for an etch stop. The wafer was placed in the STS DRIE until the sections where bare silicon was visible was completely etched through the wafer. Prior to this etch the etch rates of oxide, TEOS, and silicon in the DRIE system were all found to provide the correct thicknesses for the films to act as hard masks knowing the point when those films will be etched away.[3] When etching was complete the underside of the beam frame is shown in figure 5. The beam is still suspended to the bulk silicon by the layer of TEOS on the backside but it can be easily release by etching the TEOS in buffered oxide etch (BOE). Before the frame was released the middle of the frame was filled with nickel-loaded epoxy. Since the viscosity of the epoxy can be best described as "clumpy," a few drops of deionized water added to the epoxy thinned it out. Using the tip of a needle, a drop of the epoxy was placed into the frame and once the surface tension of the drop contacted the frame, the drop spread out, filling the frame. After the epoxy was cured the beam was soaked in BOE and the beams were released. This concluded the fabrication of the beam.

V. TESTING

Testing took part in three stages. First, the inductors were tested using ferrite powder with a particle sizes less than 5μm. If a current was placed on the coil of wire a magnetic field should be created and the powder will be attracted to the wire. Second the beam will be tested with a permanent magnet. If the silicon frame pivots towards the magnet the beam and hinges work correctly. Last, the beam will be placed over the inductors and a current will be put on the coil to attract the beam.

VI. CONCLUSION

The torsional magnetic beam was successfully fabricated and moved using a permanent magnet. This was captured through a stereomicroscope and also could be seen by the naked eye. Also, the fabricated copper inductors attracted sub 5μm particles of ferrite material moving the particles 5-20μm on average, proving a magnetic field was generated. The inductors however were not powerful enough to have an effect on the magnetic beam when it was placed above as planned. The process to use multiple levels of oxide to hard mask silicon to create a multilevel surface in a single
etch was very successful, and the beam frame was fabricated. After one DRIE 4 levels of silicon were obtained including one level etching completely through the wafer. Last, using a needle tip and a watered down solution of nickel loaded epoxy the beam was filled with the magnetic media via the surface tension of water.

VII. PICTURES/TABLE

Figure 1-3: Computer Rendered Image of beam frame structure
Figure 4,6: SEM image of silicon hinge after DRIE
Figure 5: SEM image of beam frame after DRIE
Figure 7: Computer Rendered image of cross section of beam frame w/hinge dimensions linked to table 1
Figure 8: Side view of beam frame over coils
Figure 9: Top view of beam frame over coils

REFERENCES

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Gary Fino (S’04), originally from Buffalo, NY, received a B.S. in Microelectronic Engineering from the Rochester Institute of Technology in 2004. He obtained co-op work experience at LACOMS in Rochester, NY in the areas of process improvement and power reduction. Also, he has done research on a National Science Foundation grant in Rochester, NY in the field of micromagnetics. He is currently pursuing a career to put his newly earned degree to use.
MEM’s Optical Pyrometer

Edward Camacho

Abstract— Measuring temperature accurately has been and still is a topic of interest in various professional fields such as Astronomy, Biology, Physics and Medicine. An optical pyrometer has great potential in these fields, because it can optically capture a body’s black body radiation and determine a temperature value of the body in question. This technology is well known, yet it is still gaining grounds as new uses are found. In this project a temperature sensor using Mentor Graphics was design, second a four level mask was made into one reticle. Third fabrication of the optical sensor took place using typical process steps in PMOS fabrication. Fourth, a filter out of silica/silicon was made to keep away various wave lengths in the electromagnetic spectrum from the sensor that will just become noise and, fifth testing is in the process of being performed with a known source of black body radiation.

A thermal couple is a device that can be constructed by micro machining and molding of microstructures to create a optical pyrometer (an optical temperature sensor). The thermal couple is made by the junction of two metals, and a thermopile is various thermal couples in series, the more elements in series the more accurate it becomes. Aluminum – Polysilicon thermal pile of # 16 elements was constructed. In order to minimize alignment error relative large thermal couples in the order of 10μm by 10μm in pixel size. This project used a 4-mask layer process. Having a fabricated 2 by 8 array of sensor, the double sided polished silica filter will be attached to the entire area of the sensors, and voltage meter will then be attached to the leads of the device and testing of various objects will be done.

This type of technology is used today for cost effective way to have temperature sensors in motherboard, temperature sensors, and cheap thermostats. This technology has great potential, especially in areas dealing with CMOS and MEMS.

Index Terms— Optical Pyrometer, Thermopile, Seebeck coefficient, Thermocouple

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E. Camacho is with the Rochester Institute of Technology, Rochester, NY 14623 USA (e-mail: ecamacho_98@hotmail.com).
2.1. The Peltier Effect

In 1834, Jean Charles Athanase Peltier, discovered that when an electric current flows between two conductively different metals, heat will be absorbed or released depending on the direction of the Seebeck current and the electric current. The Peltier effect can be seen in figure 1. (S. Weckmann, *Dynamic Electrothermal Model of a Sputtered Thermopile Thermal Radiation Detector for Earth Radiation Budget Applications, chapter 2*)

2.2. The Thomson Effect

In 1852, Lord Kevin (William Thomson) discovered that a current would be present in a conductor when a temperature gradient is apparent. Absorbed or rejected energy will be dependent on the current of the conductor. The release of thermal energy will imply a current inside the conductor in the same direction as the heat flow; other than this it will be absorbed. The Thomson effect is observed in figure 2. (S. Weckmann)

2.3. The Seebeck Effect

In 1821, Thomas Johann Seebeck made the discovery that the creation of an electrical voltage was possible by the temperature difference between two metals having different conductive properties at the other end of the two wires. "The Seebeck effect is the result of both the Peltier effect and the Thomson effect" (S. Weckmann). The Seebeck effect is the heart of thermocouples; if two metals having different Seebeck coefficients are jointed together at one end, the presence of a voltage (electromotive force) will be apparent using a voltmeter at the other end. The voltage that is present is due to the temperature gradient, between the two sides. (S. Weckmann). In figure 3, the Seebeck Effect is seen, showing the thermal gradient and the electromotive force to the left at the cold junction (reference junction). The $\Delta V$ Coefficient and the Seebeck Coefficient

2.4. The $\Delta V$ Coefficient and the Seebeck Coefficient

As it was mention earlier, this project will involve the use of two metals for the fabrication of the thermocouple. The two metals will be Polycrystalline Silicon (polysilicon) and Aluminum (Al). Using the three thermoelectric effects with respect to these metals will result in a potential voltage. The main effect that is predominantly applicable is the Seebeck effect, where an electromotive force is formed as a result of the proportionality of the thermal gradient between the hot and cold junctions in the materials. The change in voltage between the two junctions is described by taking an integral over the starting/reference temperature to the final temperature. This is shown by the following equation; $\Delta S = \int_{T_0}^{T} S \, dT$ which simplifies to $E = S_{A-B} \Delta T$. Keep in mind that this is true for one thermal couple. $S_{A-B}$ is the Seebeck coefficient difference between the two metals. The Seebeck coefficient is a material property that is temperature dependent, and can be found by $S = \frac{dV}{dT}$. In metals, the Seebeck coefficient is given by the approximation $S \approx (\pi^2 k^2 T^2 / 2qE_F)$ (Thermoelectric Effects in Metals: Thermocouples © S.O. Kasap 1997-2001, an e-Booklet). Some of the constants and/or variable that this equation uses include $k$ (which is Boltzmann’s constant), $P$, $T$ for temperature in Kelvin, $x$ a numerical consent dependant on charge transport mechanism, $q$ the charge of an electron and $E_F$, the Fermi energy at 0K.

2.5. Seebeck coefficient calculation for p-type polysilicon and aluminum

In the S. O. Kasap e-Booklet, table 2, lists the coefficient of

### Table 1: Poly Silicon Material Properties

<table>
<thead>
<tr>
<th>Description</th>
<th>$S$</th>
<th>$\rho$</th>
<th>$\lambda$</th>
<th>$\frac{\alpha}{\rho}$</th>
<th>$ZT$</th>
</tr>
</thead>
<tbody>
<tr>
<td>B-doped Single Crystalline Silicon</td>
<td>281</td>
<td>92</td>
<td>14.5</td>
<td>0.00037</td>
<td>0.07</td>
</tr>
<tr>
<td>P-doped Single Crystalline Silicon</td>
<td>-120</td>
<td>0.5</td>
<td>14.6</td>
<td>0.00151</td>
<td>0.03</td>
</tr>
<tr>
<td>Undoped Single Crystalline Silicon</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>P-doped CMOS Poly-Silicon</td>
<td>-122</td>
<td>0.5</td>
<td>20</td>
<td>0.00135</td>
<td>0.01</td>
</tr>
<tr>
<td>As-doped bulk single crystal cm$^3$</td>
<td>280</td>
<td>25</td>
<td>100</td>
<td>0.0035</td>
<td>0.1</td>
</tr>
<tr>
<td>B-doped bulk single crystal cm$^3$</td>
<td>-2.45</td>
<td>41</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

*Present work.* *Data taken from Ref. 18.* *Data taken from Ref. 19.* *Data taken from Ref. 20.* *Data taken from Ref. 21.

*We did not find the thermal conductivity of arsenic-doped silicon. We used the thermal conductivity of phosphorus-doped silicon at the same carrier concentration taken from Ref. 21.*
selected metals. Here the aluminum Seebeck coefficient is shown as

It needs to be noted that a positive sign on the Seebeck coefficient indicates that electrons are migrating from the cold junction to the hot junction. The Seebeck coefficient for Al was calculated at room temperature (300K) using

\[ S = \frac{\pi^2 k^2 T}{2 q E_F \rho_0} \]

to be \(-1.75645 \mu V/K\).

Polysilicon's Seebeck coefficient, on the other hand is not as simple as Al's. In a document online at http://www.ee.uta.edu/Online/cbutler/MEMSWebpage/pdfs/EE5349chapte r5.pdf it was shown that the Seebeck coefficient for n-type polysilicon and p-type polysilicon where;

\[
S_{n-poly} = -\frac{k}{q} \left[ \ln \left( \frac{N_c}{n} \right) + \frac{5}{2} \right] + (1 + S n) + \Phi_n \\
S_{p-poly} = \frac{k}{q} \left[ \ln \left( \frac{N_p}{p} \right) + \frac{5}{2} \right] + (1 + S p) + \Phi_p
\]

Where \( N_i \) is the effective density of states in the valance band, \( \Phi_n \) & \( \Phi_p \) are the excitations of molecules as a result of the thermal gradient. In the same document an approximation for n-type polysilicon and p-type polysilicon is shown as \( S = \frac{\Delta h}{q} \ln \left( \frac{\rho}{\rho_0} \right) \) where \( \Delta \) is receptivity and \( \rho_0 \) is \( 5 \times 10^6 \) O-cm. For accuracy, the results of a paper by A. Jacquot named “FIGURE-OF-MERIT AND EMISSIVITY MEASUREMENT OF FINE GRAIN POLYCRYSTALLINE SILICON THIN FILM” shown in table 1. By using a p-type phosphorous doping at a concentration of \( n = 6E20 \) [m\(^3\)] and a Seebeck coefficient of about \(-122 \mu V/K\) at room temperature for the polysilicon, the resulting \( S_{AB} \) for the Al-PolySilicon becomes \(-1.78 \mu V/K\). For the thermocouple calculation of the thermal gradient induce voltage then becomes \( \Delta V = 123.78 \Delta T \).

Therefore \( \Delta T \) equation becomes:

\[
\Delta T = \frac{P_e}{A \sigma_h} \left[ 1 - e^{-\frac{m^* c_p}{l}} \right]
\]

Now the electromotive force equation makes logical sense with respect to volume \( \Delta V = S_{AB} \Delta T \) for a thermocouple and \( \Delta V = n S_{AB} \Delta T \) for a thermopile, with elements in series. Weckmann also showed another important equation - the equation to have a measure for the thermocouple's sensitivity where \( x \) is the ratio of output voltage over input power. Shown by: Sensitivity = \( \frac{\Delta V}{P_e} \).
2.7. Specifications/Dimensions

What amount of energy is this device going to absorb? To answer this question some limitations and assumptions need to be made. For example let's limit the device by assuming that the dimension length*width*height of aluminum are approximated to the dimensions of Poly-silicon. Then let's assume that heat conduction is dependent upon the smallest conductivity and the smallest heat capacity of the two materials. Let us also assume that the time needed for any given measurement is about 1 second. Then let's assume that the device will be able to measure a heat flux in the order of 1nW. Having a small specification for heat flux absorption lets the device be capable of measuring very small changers in temperature. This project will use relative large structures in comparison to what is used today in the smallest critical dimension. This is going to be done to prove the concept of making a thermopile/thermocouple. As a result, it was decided to use a width of 2 micro meters, a height of 1 micro meter, and a length of 10 micro meters. This will give a volume of about 2E-17 m³. In table 3, some important values for the design of the structure are shown. Given the values in table 3 and \( \Delta T = \frac{\Delta Q}{\rho_s c_p} (1 - e^{-\frac{L}{r_n}}) \), \( ?T \) becomes 30.0483851637 K. Now that this is known then the value for the approximated voltage can be found from \( \Delta V = n * S_{ab} * \Delta T \), given that the previous value for \( S_{ab} \) was 123.78 [\( \mu \text{V/K} \)], and having one thermopile or a thermocouple, results in a value for \( ?V \) being 3.5530413 [mV]. (As it can be seen the value for heat flux is too big, but it can be changed)

<table>
<thead>
<tr>
<th></th>
<th>( \sigma [\Omega \text{m}] )</th>
<th>( \rho [\Omega \text{m}] )</th>
<th>( C_p [\text{J/kgK}] )</th>
<th>( S_p [\text{W/mK}] )</th>
<th>Mass [kg]</th>
<th>Density [kg/m³]</th>
<th>Volume [m³]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>2.86E-11</td>
<td>102</td>
<td>0.87</td>
<td>90</td>
<td>1.28E-14</td>
<td>7.90</td>
<td>3E-17</td>
</tr>
<tr>
<td>P-polSi</td>
<td>1.3E-11</td>
<td>25</td>
<td>1.34E-11</td>
<td>20</td>
<td>1.6E-14</td>
<td>2.30</td>
<td>3E-17</td>
</tr>
</tbody>
</table>

### III. EXPERIMENT

3.1. Process Flow

- Scribe, RCA Clean
- Nitride1 is flexible with thickness via ASM LPCVD
- LTO via ASM LPCVD
- Lithography Level1 is Active, via GCA Stepper and SVG88 coating and developing track.
- Resist Strip, RCA Clean
- Poly Deposition via ASM LPCVD
- Spin-on-glass
- Sinter - 20 min. 425°C in H₂/N₂
- Etch Spin-on-glass in – 25 min in BOE
- Measure Resistance via ResMap
- Lithography level 2 poly, via GCA Stepper
- Dry plasma etching of Nitride and Poly
- Resist Strip, RCA Clean
- 2nd Nitride via ASM LPCVD
- Lithography Level 3 Poly Contact, via GCA Stepper
- Resist Strip, RCA Clean
- Deposit Aluminum via CVC thermal evaporation
- Lithography level 4 aluminum, via GCA Stepper
- Etch aluminum via hot aluminum etch

3.2. Testing

An appropriate test setup was developed in order to test the chips. It consisted of a voltagemeter, a microscope, and a heater lab. It is seen in figure 4.

**Figure 4: Test Setup**

**IV. RESULTS**

Electrical Test Results concluded that the pyrometer works seen in table 4, yet more testing should be done to see the correlation to temperature change. Having built this device, looking back there are many things that can be done to improve how the device works. Some of these things include the design, the fabrication and the testing.
Table 4: Results

<table>
<thead>
<tr>
<th>1st Light source</th>
<th>Intensity [mW/cm²]</th>
<th>Voltage [V]</th>
<th>Temp [°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0.044</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>0.01</td>
<td>0.119</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>0.5</td>
<td>0.162</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>0.205</td>
<td>24</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2nd Light source</th>
<th>Intensity [mW/cm²]</th>
<th>Voltage [V]</th>
<th>Temp [°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0.044</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>0.01</td>
<td>0.142</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>0.5</td>
<td>0.170</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>0.200</td>
<td>24</td>
</tr>
</tbody>
</table>

V. CONCLUSION

The goal was to build a simple $2 \times 8$ thermopile consisting of 4 lithography levels. This was accomplished using a phosphorous doped poly and aluminum combination thermocouple in a 16 pixel array. The test chip can is shown in figure 5. It is seen that the aluminum etch ways completely in the require places. Yet, in figure 5 it is also observe the alignment error. The test chip showed preliminary results. Various elements can be improved to make a better overall design, ranging from the design to testing.

![Figure 5: Working Pyrometer](image)

VI. ACKNOWLEDGMENTS

- Dr. Santosh Kurinec
  - Rochester Institute of Technology
  - Microelectronic Engineering
  - Department Head
- Dr. Lynn F. Fuller

VII. REFERENCES


[3] (A, Jacquot, Figure-Of-Merit And Emissivity Measurement Of Fine Grain Polycrystalline Silicon Thin Film.)
Abstract—A study has been performed to determine the optimum surface treatment to adhere an aluminum hard mask to a polymethyl-methacrylate (PMMA) wafer substrate for the production of microfluidic channels.

The initial process parameters of the PMMA reactive ion surface treatment included oxygen plasma, sulfur hexafluoride plasma and argon plasma designs of experiments. However, a soak in tetra methyl ammonium hydroxide (TMAH) proved to provide the most adhereable surface for an aluminum deposition. It is hypothesized that the TMAH soak allowed for the removal of the surface layer of the PMMA wafer substrate.

The aluminum hard mask was deposited by evaporation after the wafers were surface treated with TMAH. Using contact photolithography, the aluminum was patterned and the PMMA wafer substrate was etched isotropically in propylene glycol mono methyl ether acetate (PGMEA) for the creation of microfluidic channels.

Success of this project is based on the quality of the aluminum evaporated film and the transparency of the PMMA wafer substrates after the isotropic etch in PGMEA.

I. INTRODUCTION

MICROFLUIDIC channels have been studied for their use in bio-MEMS related fields. These include sensors, fluid transport, DNA analysis and blood cell observation. PMMA is an ideal candidate as a substrate material because of its transparency at the visible wavelength as well as its availability and cost effectiveness. Aluminum was chosen as the hard mask for the PGMEA etch to create isotropic channels in the PMMA substrates for its availability, cost effectiveness and quality of process control. Because the melting temperature of PMMA is around 100°C, sputtering aluminum was not advised. Aluminum wet etch (phosphoric acid, acetic acid and nitric acid) does not attack PMMA. Please see Figure 1 for a drawing of the finished product of this project.

![Figure 1: Computer Rendered Concept](image)

Initially, the Drytek Quad, a reactive ion etch tool was used to try to treat the surface of the PMMA wafers using a design of experiments that included oxygen gas, SF₆ gas and argon gas from 1 - 10 minutes from 150 - 600 Watts.

It was noted that the time between reactive ion surface treatment and aluminum deposition when varied did not change the result. The PMMA substrates endured a high heat deformation at high powers and times of reactive ion surface treatment. The initial transparent PMMA wafers became non-uniformly opaque in the radial direction at every power and time reactive ion surface treatment. Aluminum depositions after a reactive ion surface treatment in all cases resulted in a non-reflective, film that did not pass the tape test.

The tape test is conducted after the metal deposition as a preliminary check to see whether or not the metal will adhere to the substrate and not be removed during an etch of the substrate. This test was advised by Dr. W. Grande and Tina Prevost. Please see Figure 2 for an actual picture of the aluminum film on a reactive ion treated PMMA surface. Please note that all wafers using every gas at various powers and times resulted in this.

This work is a design requirement for a B.S. degree in Microelectronic Engineering at the Rochester Institute of Technology (RIT), Rochester, NY. The results of the project were first presented as part of the 22nd Annual Microelectronic Engineering Conference, May 2004 at RIT.

G. Woodruff is with the Microelectronic Engineering Department, RIT. (e-mail gwW1964@yahoo.com)
II. THEORY

A. Reactive Ion Surface Treatment

Under vacuum, the PMMA wafers are subjected to plasma using a forming gas at a certain power for a certain amount of time. The gas molecules bombard the surface of the PMMA, theoretically allowing for an aluminum thin film deposition layer that is uniform, and is reliable throughout processing.

B. TMAH Soak Surface Treatment

The PMMA wafers were cut from a sheet and grinded to be the shape of a four inch silicon wafer for process manufacturing ease. The wafers came packed in a paper protective packaging that adhered to both sides of the wafer, which needed to be removed prior to processing. It is theorized that the 20 minute soak in the basic photoresist developer, 0.21 N TMAH removed the layer that adhered the protective layer to the PMMA substrates as well as cleaned the surface of the PMMA substrates.

C. Aluminum Evaporation

As current flows through the tungsten baskets, the aluminum pellets melt and aluminum molecules are released into the atmosphere inside the bell jar. As the aluminum molecules make contact with the PMMA wafers, they solidify and adhere. A low pressure and high currents are required for a thick, uniform aluminum film. Any air (carbon, nitrogen, oxygen) or alien molecules in the path of the aluminum molecules may create an aluminum film that may not stick or a very thin film. Aluminum film thickness and uniformity is also a function of the distance between source and substrate. The farther the source is from the substrate, the film is thinner and more uniform. The closer the source is from the substrate, the thicker the film but at a cost of non-uniformity.

III. PROCESS

The process for making Microfluidic channels in PMMA resulted in ignoring development in reactive ion surface treatments and using TMAH.
rotated about the top of the CHA Evaporator bell jar, approximately 27 inches above the source. The CHA Evaporator was pumped down to a pressure of $5 \times 10^{-6}$ Torr. Tungsten baskets were used to hold 4 aluminum pellets in two current sources. Sixty Amps ran through each tungsten basket melting the aluminum at 660°C for an evaporation rate up to 19 Angstroms per second and a thickness of 1.5 μm.

C. Contact Photolithography

The wafers were coated with Shipley 812 photoresist at 4500 RPM for 45 seconds and proximity pre-baked at 90°C for 3 minutes. Using the Karl Suss contact aligner, the wafers were exposed with a dose of 160 mJ/cm². The wafers were then proximity Post Exposure baked for 3 minutes at 90°C and developed using MF-CD 26, 0.26 N TMAH for 60 seconds.

D. Wet Aluminum Etch

The wafers were put into a bath of nitric, acetic and phosphoric acid to pattern the aluminum in the areas were the photoresist did not exist and expose the PMMA.

E. PMMA Etch in PGMEA

The wafers were soaked in PGMEA for approximately three hours with an etch rate of 1000 Angstroms per minute. The Phillips 525 Scanning Electron Microscope (SEM) was used in observing the wafers before and after the aluminum was finally removed. The SEM was used at an accelerating voltage of 5 kV with a spot size of 500 nm and the wafers were sputtered with gold to increase surface conductivity and the reduce PMMA charging.
IV. RESULTS AND DISCUSSION

A. PMMA Surface Quality

As seen from Figures 4 - 11, the surface of all films; aluminum, photoresist and PMMA remain spotless, pristine and uniform. The PMMA remains transparent throughout the experiment and the line edge roughness is minimal on the aluminum.

B. Aluminum Adhesion

As seen in Figures 8 – 10, the PGMEA etched the PMMA isotropically in all directions without lifting up the aluminum film. The aluminum film at the edges is undercut and overlaps in the absence of PMMA. This shows that the aluminum not only stuck to itself but also the PMMA substrate.

V. CONCLUSION

Microfluidic channels were made by etching isotropic channels in poly methyl methacrylate by optimizing aluminum adhesion. Reactive ion surface treatment was shown to thermally manipulate the PMMA substrate, while soaking the PMMA wafers in 0.21 N tetra methyl ammonium hydroxide for 20 minutes proves to clean the wafer well prior to the aluminum deposition. Propalene glycol monomethyl ether acetate is shown to isotropically etch PMMA and aluminum is proved to serve as a protective etch mask for PMMA when the substrate is properly treated.

ACKNOWLEDGMENTS

The author thanks Tina Prevost for great assistance and cooperation and Dr. W. Grande for project guidance. The author would also like to acknowledge the RIT Semiconductor and Microsystems Fabrication Laboratory staff for technical assistance and equipment support. Special thanks to Bruce Tolleson and Dr. L. Fuller.

George W Woodruff III, originally from Penn Yan and Lowville, New York, received a B.S. degree in Microelectronic Engineering from the Rochester Institute of Technology in 2004. He obtained co-op work experience at Analog Devices Inc. in Cambridge, MA, NanoPower Inc. in Rochester, NY, and Ferro Electronic Materials, in Penn Yan, NY, and has done MEMS Gear and Pressure sensor research as well as Titanium Silicide research at RIT. He is currently pursuing a Ph.D. degree in Microsystems Engineering at RIT.