TANOS (TaN, Al_2O_3, Si_3N_4, SiO_2, Si) Charge-trap Flash Devices

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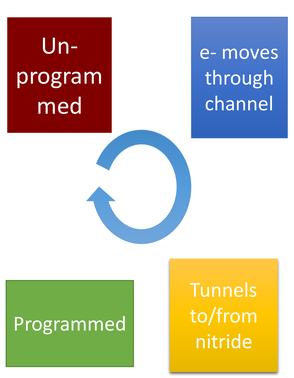
Project Objectives

Goal: To demonstrate charge-trapping in a TANOS Stack at RIT

- Gate stack film depositions determined by experimentation, testing
- C-V structures fabricated and tested by patterning gate stack with GCA C-V Mask.
- NMOS charge-trap flash devices currently being fabricated with modified version of AdvCMOS150 Process w/ TANO gate stack.

Charge-trap flash operation

- Charge-trap flash operates in a similar fashion to EEPROM, only the storage layer is Si3N4 instead of polysilicon. This is advantageous because charge is more likely to remain in the non-conductive charge traps of Nitride than in conductive polysilicon.



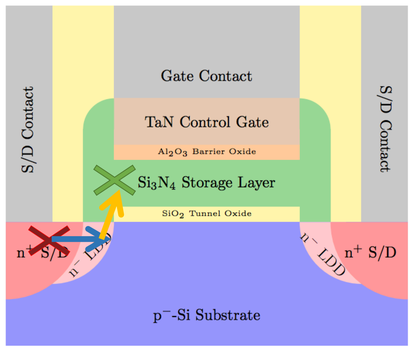
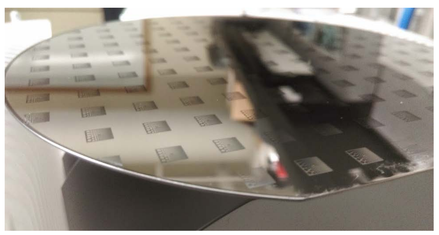
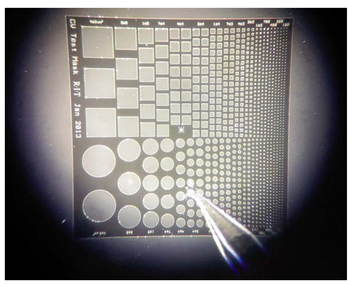
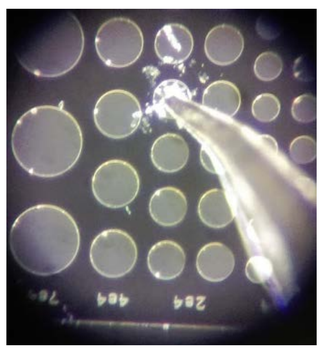


Figure 5. Adv-CMOS 150 Modified TANOS

C-V Wafer and Structures



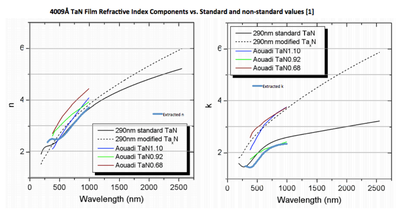


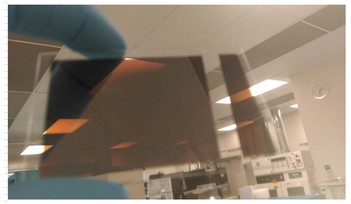


Film Optimization

Control Gate: TaN

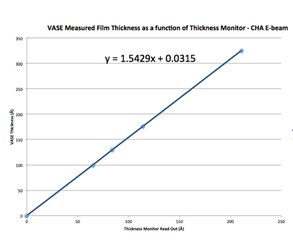
Reactively sputtered in partial pressure Ar/N_2 ambient in CVC601 plasma sputter. Deposition rates, ~802Å/min, are lower than standard Ta. Refractive index and resistivity (505μΩ•cm) match stoichiometric TaN numbers almost perfectly.

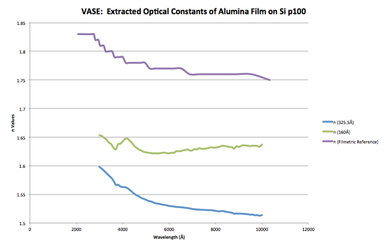




Barrier Oxide: 100Å, 130Å Al_2O_3

Deposited in the CHA E-beam evaporator, refractive index describes an Al2O3 film which may have some impurities but should perform well as a dielectric.



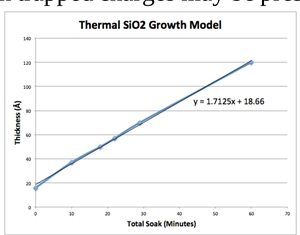


Floating Gate (Storage Layer): 100Å Si_3N_4

Deposited in ASM LPCVD Tube 2, using a shortened version of the Low Pressure Nitride recipe.

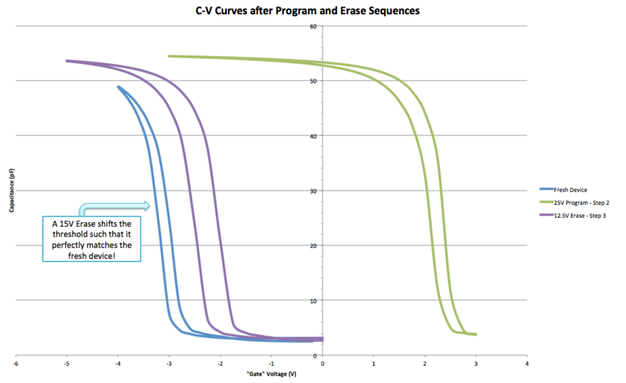
Tunnel Oxide: 30Å, 50Å, 70Å SiO_2

Grown using a shortened version of the Adv_CMOS 150 gate oxide recipe which incorporates N_2O and O_2 soaks of equal length, measured on VASE and shown to be in the linear growth region (modeled below). Refractive indexes describe a quality oxide, though trapped charges may be present due to lack of Trans-LC clean.



Measured Device Characteristics

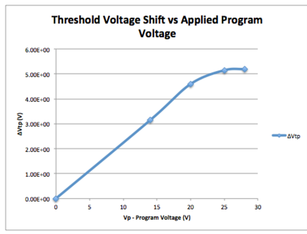
Program/Erase C-V

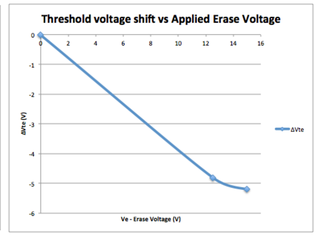


Threshold Voltage Characteristics:

$\Delta V_{tp} = V_{tp} - V_{t0}$ where, V_{tp} is the threshold voltage after program and V_{t0} is the threshold voltage of a fresh device.

$\Delta V_{te} = V_{te} - V_{tp_{max}}$ where, V_{te} is the threshold voltage after erase and $V_{tp_{max}}$ is the maximum possible programmed threshold voltage.





Conclusions

C-V Devices showing charge-trapping flash memory characteristics were successfully fabricated using CMOS processes available in the RIT SMFL. Full Device wafers will be continued and should show enhanced P/E characteristics due to the enhanced ability to program and erase the device by Hot Carrier Injection, rather than by modified Fowler Nordheim tunneling (as in C-V Devices).

Acknowledgements

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