Conference of Microelectronics Research 2000

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Editorial

These proceedings contain research papers presented at the 18th Annual Microelectronic Engineering Conference held at the Rochester Institute of Technology (RIT) on May 8 through 10, 2000 by senior undergraduate students of Microelectronic Engineering of RIT. The students graduating with BS degree in Microelectronic Engineering are required to take a four credit hour course, EMCR 660 entitled Seminar/Research in their fifth year. The course consists of submission of a research proposal, related to the field of semiconductor devices and processing, by each student and carrying out the project through the ten-week spring quarter. The students are required to present their work at the Microelectronic Engineering Conference held at RIT annually in the month of May and publish in the proceedings.

The class of 2000 presented impressive and technically challenging research projects on various topics ranging from advanced microithography, gate dielectric engineering, novel device structures and processes, back-end processes, and MEM devices.

I congratulate the students for their valuable contributions to the conference and towards the Microelectronic Engineering at RIT. On behalf of the faculty and staff of the Department of Microelectronic Engineering, I wish the students successes in their career ahead.

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A Chrome AR Film for Binary Photomasks

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Abstract- A photomask typically consists of a bulk transparent substrate and a thin metallic film with etched pattern on the surface for light absorption. Stray light reflecting off of the top surface of the photomask is especially problematic because it is focused onto the wafer surface, causing unwanted exposure of the photoresist. Lithographic performance can be significantly improved if this reflection is reduced with an antireflective layer on the top surface of the photomask. There are commercially developed antireflective films for chrome based photomasks. These films were designed to meet certain specifications for optical density and reflectivity. The goal of this project was to develop a process to replicate these commercial films at RIT. X-ray Photoelectron Spectroscopy (XPS) was performed on the commercial samples to obtain depth profiles of the atomic constituents of the chrome-based films. Absolute reflectivity and transmission data were obtained on these films using a Perkin-Elmer Lambda-11 UV/VIS Spectrophotometer. Finally, a sputter deposition process was developed to deposit a chrome film with bulk properties similar to those of the commercial films. The process was tuned so that the reflectivity of the RIT film closely matched the reflectivity of the commercial films. The result was an antireflective optically dense film appropriate for photomasks for optical lithography.

2. THEORY AND DESIGN

In order for a masking film to meet the specifications required for optical microlithography, it must be optically dense at the exposure wavelength and the reflectivity must meet certain specifications. Every material has a complex index of refraction (n + ik) that defines the speed of light through the material and the rate at which light is absorbed as it passes through the film. The index of refraction is frequency dependent, that is, it changes with changing wavelength. For metallic chrome, the imaginary part of the index of refraction is relatively high, ranging between 1.66 and 3.71 for optical lithography wavelengths. The amount of light transmitted through a material is governed by the equation,

\[ T = \exp(-4\pi k t / \lambda) \]  

where k is the complex part of the index of refraction, t is the thickness of the film, and \( \lambda \) is the wavelength of light. In order to build an optically dense film, a high k value is desirable as well as a thicker film. Because there are restrictions on the maximum thickness of the film, it is desirable to have as large a k value as possible. Because dielectric films have a much lower k value than metals, it makes sense that the bulk of the film should be mostly metallic. This was confirmed by the XPS data obtained on the commercial films shown in Figure 1 and 2. The bulk of the films on both Sample A and Sample B contained approximately 70-80% Chrome and 10-20% Nitrogen with trace amounts of Oxygen. The film is mostly metallic with a small portion of Chrome Nitride. It is assumed the nitride is present to assist in performing a more uniform etch rate through the film. The top surface of the commercial films contains a much higher concentration of Oxygen and a slightly higher concentration of Nitrogen. The presence of Oxygen makes the top surface of the film almost entirely dielectric. Dielectrics typically have a much lower k value and are therefore absorb less light than a metal.
The equation for Reflectance at a material interface at or near normal incidence is as follows, for an air-dielectric interface.

\[ R = \left[ \frac{n_1^* - n_2^*}{n_1^* + n_2^*} \right]^2 = \frac{(n-1)^2 + k^2}{(n+1) + k^2} \] (2)

Lowering the effective k value of the material can significantly reduce the reflectance. This means going to a less metallic surface, as the XPS data on the samples indicates. The reflectance of the top surface is a sensitive function of the complex index of refraction of the material, which in turn is a function of the atomic composition of the material and the wavelength of light.

3. PROCEDURES AND RESULTS

The XPS depth profiles of two commercial samples (Figures 1 and 2) were obtained by Evans East Company. These profiles were used to determine the bulk atomic concentrations of Chrome, Nitrogen, and Oxygen needed to provide a similar film. It was determined that the bulk of the film should be mostly Chrome with approximately 10-20% Nitrogen content. An iterative approach was taken to adjust the RF Power and Nitrogen partial pressure during the sputtering to develop a deposition process that hit the Nitrogen content target. The optimal conditions were determined to be 1200W forward RF power, 5mTorr pressure in the chamber at 20% N2 and 80% Ar. The deposition rate was found to be approximately 36Å/min.

The oxygen content of the top surface was adjusted according to the reflectance spectra of the film. The higher the oxygen content, the lower the reflectance, because of the reduced effective k value of the material. After several iterative approaches, the oxygen flow rate was determined to be 6sccm. This gave the reflectance spectra of the film that most closely matched the corresponding reflectance spectra of the commercial samples.

The following pages show examples of the reflection spectra of the RIT Cr AR Film compared to the reflection spectra of the commercial films (Figure 3). Also, the transmission spectra are plotted for the three films (Figure 4). The RIT film meets the requirements of an optical density of 3 (T < 0.001) for the desired exposure wavelengths less than 300nm.

4. CONCLUSIONS

The world of microlithography is full of many challenges. The reduction of flare in the optical system is one of the many steps taken to progress toward finer and finer resolution features. The development of antireflective absorber films for photomasks has contributed toward that end. The Chrome based AR film developed at RIT meets the performance specifications for a binary photomask film.
Figure 3: Comparison of Reflectance Spectra

Figure 4: Comparison of Transmission Spectra
Abstract—In lithography employed in IC fabrication, focus and exposure directly determine the printed resist image. Focus and exposure settings may be optimized with a focus exposure matrix (FEM) in which one parameter is varied by column and the other parameter is varied by row. A focus exposure matrix should be measured on a highly accurate and precise metrology tool, such as a CD-SEM. This experiment was performed using a Canon FPA 2000-il stepper, an SSI 150 coat/develop track, and a Hitachi S-6780 CD-SEM. ProData was used to graphically analyze the numerical data collected on the CD-SEM. Data collected in this experiment shows that, for the given equipment, varying exposure from 120 to 200 mJ/cm² in 10 mJ/cm² increments and focus from —0.5 to +1.5 microns in 0.25 micron increments gives a CD range beyond the +/-10% needed.

1. BACKGROUND

In the most basic sense, lithography is simply the transfer of a mask image into photoresist, a light-sensitive material. In practice, lithography is much more complex than that statement suggests. Success in Lithography, as in any other area of microelectronics, depends on successfully manipulating an extensive array of checks and balances. Broadening the tolerance on one parameter inversely tightens the tolerance on another. In a simplified view of day to day stepper operation, proper linewidth printing depends on focus and exposure dose. Critical dimensions may be plotted against focus and dose to represent the latitude for the given process. Most processes require a CD specification of less than +/- 10%. Ignoring focus variation yields the exposure latitude of the given process for the given CD specification. Exposure latitude simply represents the maximum exposure dose variation possible to meet the given CD specification. Exposure latitude simply represents the maximum exposure dose variation possible to meet the given CD specification. Exposure variation gives the depth of focus (DOF) for the given process and CD specification. DOF shows the most focus variation possible to print the CD within desired specifications. The depth of focus must account for variation in stepper focus and the wafer topography created by processing prior to the current level.

As mentioned above, considering exposure variation, focus variation, and allowable CD variation yields the process latitude or process window. The depth of focus available for a given process window is the usable depth of focus (UDOF).

Even in a simplified view such as the one above, it is vital to realize that dense features and isolated features will print optimally at different focus and exposure settings. This is largely accounted for by mask level corrections. Features may be given a mask bias based on how an unbiased feature prints. In some cases an isolated feature may be surrounded by “dummy features” to closely simulate dense features. The exposure process may then be optimized for dense features. The “dummy features” are likely printed on the mask small enough that they are below the resolution capability of the exposure tool; therefore, these “dummy features” are not transferred into a resist image. Even though these features are below the resolution capability of the exposure tool, they do modify the aerial image of the isolated feature which is actually transferred to resist.

Assuming no mask biases or corrections are present, isolated and dense features will print differently. To print these different features as designed (and without a mask bias), different process settings are necessary. Since isolated and dense features often co-exist on the same level, process settings must be chosen to adequately print both feature types making process latitude more important. The portion of the process window in which both dense and isolated features print adequately is often referred to as the process window overlay.

A dose to clear, or E0, wafer is useful as a daily or bi-daily test to baseline the lamp performance of each exposure tool used. A clear reticle may be used to expose the E0 wafer. Exposure is altered by a user specified amount at each die in the step pattern. The dose to clear can be determined by visually examining the wafer or measuring resist thickness remaining in die that appear nearly cleared. An E0 check must be performed separately for each exposure tool used.

An E0 wafer is actually a focus exposure matrix (FEM) with the focus change set to zero. The FEM, often called a FOCEX or FOCEXPO, varies one parameter by column and the other parameter by row. CD measurement
of CDs in the matrix reveal the process latitude available. Each die on a FOCEX wafer is essentially one "run" of a designed experiment. Multiple "runs" can be performed by processing multiple FOCEX wafers together. Depending on exposure tool software, it may be possible to hold focus constant on multiple columns (or exposure constant on multiple rows) to perform multiple "runs" on a single wafer. It is important to note that a focus exposure matrix must be performed separately for each level and probably for each level/exposure tool combination.

Sub-micron features are difficult to measure precisely and accurately with optical metrology tools. At some small CD, any specific optical metrology tool becomes completely inaccurate. Sub-micron CDs are best measured with scanning electron microscopes (SEMs) to guarantee precise, accurate CD measurement. Many CD-SEMs are designed to automatically drive from die to die and acquire a pre-selected CD. The CD-SEM acquires the CD by comparing what it sees to an image previously chosen and saved by a human user. CD-SEMs can measure the top and bottom of a CD and approximate the sidewall angle and a horizontal dimension part-way up the vertical axis. Since modern CD-SEMs are automated, they allow relatively quick measurement of a high number of CDs per wafer. This is necessary to reduce negative impact on wafer cycle time.

2. EXPERIMENTAL

This experiment was performed using a Canon FPA 2000-i1 stepper, an SSI 150 coat/develop track, a manual spin coater, a Nanospec Film Thickness Measurement scope, and a Hitachi S-6780 CD-SEM. OiR 620 photoresist and CD-26 developer were used. Wafers were patterned with the Canon test reticle which contains clusters of measurement CD's at 0.05 micron increments. Each cluster consists of five adjacent features. The center and outside 0.5 micron vertical lines were measured to simulate dense and isolated lines, respectively. ProData® was used to analyze the numerical data collected on the CD-SEM.

A preliminary wafer was run with focus and exposure settings determined theoretically in ProLith®, a lithography modeling software package from Finle Technologies. A final wafer was run with FE settings determined from CD measurements taken from the preliminary wafer. Besides FE settings, processing was the same for both wafers except for the coat step (and related bakes in the coat program). The preliminary wafer was coated on the SSI track. The final wafer was coated on a manual spin coater and baked on a hot plate for the dehydration and soft bakes. This discrepancy was necessary since the spin module in the coat track was under repair. The develop track was functional for processing of both the preliminary and final wafers.

A. General Process

- Dehydration Bake (200° C, 45 seconds)
- HMDS Prime
- OiR 620 positive resist coat
- Soft Bake (90° C, 60 seconds)
- Canon Exposure
- Post Exposure Bake (PEB) (105° C, 60 seconds)
- CD-26 Development (70 seconds)
- Hard Bake (120° C, 45 seconds)
- Nanospec resist thickness measurement
- Hitachi CD-SEM CD Measurement

B. Preliminary Wafer

The preliminary wafer was coated on the SSI track at a spin speed of 4500 RPM for 60 seconds. This wafer was exposed with focus varied by column from —2 to +2 microns in 0.5 micron increments and with exposure varied by row from 60 to 300 mJ/cm² in 30 mJ/cm² increments.

C. Final Wafer

The final wafer was coated on a manual spin coater at a spin speed of 3000 RPM for 25 seconds. This wafer was exposed with focus varied by column from —0.5 to +1.5 microns in 0.25 micron increments and with exposure varied by row from 120 to 200 mJ/cm² in 10 mJ/cm² increments.

3. RESULTS

The preliminary wafer which was coated on the SSI track had an average resist thickness of 9812 Å and a range
Table 1: Site-by-Site CD Data for Inside 0.5 Micron Vertical Line (Exposure across top row, Focus down left column)

<table>
<thead>
<tr>
<th>Exposure</th>
<th>120</th>
<th>130</th>
<th>140</th>
<th>150</th>
<th>160</th>
<th>170</th>
<th>180</th>
<th>190</th>
<th>200</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.50</td>
<td>0.491</td>
<td>0.429</td>
<td>0.416</td>
<td>0.346</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.25</td>
<td>0.568</td>
<td>0.548</td>
<td>0.526</td>
<td>0.478</td>
<td>0.436</td>
<td>0.408</td>
<td>0.388</td>
<td>0.346</td>
<td></td>
</tr>
<tr>
<td>1.00</td>
<td>0.574</td>
<td>0.554</td>
<td>0.526</td>
<td>0.471</td>
<td>0.443</td>
<td>0.429</td>
<td>0.401</td>
<td>0.387</td>
<td>0.346</td>
</tr>
<tr>
<td>0.75</td>
<td>0.561</td>
<td>0.526</td>
<td>0.498</td>
<td>0.429</td>
<td>0.395</td>
<td>0.408</td>
<td>0.443</td>
<td>0.422</td>
<td>0.415</td>
</tr>
<tr>
<td>0.50</td>
<td>0.533</td>
<td>0.512</td>
<td>0.491</td>
<td>0.401</td>
<td>0.387</td>
<td>0.388</td>
<td>0.464</td>
<td>0.429</td>
<td>0.415</td>
</tr>
<tr>
<td>0.25</td>
<td>0.547</td>
<td>0.533</td>
<td>0.505</td>
<td>0.429</td>
<td>0.436</td>
<td>0.436</td>
<td>0.443</td>
<td>0.436</td>
<td>0.422</td>
</tr>
<tr>
<td>0.00</td>
<td>0.547</td>
<td>0.533</td>
<td>0.491</td>
<td>0.471</td>
<td>0.409</td>
<td>0.450</td>
<td>0.456</td>
<td>0.436</td>
<td>0.429</td>
</tr>
<tr>
<td>-0.25</td>
<td>0.581</td>
<td>0.568</td>
<td>0.547</td>
<td>0.505</td>
<td>0.491</td>
<td>0.464</td>
<td>0.422</td>
<td>0.422</td>
<td>0.429</td>
</tr>
<tr>
<td>-0.50</td>
<td>0.547</td>
<td>0.526</td>
<td>0.491</td>
<td>0.433</td>
<td>0.415</td>
<td>0.367</td>
<td>0.360</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

of 32 Å for the five sites measured on the Nanospec film thickness measurement tool. The final wafer which was coated on the manual spin coater had an average resist thickness of 7744 Å and a range of 477 Å for five sites. This range was due to an area of thicker resist in the center of the wafer. Ignoring the center site (8101 Å), the four outer sites had an average thickness of 7655 Å and a range of 82 Å.

Site-by-site data for inside 0.5 micron vertical lines is given in Table 1. Figure 1 shows a CD versus focus/exposure plot for the inside feature as plotted by ProData. Numerical and graphical results for the outside 0.5 micron line are omitted since they matched those of the inside feature almost exactly. The average inside-to-outside difference was 0.00926 microns and the largest discrepancy was 0.041 microns.

SEM and operator measurement repeatability were tested by measuring a CD, leaving the site, and returning to measure the same CD. Six such measurements showed the SEM repeatability to be 0.043 microns or +/− 0.0215 microns. This number could have increased if more measurements had been taken.

4. ANALYSIS

The final wafer showed incorrect results at several center die due to poor across-wafer resist uniformity from manual spin coating. ProData rejected six data points (all center die locations) since they were statistically incorrect. These data points are plotted in Figure 1 but are not connected to they’re respective exposure trend. The final wafer had a thicker resist coating in the wafer center generally meaning more exposure energy would be necessary. This effectively makes the exposure energy delivered look smaller, a case of underexposure. Underexposed lines in positive resist should print larger than desired. However, the center die features printed smaller than expected. There is likely a more complicated swing curve interaction here. (Swing curves are caused by reflection of exposing light off the substrate back into the resist.) The swing curve for 0.5 micron lines has never been investigated since, until now, an adequate linewidth measurement tool such as the Hitachi CD-SEM has not been available.

The linewidth difference between the inside and outside 0.5 micron vertical line is within the noise level of the Hitachi S-6780’s measurement capability. SEM repeatability tests show a range in CD measurement of 0.043 microns or greater and the average and maximum inside to outside linewidth difference was 0.009 and 0.041 microns, respectively. The outside feature may actually print slightly differently than the inside feature, but the difference is negligible. Also, the outside feature does not adequately simulate an isolated feature.

Figure 2: EL versus DOF for Inside and Outside Feature

The ProData plot given in Figure 2 plots exposure latitude against DOF with separate trends for the inside and outside 0.5 micron vertical lines. Since the difference between these data sets is within the noise level of the CD-SEM, Figure 2 shows process latitude variation based on SEM measurement variation.
Table 2: Representative Data Sets from ProData

<table>
<thead>
<tr>
<th>Best Focus (um)</th>
<th>Best Exp (mJ/cm²)</th>
<th>DOF (um)</th>
<th>Exposure Latitude (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-0.07</td>
<td>149.94</td>
<td>0.00</td>
<td>42.53</td>
</tr>
<tr>
<td>-0.07</td>
<td>149.94</td>
<td>0.05</td>
<td>41.26</td>
</tr>
<tr>
<td>0.57</td>
<td>142.50</td>
<td>1.70</td>
<td>16.47</td>
</tr>
<tr>
<td>0.45</td>
<td>146.22</td>
<td>1.75</td>
<td>15.02</td>
</tr>
<tr>
<td>0.48</td>
<td>145.60</td>
<td>1.80</td>
<td>13.53</td>
</tr>
<tr>
<td>0.50</td>
<td>144.36</td>
<td>2.00</td>
<td>7.21</td>
</tr>
</tbody>
</table>

5. CONCLUSIONS

Focus and exposure settings directly determine the linewidth of the resist feature printed. A focus exposure matrix (FEM) may be used to optimize focus and exposure and to investigate depth of focus (DOF) and exposure latitude (EL). DOF and EL change inversely, so high DOF is bought at the cost of reduced EL and vice versa. The outside feature in a five feature set does not adequately simulate an isolated feature. The difference between the inside and outside 0.5 micron vertical lines was within the noise level of the Hitachi S-6780 CD-SEM. The data measured in this experiment was negatively impacted by poor resist uniformity due to a manual spin coater. Despite this, the FE settings used showed more than +/-10% CD variation and allows for adequately small changes in FE. The exposure was varied from 120 to 200 mJ/cm² in 10 mJ/cm² increments. Focus was varied from -0.5 to +1.5 microns in 0.25 micron increments. Since this experiment was performed on bare Silicon wafers (no devices or other processing), it is not useful to determine a “best process.”

REFERENCES


ACKNOWLEDGMENTS

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The author also acknowledges Dr. Bruce Smith and Dale Ewbank for guidance on this project. The author extends special thanks to Joe Perez for technical assistance with the Hitachi CD-SEM, Canon stepper, and SSI track and to Bruce Tolleson for assistance with and maintenance of the CD-SEM. The author would also like to extend special thanks to Canon for making special effort to repair RIT’s Canon FPA 2000-il in a timely manner despite the over-filled schedule of Canon repair technicians. Without this extra effort, completion of this project would not have been possible.

Jason L Burkholder, originally from Akron, PA, received the BS degree in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at Lucent Technologies in Reading PA, at Analog Devices in Cambridge MA, and at IBM in Burlington VT. He is joining IBM as a FEOL DUV lithography engineer starting in June 2000.
Investigation of Tantalum Silicon Oxide as an Attenuated Phase Shift Masking Material for 157nm Lithography

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Abstract- As the microelectronics industry trends toward 157nm lithography and device geometries shrink below 0.1μm, it seems more than likely that phase shift masking will be necessary as a means of optical enhancement. The attenuated phase shift mask is an attractive tool by which lithographers hope to push their art to its limits. However, potential materials for use as the attenuating film at wavelengths as low as 157nm have yet to be determined. There are several requirements that must be met by a material before it will be considered seriously for use on attenuating phase shift masks. One material that shows promise as a possible attenuating film is a compound film of tantalum silicon oxide, TaSiO. The rationale behind the selection of TaSiO as a material worthy for use on the technology in question will be presented, as will a preliminary overview of the characterization of the film's constituents, SiO2 and Ta2O5. The process by which a composite film with varying levels of Ta2O5 incorporation can be sputter deposited will be shown. Work that will have to be performed before the adoption or rejection of TaSiO as an APSM film will be discussed.

1. INTRODUCTION

The desire to push the limits of optical lithography has become more prevalent with the advent of 248 and 193nm systems. With the impending inception of 157nm lithography, the need to produce the dimensions necessary for advanced semiconductor technologies has facilitated the use of resolution enhancement techniques. One such technique is the phase shift mask, a subset of which is the attenuated phase shift mask (APSM). The latter has gained more attention in recent years because of the added ease of manufacturing over standard, alternating phase shift masks. The idea behind attenuated phase shift masking is a simple one, and yet the technique is very effective. This film is etched using a reactive ion etching process, creating a pattern analogous to that of a binary mask. However, the region shadowed by the attenuating film allows some amount of radiation to leak through, with transmission in the range of around 5-15%. This film also serves the purpose of the phase shifter by being engineered to a thickness that will create a π-phase shift between unobstructed and attenuated radiation from the source. It is this phase shift that produces very sharp, dark edges to features, allowing for increased resolution capabilities by taking the guesswork out of line/space differentiation by the resist. A graphical representation of what occurs as exposing radiation passes through the mask, is collected by the lens, and is sensed by the resist is shown in Figure 1. The APSM has also been shown to provide a significant increase in the useful depth of focus, which is a distinct benefit due to the trend toward shorter wavelengths and higher numerical aperture steppers.

A. Requirements of an APSM Film

The first and most elementary requirement for a phase shift masking film is that it deliver the desired 180° phase shift. The current tolerances on this requirement may be less than 1°. Assuming that the film is exactly the right thickness and understanding that the phase shift is therefore controlled by the refractive index of the phase shifting material, the requirement on refractive index control must be better than 0.6%[3]. This requires tight deposition condition restraints and etch rate/selectivity requirements. The attenuating film must also deliver the appropriate transmission characteristics. Again, this is an issue with producing a film that has the desired composition, since absorption, and therefore transmission, relies on the extinction coefficient of the composite film at a given wavelength. Both the phase shifting capabilities and the transmission properties of the APSM film must be controlled in order to deliver an aerial image to the resist that displays the characteristics of a maximizing image log slope while at the same time minimizing the printability of residual “lobes” in the areas shadowed by the attenuating
film. It is also desirable that the film reflectivity be kept below 15%. This reflectivity can be minimized by ensuring that the material in the composite film with the lower of the two refractive indices be the last to be deposited [4].

The ability of an APSM film to be patterned using reactive ion etch (RIE) techniques is another requirement. As device geometries are steadily being scaled down, the mask geometries must keep in step, requiring CD and uniformity control across the mask that is becoming more and more stringent. This points to plasma processing rather than wet etch techniques. The elimination of chrome from the mask, which is a distinct benefit of APSM over binary and alternating phase shift masks, makes this possible. The attenuating material must exhibit high etch selectivity between the film itself and the underlying substrate so that phase shifting requirements can be maintained, preserving the functionality of the system. Work that has been done previously on the etch characteristics of various APSM films will be presented in the section covering the feasibility of using TaSiO as an APSM material.

The chemical and radiation stability of the film to excimer laser exposure is a requirement that must be met by an aspiring APSM film. Any chemical or physical alteration that results from extended exposure to excimer laser radiation can eliminate a material for consideration in attenuating phase shift masking schemes. These alterations will most likely lead to changes in the optical properties of the film, an unacceptable situation for a mask with such tight restrictions set on its performance. When testing the radiation stability of the masking material, the attenuating film is subjected to pulsed radiation from an excimer laser (Ar ion laser in the case of 157nm). This is done for a long enough period of time that the test can effectively approximate the amount of radiation that the mask would see in a lifetime of heavy use. In order to isolate the effects of radiation damage, the transmittance and reflectance of the film is measured using ellipsometric techniques before and after the exposure. Tolerable exposure-induced transmission modification is near 0.5% [3], allowing very little room for chemical or physical change within the film to effect its optical properties.

B. The Selection of Ta$_5$Si$_2$O$_7$ as an APSM Film

Previous experiments have been performed at 248 and 193nm wavelengths on films that were chosen as potential candidates for APSM films. Among them were metal-rich metal nitrides (Zr/ZrN and Al/AlN), silicon-rich nitrides (Si$_3$N$_4$), nitride composites (TaN/Si$_3$N$_4$), and molybdenum silicon oxides (MoSiO). Tests were done on each of these to determine how suitable they would be for use as deep UV attenuating films. Reactive ion etch conditions were developed and analyzed for each. The radiation stability of these films in relation to the preservation of their optical properties was also explored.

Plasma RIE processes were previously explored for a number of materials for use at 193nm, among which were MoSiO and TaSiO, which etch in nearly the same way due to their similar compositions. Etch conditions were investigated using SF$_6$ and/or CF$_4$ with oxygen [2]. In the case of MoSiO etching, the chemical reaction that takes place involves the generation of volatile MoOF$_4$ and SiOF$_6$. Similar conditions could be used to etch TaSiO with the etch by-products being TaF$_6$ and SiOF$_6$, both of which are volatile at standard etch pressures and temperatures. The tantalum film exhibited higher selectivity to fused silica than the molybdenum film due to the greater transparency of Ta$_2$O$_5$ and the resulting lower SiO$_2$ content within the film. This ease of etching and relatively high etch selectivity of the TaSiO film makes it an attractive option for APSM applications from the RIE perspective.

The radiation stability of many of the films mentioned before have been previously investigated for applications at 248 and 193nm. It can be claimed that if a film does not meet stability standards set at these wavelengths, that they can provisionally be rejected from use at shorter wavelengths, since more damage is likely as wavelength decreases. The most common causes of radiation-related breakdown are cumulative damage mechanisms and oxidation effects within the film. It has been shown that metal-rich metal nitrides have a tendency to oxidize quite easily, greatly altering the optical properties of the material. In fact, after the pulsed laser test, the Zr/ZrN film was closer related to ZrO than ZrN when analyzing reflectance spectra. Past radiation damage experiments on a number of materials have led to one very important conclusion; understoichiometric metal nitrides, oxides, or oxynitrides are inherently unstable and prone to excessive oxidation [3]. The resulting transmission properties of the film are altered and this is intolerable. A material that proved to hold up to the pulsed laser experiment was the composite TaN/ Si$_3$N$_4$ film. No significant modification to the film’s optical properties was observed. This film is deposited as a multilayer stack of stoichiometric TaN and Si$_3$N$_4$, which is the cause of its relative stability. Films that are stoichiometric in nature, such as the multilayer stack of tantalum and silicon nitride, are inherently less prone to damage, which can be predicted from analysis of the film’s individual constituents [3]. Another benefit of the multilayer stack is the use of individual layer thicknesses that are significantly below the wavelength of exposing radiation. The components that make up the multilayer stack are deposited in thin (10Å or less) layers as the wafers pass under the target in the sputtering system. There is also some amount of interdiffusion that takes place on the wafer after layers are deposited on top of one another. The
result is a film that exhibits homogeneous optical behavior, which is often not the case with understoichiometric compounds. Extolling the benefits of multilayer stacks has a purpose, in that TaSiO is deposited in this manner. Something on the order of a single atomic layer of SiO2 is deposited on each layer of Ta2O5, resulting in a homogeneous film. It would be expected that a film of TaSiO would exhibit high stability to laser radiation because of the nature of the materials that compose it. This presents another benefit of using TaSiO as the attenuating film for phase shift masking applications; it can (more than likely) hold up against the day to day rigors of being subjected to excimer laser radiation.

Further benefits of selecting TaSiO as an APSM material involve its control of transmission properties. The transmission of the resulting composite film is manipulated by simply adjusting the sputter deposition conditions to tailor the amount of Ta2O5 incorporated in the film [1]. As more Ta2O5 is added to the film, the transmission decreases as a result of increased absorption from the higher extinction coefficient of the composite. If the sputter deposition used for putting down TaSiO is well controlled, the percent incorporation of Ta2O5 can be changed by simply calculating the power distribution needed at each of the targets. This also adds flexibility to the mask design, if it is discovered for instance that different transmission characteristics are desirable for specific structures.

2. EXPERIMENT AND RESULTS

Prior to an attempt to deposit a composite film, it was necessary to characterize the deposition process and optical properties of the constituent films. Blanket films of SiO2 and Ta2O5 were deposited on bare silicon wafers for this purpose. A Perkin Elmer rf magnetron sputter system, PE 2400 was used at a power of 500W. The deposition was carried out in an oxidizing ambient of 30sccm Ar with 10sccm O2. Pure targets of silicon and tantalum were used. In both cases, a base pressure of 1E-6Torr was achieved before flowing gas and performing the deposition. A fifteen minute pre-sputter was done to clean the targets prior to deposition as well. The deposition pressure was 4-5mTorr The films were deposited for 30 minutes. The film samples were then analyzed for optical properties using VUV spectroscopic ellipsometer. The data collected was then analyzed using WVASE software, with which the resulting film thicknesses, refractive indices, and extinction coefficients were determined. The SiO2 thickness was found to be 241Å and the Ta2O5 thickness was found to be 192Å, corresponding to deposition rates of 8.7Å/min and 6.4Å/min, respectively. The refractive index of SiO2 was determined to be 1.690, with an extinction coefficient of 0.005 at a wavelength of 157nm. The refractive index and extinction coefficient of Ta2O5 at 157nm were found to be 1.921 and 0.574. Plots that show the refractive indices and extinction coefficients of these two films as a function of wavelength can be found in Figures 2 and 3. These films were then combined within WVASE using an effective media approximation (EMA). A simulation of the film characteristics of an arbitrary combination of these two materials could be generated with this technique. Percent Ta2O5 incorporation in the sputtered SiO2 film was varied from 0-100%. The response of interest here was the resulting transmission of the composite film.

The theoretical refractive index (n) and extinction coefficient (k) of each composite film was extracted from the simulation. These values were then used to determine the theoretical thickness (t) at which the film would cause a π-phase shift, the absorption of the film (α), and the resulting transmission (T) [1]. This was done using the following equations:

\[ t = \frac{\lambda}{2(n-1)} \]
\[ \alpha = 4\pi k / \lambda \]
\[ T = e^{-\alpha t} \]

Table 1 contains selected theoretical TaSiO2 film compositions that would result in transmission values between 1% and 41%, more than encompassing any films that would be considered for attenuated phase shift masking applications.

Theoretical deposition conditions for a range of attenuating films were determined. These can be found in Table 2

3. CONCLUSIONS

An investigation was performed to determine the feasibility of using a tantalum silicon oxide film as an attenuating film for phase shift masking applications. The constituent films, SiO2 and Ta2O5, were deposited by sputtering metal targets in an oxidizing ambient and these films were analyzed using VUV ellipsometry. Theoretical composite films were simulated and their resulting optical properties were extracted. Theoretical deposition conditions were also determined

ACKNOWLEDGEMENTS

The author would like to acknowledge Bruce Smith for his help in devising the idea for the project and for providing some excellent research material. Further thanks go out to Matthew Lassiter, Michael Cangemi, and Anatoli Bourov, all of whom had a hand in instructing the author on machine operation necessary for the experiment.

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REFERENCES


Figure 1. The three plots above demonstrate the way in which the attenuated phase shift mask takes radiation at the mask and delivers it to the resist.
Malley, M.

18th Annual Microelectronic Engineering Conference, May 2000

Figure 2. Refractive index and extinction coefficient as a function of wavelength for an SiO₂ film.

Figure 3. Refractive index and extinction coefficient as a function of wavelength for a Ta₂O₅ film.
Table 1. TaSiO composite film composition for selected transmission values between 1 and 41%. The thicknesses shown are for the second π-phase shift thickness (total phase shift of 540°).

<table>
<thead>
<tr>
<th>%SiO2</th>
<th>%Ta2O5</th>
<th>n</th>
<th>k</th>
<th>Thickness for 180° Phase Shift (Å)</th>
<th>Transmission</th>
</tr>
</thead>
<tbody>
<tr>
<td>88</td>
<td>12</td>
<td>1.719</td>
<td>0.068</td>
<td>3275.4</td>
<td>41.01%</td>
</tr>
<tr>
<td>87</td>
<td>13</td>
<td>1.721</td>
<td>0.072</td>
<td>3266.3</td>
<td>39.02%</td>
</tr>
<tr>
<td>86</td>
<td>14</td>
<td>1.725</td>
<td>0.078</td>
<td>3248.3</td>
<td>38.28%</td>
</tr>
<tr>
<td>85</td>
<td>15</td>
<td>1.727</td>
<td>0.084</td>
<td>3239.3</td>
<td>37.66%</td>
</tr>
<tr>
<td>84</td>
<td>16</td>
<td>1.731</td>
<td>0.089</td>
<td>3221.6</td>
<td>31.74%</td>
</tr>
<tr>
<td>83</td>
<td>17</td>
<td>1.734</td>
<td>0.096</td>
<td>3208.4</td>
<td>29.15%</td>
</tr>
<tr>
<td>82</td>
<td>18</td>
<td>1.736</td>
<td>0.101</td>
<td>3199.7</td>
<td>27.44%</td>
</tr>
<tr>
<td>81</td>
<td>19</td>
<td>1.738</td>
<td>0.107</td>
<td>3191.1</td>
<td>25.50%</td>
</tr>
<tr>
<td>79</td>
<td>21</td>
<td>1.741</td>
<td>0.117</td>
<td>3178.1</td>
<td>22.58%</td>
</tr>
<tr>
<td>78</td>
<td>22</td>
<td>1.744</td>
<td>0.123</td>
<td>3165.3</td>
<td>21.05%</td>
</tr>
<tr>
<td>77</td>
<td>23</td>
<td>1.747</td>
<td>0.13</td>
<td>3152.6</td>
<td>19.39%</td>
</tr>
<tr>
<td>75</td>
<td>25</td>
<td>1.753</td>
<td>0.141</td>
<td>3127.5</td>
<td>17.12%</td>
</tr>
<tr>
<td>73</td>
<td>27</td>
<td>1.755</td>
<td>0.152</td>
<td>3119.2</td>
<td>15.00%</td>
</tr>
<tr>
<td>71</td>
<td>29</td>
<td>1.762</td>
<td>0.163</td>
<td>3090.6</td>
<td>13.32%</td>
</tr>
<tr>
<td>68</td>
<td>32</td>
<td>1.767</td>
<td>0.18</td>
<td>3070.4</td>
<td>10.95%</td>
</tr>
<tr>
<td>66</td>
<td>34</td>
<td>1.773</td>
<td>0.192</td>
<td>3046.6</td>
<td>9.82%</td>
</tr>
<tr>
<td>65</td>
<td>35</td>
<td>1.776</td>
<td>0.197</td>
<td>3037.6</td>
<td>9.11%</td>
</tr>
<tr>
<td>61</td>
<td>39</td>
<td>1.785</td>
<td>0.219</td>
<td>3000.0</td>
<td>7.21%</td>
</tr>
<tr>
<td>55</td>
<td>45</td>
<td>1.797</td>
<td>0.261</td>
<td>2984.6</td>
<td>5.14%</td>
</tr>
<tr>
<td>46</td>
<td>54</td>
<td>1.818</td>
<td>0.306</td>
<td>2879.0</td>
<td>2.94%</td>
</tr>
<tr>
<td>27</td>
<td>73</td>
<td>1.86</td>
<td>0.419</td>
<td>2738.4</td>
<td>1.01%</td>
</tr>
</tbody>
</table>

Table 2. Deposition conditions that would produce films with transmission values of 5, 10, 15, 20, and 25% at thicknesses that would exhibit the desired phase shifting characteristics.
Effects of Nitrogen Implantation on Oxide Growth and Quality

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Abstract—The effects of implanting nitrogen prior to gate oxidation are presented. Three different doses of N\(^+\), N\(_2\)^\(^+\), and Si\(^+\) were implanted, followed by a 20-minute 950\(^\circ\)C dry oxide growth. Growth rate, interface quality and breakdown strength were measured. Results show up to a 70% reduction in growth rate for high dose nitrogen implants, but no change for silicon implants. The interface trap density decreased with increasing dose for all three species. Oxides grown over N\(_2\)^\(^+\) implanted silicon showed field strengths comparable to standard oxides.

1. INTRODUCTION

The gate oxide is critical to MOSFET performance. Modern devices demand an ultrathin (<3nm) oxide with low fixed charge and interface trap densities, hot carrier and boron diffusion resistance, and high breakdown strength. As device dimensions and the gate oxide thickness are scaled down, it becomes increasingly difficult to grow high quality oxides that meet these performance criteria.

For several years, it has been known that incorporating nitrogen into the gate oxide can produce beneficial effects, namely improved resistance to boron diffusion and hot electrons [1]. Traditionally, nitridation has been done using N\(_2\)O, NO, or NH\(_3\) ambient during or after oxide growth [2]. However, these methods suffer several shortfalls. With NH\(_3\), the excess hydrogen can create trap sites [3]. For this reason, N\(_2\)O and NO are usually used. But the incorporation rate for these two gases depends highly on the temperature and the flow rate [4], leading to process variation. Furthermore, the amount of nitrogen that can be incorporated with N\(_2\)O and NO is relatively low [2]. Nitrogen implantation prior to oxidation has been suggested as an alternative method of nitridation [5]. Because the nitrogen is implanted, the dose can be precisely controlled, and much higher doses can be achieved. In addition, oxides grown over nitrogen implanted silicon exhibit much lower growth rates [5-10]. The decreased rate is beneficial because it allows for longer oxidation times, improving process control, and higher temperatures, increasing quality. One study of oxides grown after nitrogen implantation shows an improvement in breakdown strength for medium nitrogen doses [9]. In addition, nitrogen can be selectively implanted into devices to enable a multiple gate CMOS process [10]. Areas implanted with nitrogen will have thinner oxides than those that don't, giving rise to different threshold voltages. Novel designs that could not be made previously can be fabricated using this approach.

The intent of this experiment was to explore the effects of implanted nitrogen on the oxide growth rate and quality. Three implanted species were examined: N\(^+\) (amu 14), N\(_2\)^\(^+\) (amu 28), and Si\(^+\) (amu 28). The silicon implant was done to determine if implant damage causes the reduced oxidation rate. Since it has a similar atomic mass to N\(_2\), it should produce a similar damage profile. A SemiTest SCA-2500 was used extensively to study the interface quality. It has the ability to measure interface trap density, surface substrate doping, minority carrier lifetime, fixed oxide charge and flatband charge through the use of what is essentially an electro-optical C-V measurement.

2. EXPERIMENTAL

Nine p-type <100> 10 ohm-cm wafers were used. An 85nm screening oxide was grown prior to implant. Surface charge analysis was done using a SemiTest SCA-2500 to obtain a baseline. Photoresist was coated on the wafers and then the resist on half of each wafer was exposed and developed away. This protected one side of the wafer from implant. By implanting only one half of the wafer, direct correlations could be made between the implanted and non-implanted sides.

SRIM simulation software was used to determine appropriate ion energies for each species. The implant was targeted so that the peak would occur at the oxide interface, for a maximal effect. It was assumed that N\(_2\)^\(^+\) behaves similarly to Si\(^+\), since SRIM can only simulate monatomic species. Table 1 lists the doses and energies used. Note that the N\(^+\) dose was twice that of the N\(_2\)^\(^+\) so that the same amount of nitrogen was incorporated.

After implantation, the resist was stripped with hot Nanostrip and an RCA clean was done. The highest dose Si\(^+\) wafer was accidentally broken in this step, which left it unsuitable for measurement with the SCA. The screening
oxide was stripped with buffered HF, followed by an RCA clean.

To ensure a good interface, special care was taken during the cleans. The clean tanks were rinsed thoroughly with DI water, then a diluted HCL mixture was poured into the tanks to remove metallic contaminants. The HCl mixture was allowed to sit in the tanks for about 20 minutes then the tanks were rinsed again. Fresh P-Lo chemicals from Ashland Chemical were mixed for the APM and HPM baths. The ratio for the APM bath was 16:3:1 H₂O:H₂O₂:NH₄OH. The HPM bath was mixed 16:3:1 H₂O:H₂O₂:HCl. The temperature for both baths was kept at a fairly low 65-70°C to minimize surface roughening. Particle counts were taken with a Tencor Surfscan before and after cleans to monitor their effectiveness.

Immediately prior to oxidation, a TCA clean was done on the furnace tube and quartz wafer boat at 1050°C for 15 minutes. This helped remove any possible metallic contaminants. A 20-minute nitrogen purge was done after the clean to flush the chlorine from the system.

A 20-minute, 950°C dry oxidation followed by a 20-minute argon anneal at 950°C was performed on the nine half-implanted wafers. The wafers were pushed and pulled at 700°C to limit atmospheric oxide growth. The oxide thickness was measured using an ellipsometer, and the SCA was used to make 37-point maps of the wafers. Maps for the doping concentration, defect density, flat band charge, and carrier lifetimes were obtained.

Aluminum was evaporated onto the medium and high dose nitrogen implanted wafers to make capacitors for breakdown strength characterization. However, aluminum adhesion problems were encountered, so the aluminum was stripped and the wafers were recleaned. The HF dip step in the RCA clean was eliminated to preserve the oxide thickness. To drive the water from the oxide, the wafers were annealed in argon for 1 hour at 900°C. The oxide thickness was remeasured and new SCA maps were made. It was found that the wafers lost approximately 10-15Å of oxide after this processing. This left the wafer with the highest dose of N⁺ with an oxide deemed too thin (<3.5nm) to perform breakdown tests on.

To make the capacitors, aluminum was sputtered on the highest dose N⁺ wafers and medium dose N⁻ wafer using the CVC-601 sputterer. Shadow masks with 37, 35mm holes were used to pattern the aluminum. To help prevent plasma damage to the oxide, a low power 500W sputter was done for 5 minutes, followed by a 40 minute sputter at 1000W. After sputtering it was observed that the shadow masks had shifted during the run, producing small streaks of aluminum instead of perfect circles. This effect was especially bad on the medium dose N⁻ wafer, so it was removed from breakdown strength testing.

The sputtered capacitors were covered with resist so the backside oxide could be etched. Buffered oxide etch was used. To ensure a good backside contact, aluminum was sputtered on the backs of the wafers at 2000W for 20 minutes. The wafers were then sintered at 410°C for 20 minutes in forming gas (H₂:N₂).

Dielectric breakdown strength was measured on the medium and high dose N⁺ wafers using a Hewlett Packard 4145B Semiconductor Parameter Analyzer. This test was performed by sweeping a voltage across the oxide and measuring the current; a vertical jump in the current indicated a breakdown. A current limiting resistor was placed in series with the MOS capacitor. This resistor, along with the other resistances in the circuit, created an IR curve that could be superimposed over the breakdown curve. The breakdown voltage was measured by measuring the voltage difference between the IR curve and the point of breakdown.

<table>
<thead>
<tr>
<th>Species</th>
<th>Doses (ions/cm²)</th>
<th>Energy (keV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N⁺</td>
<td>2E14, 8E14, 2E15</td>
<td>32</td>
</tr>
<tr>
<td>N₂⁺</td>
<td>1E14, 4E14, 1E15</td>
<td>58</td>
</tr>
<tr>
<td>Si⁺</td>
<td>1E14, 4E14, 1E15</td>
<td>58</td>
</tr>
</tbody>
</table>

2. RESULTS AND DISCUSSION

A. Oxidation

Figure 1 shows the oxide thickness plotted versus dose for each species. Note that the nitrogen dose is plotted as the actual number of atoms incorporated, rather than implant dose. This graph shows that the oxidation rate decreased substantially with the higher doses of nitrogen. The N⁺ implant caused the largest effect, resulting in a 70% decrease in growth rate. The silicon implant had virtually no effect, which means that the decrease in growth rate is not due to implant damage. It is not known why there are differences between the N⁺ and N₂⁺ implants. It is possible that the implant peaks were shifted away from the oxide interface. Additional studies, such as SIMS analysis, need to be conducted to determine the implant profiles.

These results compare favorably to previously published reports [5-10], however, oxide growth rates vary widely. Liu et al. [6], Lopez [7] and Wescott [8] observed larger reductions in growth rate with smaller doses. The results obtained in this experiment most closely match those of Kurucan et al. [9] and Soleimani et al. [5]. The Soleimani group did a deep N₂⁺ implant (0.1μm) followed by an anneal to pile-up the nitrogen at the screening oxide interface. The screening oxide was then stripped and the gate oxide was grown. The reported growth rates appear to be related to the initial implant profile. Again, more analysis needs to be conducted to determine how the profile affects growth rate.
B. Interface Quality

The 37-point SCA wafer maps were used to analyze the changes in interface quality. Because the wafers were only half implanted, direct differences could be observed on some of the wafers. Figure 2 shows the change in interface trap densities ($D_A$) versus dose. As shown, all three species produced a change, with $D_A$ generally trending downward with increasing dose. Surprisingly, the silicon implant had the largest effect, followed by the $N_2^+$. The effect of the $N^+$ was relatively small. The implants appear to be passivating the surface states. The passivating effects of nitrogen have been observed in $N_2O$ growth [11]; however, it is unknown why the silicon appears to be doing the same. It is possible that implant damage is a factor.

Figure 3 shows the change in surface substrate doping ($N_{w}$) versus dose. The initial substrate doping for all wafers was approximately $4 \times 10^{14}$ cm$^{-3}$. All three species caused a decrease substrate doping with increased dose. Again, the silicon showed the strongest effect followed by the $N_2^+$ and the $N^+$. It is likely that the substrate doping is not changing this substantially, but some other effect is causing the SCA to report it as such.

C. Dielectric Strength

Figures 4 and 5 show cumulative percentage plots of the breakdown strength of oxides grown over the medium and high dose $N_2^+$ implants versus oxides grown over the non-implanted silicon. The nitrided oxides showed breakdown strengths similar to the standard oxides. However, the nitrided oxides were thinner. It is speculated that if similar thicknesses were compared, the nitrided oxides would show higher breakdown strength. Kurinec et al. [12] found significant improvements in dielectric strength in $12nm$ oxides for medium doses ($5 \times 10^{14}$ ions/cm$^2$) of $N^+$. Doses at and above $1 \times 10^{15}$ ions/cm$^2$ showed poor dielectric strength, possibly due to heavy implant damage.

A large percentage of the tested capacitors were shorts. This is probably due to the large area of the aluminum streaks used for capacitors. Thus, there was a high probability of a defect being present in the oxide. Further studies need to be done with smaller capacitor areas.

3. CONCLUSIONS

Nitrogen implantation can be beneficial when growing thin oxides. $N^+$ or $N_2^+$ doses in the range of $4 \times 10^{14}$ to $2 \times 10^{15}$ have been shown to significantly reduce the oxidation rate, which can improve process control. Furthermore, results indicate some improvements to oxide quality as well, with reductions in interface trap density observed in implant doses above $1 \times 10^{15}$ ions/cm$^2$. Dielectric strength is at a minimum consistent with standard oxides.

REFERENCES


5. ACKNOWLEDGMENTS

The author would like to thank Dr. Michael Jackson and Dr. Santosh Kurinec for their support and guidance throughout the course of this experiment.

Jason Meiring, originally from FORT RECOVERY, OH, received a B.S in Microelectronic Engineering from the Rochester Institute of Technology in 2000. He attained co-op experience at Xerox Corp., Atmel Corp., and Motorola. He will be pursing a Ph.D. in Chemical Engineering at The University of Texas at Austin stating August 2000.
* Dose is reported as a function of the actual number of atoms incorporated, instead of the implant dose.
Abstract—A Tantalum Pentoxide deposition by reactive sputtering was optimized on a CVC-601 sputterer and working MOS transistors were made using Tantalum Pentoxide. The target was an 8" pure Tantalum target. The optimization was done over a power range of 700 to 1700W DC and over an Oxygen flow of 15 to 35%. The optimal process from this study was at 1200W and an Oxygen flow of 15% or less. A standard PMOS process was modified to use Tantalum Pentoxide using the gate dielectric. The resulting transistors worked well.

1. INTRODUCTION

Tantalum pentoxide is a material that has received much attention from microelectronics researchers over the past few decades. The regions of interest have been its dielectric properties, its optical properties, and its chemical properties.[1] The high dielectric constant (typically in the range of 20 to 25) makes it desirable for capacitor and gate dielectrics as devices are scaled down to smaller and smaller dimensions. The high refractive index (greater than 2.0) have made it of interest for mirrors, waveguides, and other optical devices and structures. The chemical resistance it displays has seen it being used as etch barriers in various studies. Many different methods and combinations of methods, including thermal oxidization, anodization, chemical vapor deposition, and sputtering, have been used to deposit tantalum pentoxide.[2] The low temperature deposition and the ease of implementation of sputtering have made it the focus of this experiment. More specifically, the DC reactive sputtering of a tantalum target in a partial ambient of oxygen was explored and optimized for dielectric properties.

The optimization was performed on a CVC-601 operating in DC mode with an 8" tantalum target. Initial runs were made to establish a good design space before establishing the design. The design that was chosen was a central composite design (CCD) because it can detect quadratic effects and it has the spreads the design to five levels while maintaining a reasonable amount of runs. The parameters that were varied as factors in the CCD were power and percentage of oxygen flow (as compared to the total flow of argon and oxygen). The responses that were observed were breakdown voltage, leakage current, and dielectric constant. These were tested by making capacitors with the heavily doped p-type silicon substrate, the film, and aluminum. Other responses that were observed were film thickness and refractive index.

In addition to the design of experiments, MOS devices and capacitors for gallium arsenide were planned to be made and tested with the optimized film. For MOS devices, the higher dielectric constant of tantalum pentoxide could allow for smaller effective gate dielectric thicknesses than currently possible with silicon dioxide. An established MOS device process was used up to the gate oxidization. The tantalum pentoxide film was then deposited in place of the gate oxide. The processing continued with the addition of a CHF₃ RIE etch to pattern the contact cuts through the tantalum pentoxide film. The MOS devices were made in conjunction with Dave Rines' senior project. The resulting devices were made on wafers that had received a nitrogen implant on half of the wafer. This could potentially help reduce silicon dioxide formation at the interface between tantalum pentoxide and silicon. Capacitors are used on gallium arsenide substrates to supplement and control optoelectronic devices. For gallium arsenide, the processing temperature is limited because of the outgassing of arsenic. The sputtering of tantalum pentoxide has a low enough temperature to be compatible with gallium arsenide processing.[3] Tantalum pentoxide could reduce the area of the capacitors on these substrates.

2. DEPOSITION OPTIMIZATION PROCESS

The process that was to be used for the deposition was established before any of the DOE runs were done. The process started with 4" heavily doped p-type Silicon substrates. These substrates acted as the bottom electrode for the test capacitors. The Si substrates were dipped in buffered oxide etch (BOE) for 30s, DI rinsed and spin rinse dried (SRD) just before being put into the sputtering chamber. This was done to get rid of any native oxide. The sputtering was pumped down to the low 10⁻⁵ to high 10⁻⁶ Torr range. The CVC-601 was operated with a pulsed DC power supply set at the desired power. The heater was
turned on during the run to help densify the film. The substrates made a complete revolution around the chamber every 15s. The total gas flow of the Argon and Oxygen was held at 200sccm while the percentage of Oxygen was changed run to run. This equated to pressures of about 6.2mTorr. After everything was set up, a 10 minute presputter was done before the 30minute deposition. After the deposition was complete, the wafers were again dipped in BOE, rinsed, and dried before the Aluminum top electrode layer was sputtered. The a capacitor test mask was used to pattern the capacitors with a standard g-line photolithography process. The Aluminum was etched in heated Aluminum etch. The wafers were then stripped of the resist and SRDed. The backside Aluminum was then sputtered. No sintering step was used because there is evidence that the smaller metallic and semiconductor elements such as Si and Al diffuse into the Ta2O5 film and decrease the quality of the film.

3. TESTING

The film thickness and refractive index were measured after deposition with an ellipsometer. The dielectric constant, breakdown voltage, and the leakage current were measured in the test area after the devices were completed. All of the device testing was done on the smallest round capacitors, which were 100,000 microns square in area.

The capacitance of several devices on a wafer were measured on a CV analyzer. The capacitance, the area, and the film thickness were used to find the dielectric constant using the following equation.

\[
\varepsilon_r = \frac{C \cdot t}{\varepsilon_0 \cdot A}
\]

Where \(C\) is the capacitance, \(t\) is the film thickness, \(A\) is the area, \(\varepsilon_0\) is the absolute dielectric permittivity, and \(\varepsilon_r\) is the relative dielectric permittivity or the dielectric constant.

4. DOE RESULTS

The results from the testing are shown in Table 2. The leakage current was left out due to troubles with testing for it. This was a surprise due to the fact that film was expected to be very leaky. The breakdown voltages were higher than were expected, but the dielectric constants were lower than expected. The refractive index was in the expected range.

The results were analyzed with RS/1. From this analysis the peak breakdown voltage should be around

Table 2. DOE Results

<table>
<thead>
<tr>
<th>Run #</th>
<th>(t) avg. (m)</th>
<th>(n_i) avg.</th>
<th>(\varepsilon_r)</th>
<th>strength (V/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7.74E-08</td>
<td>2.085</td>
<td>1.33E+01</td>
<td>5.49E+06</td>
</tr>
<tr>
<td>2</td>
<td>1.50E-07</td>
<td>2.036</td>
<td>1.75E+01</td>
<td>6.65E+06</td>
</tr>
<tr>
<td>3</td>
<td>7.20E-08</td>
<td>2.065</td>
<td>1.22E+01</td>
<td>7.08E+06</td>
</tr>
<tr>
<td>4</td>
<td>1.29E-07</td>
<td>2.072</td>
<td>1.52E+01</td>
<td>6.98E+06</td>
</tr>
<tr>
<td>5</td>
<td>6.26E-08</td>
<td>2.065</td>
<td>1.15E+01</td>
<td>6.43E+06</td>
</tr>
<tr>
<td>6</td>
<td>1.65E-07</td>
<td>1.939</td>
<td>1.88E+01</td>
<td>6.07E+06</td>
</tr>
<tr>
<td>7</td>
<td>1.16E-07</td>
<td>2.095</td>
<td>1.61E+01</td>
<td>7.83E+06</td>
</tr>
<tr>
<td>8</td>
<td>9.67E-08</td>
<td>2.09</td>
<td>1.35E+01</td>
<td>7.06E+06</td>
</tr>
<tr>
<td>9</td>
<td>1.03E-07</td>
<td>2.101</td>
<td>1.34E+01</td>
<td>7.79E+06</td>
</tr>
<tr>
<td>10</td>
<td>1.07E-07</td>
<td>2.092</td>
<td>1.59E+01</td>
<td>7.24E+06</td>
</tr>
</tbody>
</table>
The analysis also showed the dielectric constant to be increasing from these results the best film parameters would be much oxygen getting into the film decreasing oxygen flow. These both could be due to too much oxygen getting into the film with these settings. From these results the best film parameters would be 1200W and 115% or less flow of Oxygen

5. MOS APPLICATION

For the MOS devices, the film was deposited on wafers that had been implanted with Nitrogen on one half and processed up to the gate oxide step. On one wafer, a 420 Angstrom layer of Ta2O5 was deposited at 1200W and 25% Oxygen flow. The film was then annealed at 750C for 5 minutes in dry Oxygen in a furnace tube. The anneal was done to improve the film quality. Another wafer received an additional 80 Angstrom layer of Ta2O5 on top of the annealed layer to help prevent possible migration of Al during the sinter step. Contact cuts were then etched through the Ta2O5 (after contact cut photolithography) in a CHF3 RIE step. The RIE step was developed on a Drytek Quad Etcher from published papers to have a favorable selectivity to resist.[5] The gas flow was 50sccm and the power was 350W. The resulting etch rates were 150 Angstroms/minute for Ta2O5 and 200 Angstroms/minute for Shipley 812 positive resist.

After this step, the processing continued as normal. The resist was removed. The Aluminum was deposited, patterned, and sintered.

The devices were tested using the standard PMOS test setup with a wafer prober and an HP4145. Family of curves, linear VT, and linear subthreshold plots were made for both sides of each wafer. The general results showed higher gains and lower thresholds than the normal process. The nitrogen implanted sides actually had higher thresholds than the non implanted sides. This was opposite to the results that Dave Rines observed in his SiO2 gate PMOS. A set of plots from the nitrogen implanted side of the wafer with a single layer of Ta2O5 can be seen in Fig. 2, 3, and 4. This set of devices was the only one that demonstrated the best subthreshold plot. The rest were mostly noisy at the leakage regime. The characteristics of these particular films were not tested so expected results for threshold could not be accurately calculated.

6. CONCLUSIONS

The development and optimization of the Tantalum Pentoxide deposition process was a success. The base process is now ready to be applied to future research and applications. The basic process is at 1200W and 15% Oxygen flow.

The demonstration of MOS devices with Tantalum Pentoxide as a gate dielectric was also successful. The devices worked well. The GaAs capacitors were not made however.

There is much room for future work with both the process and the applications. For the process, the Oxygen flow could be reduced even more to try to get better films. Other parameters such as pressure could also be varied to find better results. Anneal steps could also investigated as ways of improving the film quality. For the MOS applications, thinner films and more exhaustive testing could be done, especially in regards to the nitrogen...
implants. The GaAs capacitors could be made and tested. Optical applications and MEMs applications could be looked at as well.

REFERENCES


ACKNOWLEDGMENTS

The author acknowledges Dr. Santosh Kurinec guidance in this work, Dr. Mike Jackson for guidance in the device testing, Dave Rines for Nitrogen implanted PMOS wafers, and Rich Battaglia for the maintenance of and assistance with the CVC-601 sputterer.

Mark A. Bossard, originally from Upper Marlboro, MD, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at the National Security Agency. He is joining Atmel Corporation as a design engineer starting in June of 2000.
MOSFETs with Variable Gate Oxide Thickness by Selective Nitrogen Ion Implantation

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Abstract- The incorporation of nitrogen in silicon has been shown to retard the oxidation growth rate. The present study produced aluminum gate PMOSFETs with varied gate oxide thickness on the same chip through selective nitrogen ion implantation. The nitrogen implant dose of $4 \times 10^{14}$ ions/cm$^2$ at 35 keV prior to gate oxide growth reduced the oxidation rate between 10% and 60% at the oxidation schedules employed. This active area N-implant led to no degradation in electrical parameters such as gate delay, mobility, or subthreshold swing. MOSFETs with different gate oxide thicknesses allow for different threshold voltages on the same chip and increased non-minimum channel length MOSFET reliability.

I. INTRODUCTION

Current trends in industry are leading to system on a chip solutions. These solutions generally require varied devices to perform many different functions. The integration of different voltage bipolar junction transistors has been developed, but MOSFETs have not yet crossed this technological river, as MOSFET threshold voltage is primarily determined by the blanket processed gate oxide thickness and composition.

Gate oxide thickness is generally scaled down with channel length. This gate oxide thickness reduction leads to reliability issues associated with thin oxides. Nitrogen implantation in Si prior to oxidation has been shown to retard oxidation rate in thin oxide regime [1]. Selective nitrogen ion implantation would allow long channel MOSFETs devices to have thicker gate oxides than minimum length transistors on the same chip. This would lead to enhanced chip reliability. Direct thermal incorporation of nitrogen in gate oxide growth steps has been standard practice in industry for some time.

The nitrogen in the SiO$_2$ film improves dielectric strength, acts as an impurity diffusion inhibitor, and reduces hot-carrier effects in submicron MOSFETs [2]. Previous work examined the kinetics and reliability of N-implanted and Si-implanted SiO$_2$ gate dielectrics. Data showed increased dielectric strength and decreased thickness uniformity for N-implanted SiO$_2$ [3]. This study fabricated aluminum gate PMOSFETs with N-implanted gate oxides. The fabricated PMOSFETs have two different gate oxide thicknesses on each wafer. The standard RIT aluminum gate PMOS process was run on n-type wafers with resistivity in the range of 10-30 ohm cm. The standard process involves four photo steps namely Source/Drain, Active, Contact Cut, and Metal. An additional photo step to selectively block the nitrogen implant was introduced prior to gate oxide growth. Nitrogen was implanted at a dose of $4 \times 10^{14}$ ions/cm$^2$ and at an energy of 35 keV. This energy and dose had been optimized by a previous study [4].

The gate oxide growth process resulted in a thickness differential between masked and unmasked active regions. The standard process grows a 700Å thermal SiO$_2$ gate dielectric. This study grew thermal oxides between 55Å and 675Å. These results can be seen in Figure 1. Oxides were grown in dry oxygen between 900 and 1050 degrees Celsius for eight to thirty minutes. All oxide growth recipes included a nitrogen anneal ramp down cycle.

![Figure 1. Oxide thickness obtained on un-implanted and N-implanted regions.](image-url)
devices were then tested using an HP4145 parameter analyzer.

3. RESULTS AND DISCUSSION

PMOS transistors with different threshold voltage magnitudes and transconductance have been realized on the same chip. The threshold voltage was found by extrapolating the x-intercept of the linear fit to the transfer characteristic—drain current versus gate voltage at a drain-source voltage of –0.1 V as shown in Figure 2. The figure shows two distinctly different characteristics of the same size PMOS devices fabricated on each wafer. The threshold voltage of a PMOSFET is given by

\[ V_t = \phi_{ms} - Q_o/C_{ox} - 2(\phi_f + 6\phi_i) \]

\[ - \sqrt{(2q\phi_o N_D)(2\phi_f + 6\phi_i)} / C_{ox} \] (1)

Where \( \phi_{ms} \) is the metal semiconductor work function difference, \( Q_o \) is the oxide charge density in C/cm\(^2\) associated with the SiO\(_2\)/Si interface, \( C_{ox} \) is the oxide capacitance in F/cm\(^2\), \( \phi_f \) is the Fermi potentials and \( \phi_i \) is the thermal potential, \( N_D \) is the substrate (channel) doping density. The magnitude of the threshold voltage varies almost linearly with the oxide thickness.

The slope of the threshold voltage versus oxide thickness plot can be written as

\[ \text{Slope} = \left( \frac{\sqrt{(2q\phi_o N_D)(2\phi_f + 6\phi_i) + Q_o)} }{ \varepsilon_{ox} } \right) \]

and the intercept on the y-axis gives the value of \( \phi_{ms} - [2\phi_f + 6\phi_i] \).

The experimentally observed threshold voltages have been plotted with the corresponding gate oxide thickness for un-implanted and nitrogen implanted devices in Figure 3. A fairly good linear fit to the data is obtained for both un-implanted and N-implanted devices. It can be observed that for lower substrate doping and lower oxide charge density, the threshold voltage is insensitive to the change in oxide thickness[3]. The wafers employed in the present study correspond to a doping density of 1.5X10\(^{14}\) cm\(^3\).

**Transfer Characteristics**

(20x80 PMOSFET, Wafers D4 & D5, Center Site, Vds = -0.1V)

![Figure 2](image-url)  
Figure 2. Drain current versus gate voltage for the drain-source voltage of -0.1V for identical size PMOS devices on the same wafer with different oxide thicknesses.
From the calculated data shown in Figure 4, it can be seen that at this doping level, the magnitude of the threshold voltage should be essentially independent of the gate oxide thickness. It is inferred that the slope observed in Figure 3 is primarily due to the presence of appreciable oxide charge density. SUPREM simulations show that the piling up of phosphorus at the SiO₂/Si interface at the substrate doping employed is not expected to a significant effect. Assuming the effect of oxide charges alone, an interface oxide charge density of 4X10¹¹ q/cm² has been estimated.

Detailed analysis of PMOS electrical characteristics did not resolve nitrogen implant induced variation in hole mobility, subthreshold swing, or gate delay as shown in Figures 5, 6, & 7.

Figure 3. Threshold voltage versus gate oxide thickness

Figure 5. Calculated hole mobility of un-implanted and N-implanted devices

Figure 6. Subthreshold Swing for un-implanted and N-implanted devices

Figure 7. Ring oscillator time delay on both type devices.
4. CONCLUSION

Aluminum gate PMOSFETs with two different gate oxide thicknesses, threshold voltages, and transconductances were fabricated on the same chip. This selective nitrogen implant process gives the IC design team more device flexibility, and enhances non-minimum channel length MOSFET reliability. In addition, the RIT aluminum gate PMOS process has been shown to be effective with a gate oxide thickness down to about 10 nm.

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Design and Fabrication of Ring Gate Surface Junction Tunneling Devices

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Abstract—Silicon based ring gate surface junction tunneling devices (SJT) were studied due to their promise of incorporating quantum functional devices with integrated circuits. SJT devices of various gate lengths ranging from 1 μm to 50 μm were designed using Mentor Graphics tools, and were fabricated using standard CMOS processes on SIMOX substrates. SIMOX wafers were used to help reduce bulk leakage and enhance the drain impurity profile. SIMOX mesa isolation also significantly reduced the process flow.

1. INTRODUCTION

Recent advances microelectronic technology has reduced device gate lengths to 0.15 μm and below. At these dimensions, effects such as tunneling become significant. Current efforts to reduce these effects usually focus on minor modifications to materials and device structure. The surface junction tunneling device, on the other hand, attempts to utilize tunneling instead of overcoming it.

The silicon based SJT is a three terminal device that operates as a gated tunnel diode. As with other tunneling devices, the SJT exhibits a negative differential resistance (NDR) characteristic curve. Though the SJT differs from these compound semiconductor devices due to its silicon substrate and processing. The advantages over ordinary MOS devices are realized in its high speed and low power consumption.

Similar to a conventional n-channel MOSFET, the SJT employs a source, gate, and drain. The difference lies in the p+ doping of the drain. Applying sufficient positive gate bias will cause the channel to form a p+/n+ tunnel junction that is similar in principle to those studied by L. Esaki. While ordinary Esaki diodes will result in a single NDR curve under positive drain to source biasing, the SJT will result in a family of curves. This is due to the modulation of surface charge density with gate bias. As a result, the gate can control the tunnel current and negative resistance.

2. THEORY AND DESIGN

As mentioned, the SJT is similar in principle to an Esaki junction tunnel diode. Though the formation of the junction is controlled by the gate and can be characterized by ordinary device physics equations, the junction phenomena is identical to that of an Esaki diode.

When p+ and n+ regions are heavily doped to degeneracy, a very abrupt junction is formed and results in a depletion layer of 10 nm or less. This depletion layer is the barrier through which the electrons tunnel.

![Figure 1: Band diagram for tunneling condition.](image-url)

Figure 1 shows the band to band tunneling for the device in the forward biased condition. Band to band tunneling will occur as the drain bias is increased from zero volts. This will continue until a drain to source voltage is reached in which tunneling will no longer occur. At this point, termed the peak, the drain current begins to sharply fall off until it reaches a minimum, the valley. In this negative resistance region, the SJT derives its usefulness. Due to the relative ease of varying the drain voltage, the SJT has very fast switching speeds due to the short transit times for electrons across the tunnel barrier. The tunneling current density can be found using the following equation.

\[ J_T = J_S \exp \left( -\pi \sqrt{E_F} \left( \frac{m}{2 \hbar^2 N^2} \right)^{1/2} E_t \right) \]
Hughes, E.

Figure 2: Expected STJ curves.

The ratio of the peak to valley current (PVCR) is controlled by the gate bias. Figure 2 shows how the PVCR is changed with increasing the gate to source voltage. Note that a zero bias is expected to give an ordinary p-n diode curve.

The design of the device is centered on defining the ring gate structure. Koga et al. found that using a ring gate significantly reduces excess tunneling by eliminating corner [1]. Excess currents are undesirable because they tend to degrade the PVCR. This effect might be severe enough to completely cancel the NOR region. To avoid this possibility, the ring gate is used.

Implementing the combination of p+/n+ implants with the ring structure requires the use of two photolithography steps. After polysilicon is deposited, the outer structure of the ring must be defined. A n+ flood implant dopes the source, but the drain is masked by the poly. The next photo step is a dark field mask that defines the inner diameter of the ring. A p+ implant then creates the drain. These mask levels were designed using Mentor Graphics IC-Station component of Design Manager. The design process was the standard RITCMOS and the design rules were modified versions of the MOSIS rules.

3. FABRICATION

The device was fabricated using SIMOX silicon on insulator substrates. The prime reason for using SOI in this study was to simplify the process flow through the use of silicon mesa isolation. The use of SOI has also been found to enhance the drain impurity profile as well as reduce bulk leakage. The SOI wafers had approximately 300 nm of silicon on top of 350 nm of oxide. The use of the Nanospec and ellipsometer was not possible for measuring film thicknesses on the SOI substrates. The thickness of films was determined using dummy wafers. The process flow and procedure are shown in figure 3 and in the appendix, respectively.

4. RESULTS AND DISCUSSION

Testing of the completed STJ devices initially yielded no observable NDR characteristics or the expected diode curve for zero gate bias. These results were confirmed with more extensive testing. There were a few process issues that might have contributed to this.

The first issue is that there were difficulties with stepper overlay. Since the mask levels were designed from scratch, a stepper job needed to be created to handle the design. This includes the identifying the location of the alignment key. Though this was done, there was difficulty in adjusting for the mechanical error due to stepper. As a result, the misalignment rendered all but the largest devices inoperable.

Another issue is with the LTO deposition and etch. As a result of the inability to measure the thickness of films on the SOI wafer, the thicknesses had to be estimated from the films that were deposited on the dummy wafers. The six inch LPCVD tube using caged boats produced wafer to wafer thicknesses ranging from 3500 A to 5100A. This made it difficult to calculate and LTO deposition rate.

The wafers were etched in the GEC-Cell for 6min each, since a 20% over-etch is acceptable. It is possible that the plasma etched completely through the oxide and then through the silicon layer down to the buried oxide layer. This would account for the nano-amp noise that was experienced. Another related possibility is that the plasma did not completely clear the oxide. In both cases, the metal would be in contact with the oxide which would result in an open circuit.

5. CONCLUSION

A silicon based quantum functional device, the surface junction tunneling device, was design and fabricated. Though devices displaying negative differential resistance and ordinary p-n junction characteristics were not observed, the desired results might be achieved with further study and modifications and improvements to the existing process. Further might will include modifications and simulations of implant profiles as well as modifying the LTO etch. The use of the new advanced RIT CMOS processes might also be considered.

REFERENCES


APPENDIX

A. Experimental Procedure

1. Scribe.
2. 4pt probe.
3. RCA clean.
4. Photo-1: Mesa isolation.
5. Etch Mesa: SF$_6$+O$_2$ 42:7.5 sccm, 35sec, 400mT, 40W.
6. Ash resist: 45min
7. RCA clean.
8. GOX growth: Dry O$_2$ soak at 1000C for 25min.
9. Poly Deposition: 70min.
11. Etch Poly: SF$_6$+O$_2$ 42:7.5 sccm, 45sec, 400mT, 40W.
12. Ash resist: 45min.
13. Implant Phosphorus 100keV and 1E15 dose.
15. Etch Poly: SF$_6$+O$_2$ 42:7.5 sccm, 45sec, 400mT, 40W.
17. Ash resist: 45min.
18. RCA clean.
19. Anneal D/S.
20. LTO deposition: target 5000 A.
21. Photo-4: Contact cuts.
22. Etch Contacts: 6min SF$_6$+CH$_3$, 50mT and 270mT.
23. Ash resist: 45min.
24. Pre-Metal clean.
25. Metal Deposition.
27. Etch metal.
28. Ash resist: 45min.
29. Sinter.
30. Test.

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The author would like to thank Dr. Santosh Kurince and Dr. Turkman for their guidance. The author would also like to thank the various faculty, staff, and students who provided assistance.

Eliott Hughes, originally from Buffalo, NY, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at Motorola and Photronics.
He will be joining the Motorola Corporation as a device engineer starting July 2000.
Erbium-Doped Silicon Based LEDs

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Abstract—A preliminary effort in Electroluminescent (EL) device fabrication using erbium-doped silicon based materials at Rochester Institute of Technology’s Microelectronic Engineering Fabrication Facilities was attempted in this study. Field-assisted infiltration would be used to incorporate erbium ions into a porous silicon film. The film would be oxidized and anneal to form and erbium and oxygen rich active layer suitable for light emission. Different erbium anneals (900°C to 1100°C) would be executed and results would be thoroughly examined for any differences in the electrical or luminescent characteristics. No functional devices were fabricated, but proof of erbium activation and excitation was achieved through detection of photoluminescence (PL) in the 1100°C samples.

1. INTRODUCTION

For years, scientists have been searching for an integrated approach in producing optoelectronics on silicon chips. Such a tool would allow for further development of important applications, such as chip-to-chip interconnects and silicon based photonics. There are a number of obstacles in achieving this goal, though, since any radiation source applicable in today’s technology would have to be efficient, at a functional wavelength, able to operate in a wide range of temperatures, and still have a suitable frequency response. Since silicon is used for the vast majority of IC manufacturing, it would be an advantage if the light emitter could be fabricated using silicon process technology. Crystalline silicon by itself (c-Si) is an unsuitable source, mostly because of inefficient emission due to its indirect energy bandgap. As of late, a considerable amount of work has been done to incorporate impurities such as erbium (Er) into silicon-based films. One specific composition of interest, which is examined in this project, is Er-doped porous SiO2.

Erbium is a rare-earth metal with an atomic number of 68 and an atomic weight of 167.62. When properly inserted into a crystal structure, Er takes a 3+ ionic state. This ion can emit photons at a wavelength of 1.54 μm, a wavelength of particularly strong interest because of its ideal applications in silica based fiber optics. The 1.54 μm luminescence takes place due to a radiative internal 4f transition and is practically independent of the host crystal. There are reasons why Er-doping directly into crystalline silicon based materials will not work. Specifically, the low solid solubility of Er in Si (~10^16/cm^3 at 1300°C) prevents the incorporation of acceptable Er concentrations. Even with the use of ion implantation, Er incorporation at concentrations ~5x10^7 is prevented by the onset of Er precipitation. For practical applications higher erbium concentrations (at least 10^19/cm^3) should be engineered. One way to inhibit Er segregation is through introduction of oxygen. Er-O structures have higher solubility limits than erbium itself, and exist in a form that promotes the excitation of the Er^{3+} ion. Two methods of excitation have been identified.

![Figure 1: Methods of Er excitation in SiO structure](image)

The energy transfer shown as method A is based on electron-hole recombination. As a result of Coulomb interaction the energy released due to electron-hole recombinations is transferred to the electron-vibrating ion system. The local vibration excitation relaxes very quickly due to decay into lattice phonons, thereby exciting the Erbium ion. Method B is a schematic representation of hot-carrier impact excitation. The formation of hot carriers relies on the existence of high electric fields within an active Er-rich layer. With this knowledge, a material will be engineered with a high concentration of erbium and the ability to transport carriers. Higher fields within the...
sample will enhance impact excitation. If these goals are achieved, the sample should emit measurable amounts of electroluminescence (EL). In this case EL is radiation that is emitted when the when Er ions are excited by methods associated with electric fields and current flow. Another way to detect the erbium is through Photoluminescence (PL). PL is any radiation emitted when the when Er ions are excited by methods associated with electric fields and current flow. Another way to detect the erbium is through Photoluminescence (PL). PL is any radiation emitted when the when Er ions are excited by an external radiation source (such as an Ar laser), with no current flowing through the device. This method is not

2. EXPERIMENTAL PROCEDURES

The silicon based LEDs were fabricated on p+ silicon substrates and consist of multiple thin layers as shown in Figure 2. The structure includes a top electrode, a backside aluminum contact, an active layer, and a selectively doped n-type poly-silicon layer. Note that emission will occur in the active layer and travel through the poly-silicon. The active layer is abbreviated OPNSi, for oxide passivated nanocrystalline silicon. The OPNSi is a glass that is rich in silicon and allows for current flow.

![Figure 2: LED Device Cross Section](image)

A. Device Fabrication

Bulk-film LEDs were fabricated from the OPNSi active layer in three basic process stages; substrate preparation, active layer formation, and contact formation. Substrate preparation involved backside doping of a p-type wafer, then a 950°C steam oxidation for 3.5 hours, growing approximately 5000Å of SiO2. This oxide is removed, and followed by a backside aluminum sputter. The heavily doped backside guarantees an ohmic contact.

Active layer formation begins when the wafer is anodized in a 49% HF / ethanol (1:1 by volume) solution at a constant current density of 3.5mA/cm² for 2 min., forming a 70% porous PSI layer about 4000Å thick. Immediately after the formation of porous Silicon, erbium was introduced via field-assisted infiltration from an erbium chloride solution (ErCl₃·6H₂O dissolved in ethanol). To do this correctly, the bias used during the anodization of the porous silicon must be reversed. After infiltration, the solution was rinsed with ethanol, submerged into DI water, and quickly moved to the SRD. The backside aluminum was removed in preparation for the following oxidation and anneal. During this furnace step, a small designed experiment would be coordinated. All samples would be pushed into an O2/N2 ambient at 900°C, enough to partially oxidize the active layer. Group 1 remained at 900°C for 20min after the 02 had been shut off. Group 2 was ramped to 1100°C (in N2) and annealed for 10 min.

<table>
<thead>
<tr>
<th>Group (Wafers)</th>
<th>Anneal Temp</th>
<th>Anneal Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (A, B)</td>
<td>900°C</td>
<td>20 min.</td>
</tr>
<tr>
<td>2 (C, D)</td>
<td>1100°C</td>
<td>10 min.</td>
</tr>
</tbody>
</table>

Table 1: Experimental adjustments in Er anneal

During both thermal variations the porous silicon is transformed into the Er-doped porous glass (OPNSi). In such a film, carrier transport is facilitated through defect states, which in turn provides the necessary means for exciting the Er ions. The concentration of Er and the efficiency of the excitation would depend on the anneal times and temperatures. The active layer is then capped with 0.25um polysilicon deposited via low-pressure chemical vapor deposition at 610°C, forming an excellent interface to the active light-emitting material. The polysilicon is then selective doped n⁺ using contact lithography and a high-dose low-energy phosphorous ion-implant, followed by an activation anneal at 900°C for 15 min.

Finally, for the contact stage, the backside poly and any backside oxides are removed using an SF₆ reactive-ion etch, and a dilute 50:1 HF etch. Aluminum contacts are then formed to the n poly cathode areas via sputter deposition though a shadow mask, and backside aluminum is deposited to reproduce the backside substrate anode contact.

B. Device Testing

There were two areas of testing from which data were collected; the I-V characteristics, and the measurable luminescence. During electrical testing current was forced through the device while measuring voltage. The device was tested in both forward and reverse bias, using an HP4144 parameter analyzer. Characteristic plots will be examined to look for rectification and conductance. It is expected that the p-type regions of the substrate separated from the n-type poly under the Al contact by a semi-
The conductive layer will have characteristics similar to a diode. The techniques used during the detection of luminescence were much more involved. To detect PL, the device was excited by an Argon laser. A germanium detector was aimed at the point of excitation and a spectrum was taken by varying the value of wavelength detection over time. The area of detection was very small and initially set using a HeNe laser. During EL detection, the same germanium detector was used, but there was no external laser source exciting the LED. Instead, current would be forced through the device. Once again, the point of detection was aimed using a HeNe laser before the spectra was taken. Wavelengths under investigation would range from 1450nm to 1650nm, including the target 1540nm emission.

3. RESULTS AND DISCUSSION

When examining the IV characteristics of the LED, it is important that the devices facilitate carrier transport but are not overly conductive. The first test involved forcing a 20mA constant current and measuring the voltage (samples were allowed to reach steady state before V was recorded). These voltages ranged from 7.92V to 11.10V in Group 1 and from 8.31V to 17.22V in Group 2. The mean value of group 2 was significantly higher. Right from the beginning, we were able to tell that the wafers receiving the 1100°C anneal were more resistive. This test was also valuable in determining a device that is characteristic of the entire group, since I-V curves were not drafted for each individual device. With the same set-up as this initial testing, higher currents (100mA) were forced through the devices to get a feel for the integrity. As expected, visible light was observed at levels detectable by the human eye.

Once that single device was determined for each group, the IV tests were administered and curves were generated. Log vs. Log curves are helpful in determining the different operation regimes.

The Log vs. Log curves show that the LEDs do not have conventional diode characteristic, but still have a logarithmic response to voltage.

The linear plots (more recognizable for comparison to ideal diodes) show that the 900°C anneal samples are much more diode-like, apparent in that fact that there is a greater amount of rectification and a greater increase in current at higher voltages. For the voltages (forward bias)
at which EL testing occurs, the 1100°C anneal samples will be less conductive with higher internal fields. In both groups there are non-characteristic reverse bias curves with no sign of avalanche breakdown.

In both groups, there were no detectable levels of EL. Multiple devices from all wafers were tested at current levels ranging from 20mA to 500mA. Each time, there were visible amounts of light and significant wafer heating, but the signal from the germanium detector could not be discerned from the inherent noise. What we were expecting (PL and EL) would have appeared as follows.

Figure 6 suggests that there is more activated Er$^{3+}$ in the silicon rich silicon oxide active layer. This is accounted for because of a number of reasons. First off, there was probably a more complete anneal of the erbium within the active layer. The Er has to be bonded and in the structure for infrared emission to occur. The higher temperatures allow for more bonding to take place. Secondly, the higher oxidation and anneal temperatures allowed for a more complete oxidation of the active layer. This accounts for the lower conductivity, which would cause higher fields within the layer itself. Hot carriers would therefore have a higher probability of being generated. Since there was only a high and low setting for this designed experiment, it is impossible to tell exactly how the anneal temperature effect erbium concentrations. It is possible that higher temperature may have been too much, causing that active layer to be too resistive.

4. CONCLUSION

Even though there were no measurable levels of EL, it is reassuring to see that there were detectable levels of PL. The PL was higher in the samples annealed at 1100°C, suggesting that there were higher concentrations of Erbium and higher fields within the light-emitting active layer. It is possible that an anneal between temperatures of 900°C to 1100°C could produce even more desirable results. This experiment helped to show that erbium could be activated within the OPNSi film. Ion concentrations higher than those achieved through the field-assisted infiltration could be achieved through ion implantation. Still, large strides will have to be taken to make this film applicable in today’s opto-electronic applications.

REFERENCES


ACKNOWLEDGMENTS

The author acknowledges Dr. Karl D. Hirschman for his guidance and knowledge in this work.

Development of an Anisotropic, Selective Polycrystalline Silicon Dry Etch Process

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Abstract — The development of a polysilicon dry etch process that would result in anisotropic etch profiles as well as high selectivity to photoresist and silicon dioxide has been studied. It was found that decreasing the amount of fluorine (SF₆) in the plasma significantly increased the polysilicon etch rate while only increasing the etch rate of silicon dioxide slightly.

Two optimal processes were found: One that emphasized anisotropy (70% SF₆ flow, 90mTorr pressure, and 200W RF power) and one that emphasized SiO₂ selectivity (70% SF₆ flow, 230mTorr pressure, and 200W RF power).

1. INTRODUCTION

Highly anisotropic etching of silicon is a key process in many applications, such as deep trenches for capacitors, integrated optoelectronics, and integrated sensors. It is also extremely important in the manufacturing of very large scale integrated (VLSI) circuits, specifically in the area of polycrystalline silicon (polysilicon) gate etching. Anisotropic etch profiles are important to ensure that gate lengths are within specification, as well as to facilitate conformal film deposition in subsequent processing.

A. Background

Polysilicon etching is typically performed using a chlorine or bromine chemistry [1]. Both these gases are extremely toxic and corrosive. Their use requires special hardware to prevent corrosion of the processing equipment. Chlorine/bromine etch chemistries also have the disadvantage of etching most masking materials used. This lowers the selectivity to other layers, such as silicon dioxide (SiO₂) and photoresist.

Fluorine-based chemistries, such as SF₆, offer an alternative to chlorine/bromine. In addition to being less hazardous to the environment, the SF₆ chemistry provides higher silicon etch rates and selectivities than chlorine/bromine chemistries. The major disadvantage of SF₆ is it yields isotropic etch profiles. Cryogenic etching is a means of overcoming this isotropy, as is the addition of O₂ or C₂Cl₃F₃ [2]. As reported in [2], the addition of O₂ reduces selectivity to photoresist, and C₂Cl₃F₃ is a chlorine containing material.

The development of an anisotropic, selective polysilicon dry etch process was the focus of this experiment. Considerable research has gone into the development of anisotropic, selective dry etch processes for polysilicon using a variety of process conditions [3-5]. Because of the limitations regarding chlorine gas mentioned before, alternatives were sought. Fluorocarbon plasmas were not considered, as they result in polymer formation which can contaminate the process chamber if strict attention is not paid to cleanliness (i.e., O₂ plasma after etch to clean chamber).

B. Theory

With these considerations in mind, SF₆/O₂ was chosen for the plasma chemistry. As shown in Equation 1, the addition of O₂ to the plasma results in an increase in the F⁻ concentration, which increases Si etch rate.

\[
SF₆ + Si + O₂ \rightarrow SO₂ + SiF₄ + 2F⁻
\]  (1)

Equation 1 shows that O₂ reacts with S and prevents recombination with F⁻. Oxygen also combines with Si at the sidewalls to form SiO₂, thereby passivating the sidewalls and reducing isotropy.

Fluorine is strongly electronegative, and as a result electron attachment ionization can occur in the plasma. This results in the formation of negative ions:

\[
e^- + SF₆ \rightarrow SF₆^- \rightarrow SF₅^- + F^+
\]  (2)

Negative ions assume the role of electrons in the plasma. Because negative ions are more massive than electrons, they oscillate slower under AC excitation. This reduces the conductivity of the plasma, and results in non-uniformity in the plasma. Thus, a SF₆ chemistry can lead to non-uniform etching.

2. EXPERIMENTAL

A. Sample Preparation

All of the etching was carried out in a Drytek Quad 482 parallel plate reactor with an operating frequency of 13.56MHz. A two level factorial experiment was used.
where the power (200 – 350W), pressure (90 – 230mTorr), and SF₆ flow (70 – 100%) were varied. Table 1 lists the experimental details of the experiment.

Table 1: Experimental Design

<table>
<thead>
<tr>
<th>Run</th>
<th>SF₆ Flow (%)</th>
<th>Pressure (mTorr)</th>
<th>Power (Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>90</td>
<td>350</td>
</tr>
<tr>
<td>2</td>
<td>70</td>
<td>230</td>
<td>350</td>
</tr>
<tr>
<td>3</td>
<td>85</td>
<td>160</td>
<td>275</td>
</tr>
<tr>
<td>4</td>
<td>100</td>
<td>230</td>
<td>200</td>
</tr>
<tr>
<td>5</td>
<td>70</td>
<td>90</td>
<td>200</td>
</tr>
<tr>
<td>6</td>
<td>100</td>
<td>90</td>
<td>350</td>
</tr>
<tr>
<td>7</td>
<td>85</td>
<td>160</td>
<td>275</td>
</tr>
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<td>8</td>
<td>70</td>
<td>90</td>
<td>350</td>
</tr>
<tr>
<td>9</td>
<td>85</td>
<td>160</td>
<td>275</td>
</tr>
<tr>
<td>10</td>
<td>70</td>
<td>90</td>
<td>200</td>
</tr>
<tr>
<td>11</td>
<td>100</td>
<td>230</td>
<td>350</td>
</tr>
</tbody>
</table>

Three center point runs (275W, 160mTorr, 85% SF₆ flow) were included to evaluate experimental error.

The starting material was 100mm n-type silicon wafers (100). A 1000Å wet oxide was grown in a 6" horizontal furnace at 900°C for 42 minutes. A 0.6μm polysilicon layer was then deposited in a LPCVD furnace at 610°C for 78 minutes.

In order to simulate the CMOS process used at Rochester Institute of Technology (RIT), the polysilicon was then doped using N250 arsenosilicate spin-on glass. The SOG was spun on at 3500RPM for 30 seconds, followed by a 15 minute pre-bake at 200°C. An arsenic drive-in step followed this at 1000°C for 15 minutes.

The wafers were next coated with 0.98μm of Shipley S-8 photoresist and exposed using a g-line stepper. The reticle used was the RIT CMP test mask, which had various features including dense lines/spaces of varying coverage. The minimum resolvable linewidth in photoresist was 1μm.

Windows were opened through the resist across the wafer to make direct measurements of the polysilicon thickness.

Initial step height measurements were made using a Tencor Alpha-step profiler. These would be later used to determine polysilicon etch rates and selectivities to SiO₂ and photoresist. Scanning electron microscopy was used to evaluate anisotropy of the individual process runs.

**B. Etching Process**

The SF₆ flow was held constant at 40sccm while the O₂ flow rate was varied from 0 – 17sccm. This allowed variation in SF₆ flow from 70-100%. Each wafer was etched for 20 seconds. Polysilicon thickness measurements were then made using a Nanometrics Nanospec AFT thin film thickness measuring tool. Polysilicon etch rate was calculated from these pre- and post-etch values. Each wafer was then etched, in 15 second increments, until all the polysilicon cleared, exposing the oxide. A 15 second over etch was then performed to determine the selectivity to oxide.

**3. RESULTS AND DISCUSSION**

The most noticeable result after removing each wafer from the etch tool was the etch non-uniformity across the surface of the wafer. The edges of the wafers etched significantly faster than at the center. This is shown in Figure 1.

**Figure 1: Etch non-uniformity across wafer**

Shown in Figure 2 is a plot of the polysilicon etch rate, both edge and center, and the selectivity to SiO₂. It should be noted that photoresist loss for each experimental run was minimal, and those values are not reported in the results presented.

**Figure 2 confirms the etch rate non-uniformity observed in Figure 1.** The etch rate at the edges of the wafers was almost twice what it was at the center of the wafers. As mentioned earlier in this paper SF₆ plasmas can be non-uniform due to the formation of negative ions in the plasma. Another possible explanation for this non-uniformity is in the etch tool itself – it is a tool designed for 150mm wafers, and the wafers used in this experiment were 100mm.

From Figure 2 some general trends can be established. With a SF₆ flow of 70% and a pressure of 90mTorr, increasing the power from 200W to 350W caused an increase in edge etch rate of 20%, while the center etch rate decreased by 9%, and the SiO₂ selectivity decreased by 40%. With 70% SF₆ flow and 230mTorr pressure, a power increase from 200W to 350W caused edge etch rate to increase by 133%, center etch rate to increase by 148%, and selectivity to decrease by 34%.

In order to evaluate the anisotropy of each of the etch processes a Philips scanning electron microscope (SEM) was used to view cross sections of the samples. Each
sample was cleaved through the desired features, and then sputter coated with gold at a pressure of 100mTorr for 60 seconds. SEM micrographs are given in Figures 3 – 6.

Not every etch process underwent cross sectioning; only those that yielded relatively high polysilicon etch rates and high SiO₂ selectivities.

Figure 3: 100% SF₆, 230mTorr, 200W

Figure 4: 70% SF₆, 90mTorr, 350W

Figure 5: 85% SF₆, 1600mTorr, 275W

Figure 6: 70% SF₆, 90mTorr, 200W

Although difficult to tell from the above SEM micrographs, there was significant undercutting of the process shown in Figure 3. There was a significant CD bias due to this undercutting. The same was observed for the process in Figure 4. For the process in Figure 5, no undercutting was observed. However, resist loss at the
edge of the line was significant, resulting in linewidth narrowing.

The process shown in Figure 6 (70% SF₆, 90mTorr pressure, 200W RF power) gave very anisotropic etching. The measured linewidth was 4.5μm for a 5μm line. Resist loss was minimal over the polysilicon line.

4. CONCLUSION

An investigation of polysilicon plasma etching was performed. The goal was to develop a process the had both a high polysilicon etch rate and high selectivity to SiO₂ and photoresist, while at the same time providing anisotropic etch profiles. A single process that met these requirements was not found; instead, two different processes were found.

The process that provided maximum anisotropy (see Fig. 6) used a SF₆ flow of 70%, pressure of 90mTorr, and RF power of 200W. The major drawback of this process was the disparity between center and edge etch rates. A 42 second etch, which would completely clear the polysilicon in the center of the wafer, would result in a 12 second over etch at the edges. This translates to a SiO₂ loss of 125Å.

The process that provided maximum selectivity (see Fig. 2) was run #5 (70% SF₆ flow, 230mTorr, 200W). This resulted in a 108Å SiO₂ loss at the edge of the wafer.

Future work for this experiment includes further study of process parameters around the optimal ones determined in this experiment. Further cross sectioning is needed to understand the anisotropy of the etch processes. Exploration of the etch non-uniformity is critical to developing an anisotropic, selective polysilicon dry etch process.

ACKNOWLEDGMENTS

The author would like to thank Dr. Santosh Kurinec for her assistance with this experiment. The author also thanks the RIT equipment technicians for maintaining the equipment during the course of this experiment.

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Cobalt Silicide Formation and Patterning Technology

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Abstract—The goal of this investigation was to develop a cobalt silicide formation process as a stepping stone to investigate a novel patterning technique known as LOCOSI (LOCal Oxidation of Silicide). Cobalt silicide films were formed by sputter depositing cobalt onto silicon wafers then annealed at temperatures varying from 750 - 1000°C using two methods. The first method was a conventional anneal using a horizontal furnace using a forming gas ambient. The second method was a RTA (Rapid Thermal Anneal) using a nitrogen ambient. The RTA process for silicidation provided essentially a continuous film with minimal cracking, whereas the furnace anneals resulted in non-continuous cobalt silicide films. The patterning of the films, which requires a patterned oxidation mask similar to the LOCOS (LOCal Oxidation of Silicon) process, was unsuccessful.

1. INTRODUCTION

Cobalt silicide has been used in industry to form self-aligned low resistance source/drain and gate contacts. New applications of cobalt silicide include fabrication of ultra-short Schottky-Tunneling MOSFETs and MSM (metal-semiconductor-metal) photodetectors. Fabrication of these devices requires nanometer scale patterning of cobalt silicide film. Unfortunately, conventional patterning techniques require high-end lithography equipment for the small dimensions and a dry etch process. Using a novel patterning technique, known as LOCOSI (LOCal Oxidation of Silicide), cobalt silicide films can be patterned using low-end lithography equipment.

As cobalt was new to RIT the deposition and silicidation processes needed to be developed before any patterning could take place. This development work sets the groundwork for future optimization and for studies of other cobalt/cobalt silicide applications.

2. THEORY

A. Cobalt

Cobalt is a group VIII, near noble metal with the following material properties.

Table 1: Selected Properties of Cobalt

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atomic Number</td>
<td>27</td>
</tr>
<tr>
<td>Atomic Mass</td>
<td>54.938</td>
</tr>
<tr>
<td>Reflectivity</td>
<td>67%</td>
</tr>
<tr>
<td>Melting Point</td>
<td>1495°C</td>
</tr>
<tr>
<td>Resistivity</td>
<td>6 μΩ cm</td>
</tr>
</tbody>
</table>

B. Cobalt Silicide

Cobalt reacts with silicon to form cobalt silicide, which has a resistivity ranging from 18-20 μΩ cm. While many combinations are possible, the stoichiometry of interest is cobalt disilicide, CoSi2 because silicon-rich silicides are more stable than metal-rich silicides. Figure 1 below shows how the heats of formation rises as the silicon content increases but levels off after silicide becomes silicon-rich. [1]

Figure 1: Heat of formation per metal atom of silicides as a function of metal to silicon ratio [1]
The phase of the silicide is temperature dependent. According to literature, at temperatures from 300-600°C mostly CoSi and CoSi2 with some CoSi2 are formed. At temperatures above 600°C only is formed CoSi2. Also at temperatures ranging from 200-600°C, cobalt is the dominant diffuser. At higher temperatures silicon gradually becomes the dominant diffuser. These concepts are important when siliciding by annealing cobalt films on silicon substrates. [1]

Cobalt silicide is a tensile film, which can result in film cracking. The magnitude of stress varies with the phase of the silicide, substrate doping, and temperature. As the CoSi2 phase about to form silicon diffuses through the grain boundaries of the silicide and metal films resulting in compressive stress. Once the phase forms a volume contraction takes place resulting in tensile stress in the film. Once the film has cooled the end result is a tensile film. The silicon doping concentration works to slow the silicidation process thus shifting the temperatures at which the different phases form. [2]

The thermal stability of the cobalt silicide varies with the dopant species in the substrate and whether the substrate is poly or monocrystalline silicon. Silicides on polysilicon substrates typically are more sensitive to thermal processing, however this phenomenon still occurs with silicide on monocrystalline silicon. The degradation of the silicide at temperatures over 800°C occurs because of silicon precipitation in the silicide film. As discussed earlier, at higher temperatures silicon becomes a dominant diffuser. The result is a breakup in the continuity of the silicide film. [3]

C. LOCOSI (Local Oxidation of Silicide)

The LOCOSI process is similar to the well-known LOCOS process used to selectively grow the isolation oxide in CMOS technology. However, the purpose and functionality of these two processes is different. Both processes use a Si3N4/SiO2 oxidation mask to selectively grow an oxide. The purpose of LOCOSI is to pattern the silicide layer under the oxidation mask.

Below is a breakdown of the mechanism, which leads to separation in the film (Figure 2).

1) Oxidizing ambient diffuses through oxide and dissociates the silicide.
2) The free silicon reacts with the oxidant to form silicon dioxide.
3) The free cobalt diffuses through the silicide to the silicide/substrate interface where it reacts with silicon to form silicide.
4) Near the edge of the oxidizing mask the stress of the nitride forces the diffusing cobalt to drift away from that edge. This causes a gap to form at the mask edge.

In the LOCOSI process the stress of the nitride film is desired unlike in the LOCOS process.

Figure 2: Cross-sections showing the functionality of the LOCOSI process.

Figure 3 below illustrates why the oxidation process forms SiO2 on the surface rather than a cobalt oxide. [4]

Figure 3: Heats of formation per oxygen atom of various oxides. Also shown is the heats of formation for SiO2. Cobalt oxides behave like the group VIA elements. [1]

According to literature cobalt oxides behave like the oxides of VIA element oxides. As can be seen in figure 3 it is more favorable for SiO2 to form than a cobalt oxide. Once the cobalt is dissociated it diffuses through the silicide since it is not favorable for the cobalt to form a metal rich silicide. (Figure 1)

LOCOSI experiments found in literature used epitaxial CoSi2 deposited by MBE (Molecular Beam Epitaxy). The oxidation mask is then aligned parallel to <110> directions of the silicide to obtain a clean separation. However, it is
mentioned process works for polycrystalline cobalt silicide. [4, 5]

3. EXPERIMENTAL

A. Furnace Anneal

The initial step before cobalt can be deposited on the wafers was a preclean. This was done by immersing the wafers for 10 min in a H$_2$SO$_4$/H$_2$O$_2$ solution for 10 min. This was followed by a 5 min rinse and a 10 sec HF dip to remove any native/chemical oxide.

The wafers were then pulsed DC sputtered using a CVC 601 sputterer at the following setpoints.

Table 2: Sputtering setpoints for Co deposition

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setpoint</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>500 W (4” Co target)</td>
</tr>
<tr>
<td>Base Pressure</td>
<td>~2E-5 Torr</td>
</tr>
<tr>
<td>Argon Pressure</td>
<td>5 mTorr</td>
</tr>
<tr>
<td>Pre Sputter Time</td>
<td>5 min</td>
</tr>
<tr>
<td>Sputter Time</td>
<td>5 min</td>
</tr>
</tbody>
</table>

The deposited film was about 800 to 1000Å thick. Readings were performed on an Alphastep, which was uncalibrated after being serviced so readings may not be accurate.

The average resistivity of the Co film on Si was 88 $\mu$Ω cm, which is about 15 times greater than the literature quoted value of 6 $\mu$Ω cm. This could be due to oxygen incorporation into the film during sputtering.

This first batch of wafers were then annealed in a Bruce 6” horizontal furnace at 800°C, 900°C and 1000°C. The basic recipe for the anneal is listed below in Table 3.

Table 3: Basic Furnace Anneal Recipe

<table>
<thead>
<tr>
<th>Step</th>
<th>Time</th>
<th>Gas</th>
</tr>
</thead>
<tbody>
<tr>
<td>Push in 800°C</td>
<td>12 min</td>
<td>N$_2$</td>
</tr>
<tr>
<td>Stabilize at 800°C</td>
<td>15 min</td>
<td>N$_2$</td>
</tr>
<tr>
<td>Ramp up to Soak Temp</td>
<td>20–30 min</td>
<td>N$_2$</td>
</tr>
<tr>
<td>Soak at Soak Temp</td>
<td>30 min</td>
<td>H$_2$/N$_2$</td>
</tr>
<tr>
<td>Ramp down to 800°C</td>
<td>30–40 min</td>
<td>N$_2$</td>
</tr>
<tr>
<td>Pull at 800°C</td>
<td>15 min</td>
<td>N$_2$</td>
</tr>
</tbody>
</table>

After the wafers were annealed they were placed in a selective etch to remove unreacted cobalt if any. This was done in a 35 sec dip in H$_2$SO$_4$/H$_2$O$_2$ at 125°C. The wafers were all hazy and gray before the etch with divots missing in the films. Afterwards it appeared as if the material at the edges of the wafer etched away and the gray streaks remained on the wafer along with the divots (figure 4). Attempts at resistivity measurements gave odd results with varying amounts of current with no voltage reading or reading that resembled the bare silicon measurements.

Figure 4: Divot in film after silicidation in furnace.

After inspection of the films under an optical microscope it was discovered that the films were not continuous (Figures 5-7).

Figure 5: Silicidation in furnace at 800°C

Figure 6: Silicidation in furnace at 900°C
Although the silicide films were not continuous the wafers were still oxidized to see the effect. The oxidation was performed in a Bruce 6" horizontal furnace using the following recipe.

**Table 4: Recipe for thermal oxidation of cobalt silicide.**

<table>
<thead>
<tr>
<th>Step</th>
<th>Time</th>
<th>Gas</th>
</tr>
</thead>
<tbody>
<tr>
<td>Push in 800°C</td>
<td>12 min</td>
<td>N$_2$</td>
</tr>
<tr>
<td>Stabilize at 800°C</td>
<td>15 min</td>
<td>N$_2$</td>
</tr>
<tr>
<td>Ramp up to 900°C</td>
<td>20–30 min</td>
<td>N$_2$</td>
</tr>
<tr>
<td>Soak at 900°C</td>
<td>10 min</td>
<td>H$_2$O</td>
</tr>
<tr>
<td>Ramp down to 800°C</td>
<td>30–40 min</td>
<td>N$_2$</td>
</tr>
<tr>
<td>Pull at 800°C</td>
<td>15 min</td>
<td>N$_2$</td>
</tr>
</tbody>
</table>

Figure 8 shows the result after oxidizing a wafer annealed at 800°C. The oxidation process made the non-continuous film worse.

**B. RTP Anneal**

Since the furnace anneals gave a poor film a rapid thermal anneal process was developed. Once again the initial step before cobalt was deposited was a preclean. The clean procedure was changed in case the cause for the divots in the films produced in the furnace was due to poor adhesion. During this trial a full RCA clean was performed followed by a 10 sec HF dip to remove any native/chemical oxide.

The wafers were then pulsed DC sputtered using a CVC 601 sputterer at the following setpoints. The only difference was the lower base pressure.

**Table 5: Sputtering setpoints for Co deposition**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setpoint</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>500 W (4&quot; Co target)</td>
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<td>Base Pressure</td>
<td>~8.6 E-6 Torr</td>
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<td>Argon Pressure</td>
<td>5 mTorr</td>
</tr>
<tr>
<td>Pre Sputter Time</td>
<td>5 min</td>
</tr>
<tr>
<td>Sputter Time</td>
<td>5 min</td>
</tr>
</tbody>
</table>

Once a gain the deposited film was about 800 to 1000Å thick. The average resistivity of the Co film on Si was, 48 μΩ cm. This is an improvement over the wafer which were used for the furnace anneal runs which gave 88 μΩ cm. The wafer for this run were heavily doped p-type (20 Ω cm) whereas the wafer used during the previous runs were moderately doped p-type (40–60 μΩ cm). Also the lower base pressure results in less oxygen incorporation into the cobalt film.

This batch of wafers were annealed in a AG Associates HeatPulse 410 RTP at 750°C, 800°C and 900°C in a nitrogen ambient. When performing anneals in the HeatPulse 410 there is no recipe to run, the time and temp are set and then started. However, a 30 sec delay was used after the wafer was in the chamber before starting the anneal to allow the chamber to fill up with nitrogen. Afterwards the wafer was allowed to cool in the chamber for about a minute before removing it. This is to avoid any potential reactions with the clean room ambient while the wafer is still hot. Figures 9-11 below show the cobalt silicide films formed by RTA.
Notice that the films produced by RTA are continuous with minimal cracking. The wafers annealed at 750°C showed less cracking and flaking of unreacted cobalt. At the higher temperature anneals, 800°C and 900°C, the films showed large areas of flaking cobalt. The majority of the film on the 900°C sample showed film degradation. When the wafers were selectively etched for 35 sec in H$_2$SO$_4$/H$_2$O$_2$ at 125°C, the degraded film regions and the areas with flaking cobalt were removed. Figures 12-13 below show this film defects.

Table 6 below shows the resistivity results of the RTA silicides on silicon. The measurements were taken in areas where there was no film degradation.

<table>
<thead>
<tr>
<th>Anneal Temp</th>
<th>Resistivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>750°C</td>
<td>326 $\mu$Ω cm</td>
</tr>
<tr>
<td>800°C</td>
<td>No reading film was damaged</td>
</tr>
<tr>
<td>900°C</td>
<td>16 $\mu$Ω cm</td>
</tr>
</tbody>
</table>

C. Patterning

Due to time restrictions a new 800°C sample was not created to replace the one that was damaged. The first step of the patterning process was to build the oxidation mask. The oxide layer was deposited using an LTO process in a 4" LPCVD tube. The process parameters are below.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>400°C</td>
</tr>
<tr>
<td>Base Pressure</td>
<td>60 mTorr</td>
</tr>
<tr>
<td>Gasses</td>
<td>40 sccm of Silane</td>
</tr>
<tr>
<td></td>
<td>48 sccm of Oxygen</td>
</tr>
<tr>
<td>Dep Time</td>
<td>15 min</td>
</tr>
</tbody>
</table>

The target thickness was 500Å, but the actual thickness was 711Å. Figures 14-15 show the LTO film over the cobalt silicide. The cobalt silicide films look intact which is expected because of the low temperature of the LTO process.
After the LTO deposition the nitride film was deposited in the same CVD tube as the LTO at the following setpoints.

Table 8: Process setpoints for silicon nitride deposition

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>810°C</td>
</tr>
<tr>
<td>Base Pressure</td>
<td>60 mTorr</td>
</tr>
<tr>
<td>Gas</td>
<td>Dichlorosilane</td>
</tr>
<tr>
<td>Dep Time</td>
<td>17 min</td>
</tr>
</tbody>
</table>

The target thickness was 1500Å but the actual thickness was 1349Å. The result is a nitride/oxide thickness ratio of 1.89.

The oxidation mask must be patterned before the actual thermal oxidation takes place. The wafers were coated and exposed using a G-line stepper and capacitor mask, which has large capacitor pads. Afterwards the nitride was etched off using a Drytek Quad. Table 9 gives the process parameters of the nitride etch.

Table 9: Nitride etch process parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure</td>
<td>300 mTorr</td>
</tr>
<tr>
<td>Forward Power</td>
<td>265 W</td>
</tr>
<tr>
<td>Gas</td>
<td>30 sccm of SF6</td>
</tr>
<tr>
<td>Etch Time</td>
<td>65 sec</td>
</tr>
</tbody>
</table>

This etch process consumes all of the nitride and some of the oxide underneath. Figures 16—7 show the films after the etch process.

Once the nitride is removed the wafers can be thermally oxidized to pattern the cobalt silicide film. The oxidation recipe parameters are the same as described in Table 4. Figures 18—19 show the results after oxidation.
The RTP anneals showed similar issues with film degradation at higher temperatures as the furnace anneals. The other issue with the RTP anneal was the high resistivity (326 μΩ cm) of the 750°C annealed wafer. This along with the reaction seen with the LTO and Nitride films (Figure 18) during patterning indicate that the silicide film did not contain large amounts of cobalt disilicide, which should be more stable and have much lower resistivity like that of the 900°C annealed sample (16 μΩ cm). Although literature states that cobalt disilicide is formed at temperatures above 600°C, this could be explained by the high dopant concentration in the wafer which slow down the process thus requiring higher temperatures to change phase. However this would need to be investigated further.

XRD data for the samples silicided at 750°C and 800°C showed no peaks. Perhaps this means that the films were still amorphous. Figure 20 is a sample from literature showing peaks.

4. DISCUSSION

The poor results given by the furnace silicidation can be attributed to several reasons. First is the pre clean before the Co deposition, which was not a complete RCA clean as done with the wafers used processed in the RTP. If the wafers were not clean enough the poor adhesion would explain the divots in the silicide film.

Another reason is the furnace recipe itself. The recipe dictates that the wafers are push and pulled at 800°C. Although nitrogen is flowing during this the wafers are exposed to the clean room ambient while they are hot. This can cause oxygen incorporation into the film. Also at the high temperatures the silicon tends to diffuse through the metal and precipitate causing the break up of the film.

A slower furnace recipe may be beneficial in controlling the reaction. The wafers could be pushed in at lower temperatures (500°C) then ramped to the desired anneal temperature.

5. CONCLUSIONS

Of the two silicidation techniques, RTA produced essentially continuous films with minimal cracking. The furnace anneals produced non-continuous films. The flaws in the furnace anneals include the push in at a high temperature of 800°C. This coupled with the long stabilization time may have caused the film degradation. The furnace anneal recipes should be rewritten to start off
at a lower temperature and ramp up once the wafers are in the tube.

Although the RTA films were practically continuous, the HeatPulse 410 does have some thermal non-uniformity which prevent the formation of a uniform cobalt silicide film across the wafer. Another issue is the cracking in the films silicided at temperatures above 750°C. The furnace anneals heating the wafer up to such high temperatures quickly causes stress and film degradation issues. It would be beneficial to process the wafers in a 2-step anneal starting with a lower temperature around 500°C and then moving to higher temperatures.

The silicide films produced at 900°C in the RTP proved to be the most stable film and exhibited the lowest resistivity of 16μΩ cm, which corresponds to literature values for cobalt disilicide films.

The patterning process was not successful. The cobalt silicide films under the oxidation mask broke up into islands after nitride deposition. The wafers, which were silicided at 750°C showed reaction the oxidation mask after the final oxidation step in the LOCOSI process. This however was not observed with the wafer, which was silicided at 900°C.

Some future work that could be done include investigating what effect the pre-deposition clean has on the silicidation and resistivity of cobalt silicide and testing out a piecewise anneal process on both the RTP and furnace to see if a the silicide quality is improved (i.e. thermal stability and continuity). Once a thermally stable and continuous film is achieved then the oxidation mask thickness ratios for the LOCOSI need to be optimized to see observe their effect on the patterning process. Also a rapid thermal oxidation should be investigated for the patterning process.

REFERENCES


ACKNOWLEDGMENTS

The author acknowledges Dr. Santosh Kurinec and Dr. Renan Turkman for guidance in this work and Rich Battaglia, Bruce Tolleson and Dave Yackoff for equipment support.

Neil S. Patel, originally from Dayton, NJ, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at National Semiconductor and Motorola MOS 11. He will be joining National Semiconductor as a photolithography process engineer starting June 2000.
Reactive Sputtering of Tantalum Nitrides for Diffusion Barrier Layers

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Abstract – The objective of this project is to develop a robust process to deposit Tantalum nitride barrier layer for copper metallization. TaN films were reactively sputtered in a twin cathode AC inverted cylindrical magnetron configuration using the IonTech Cyclone sputtering system. The dependence of thickness, resistivity and phase changes as a function of N₂ flow rate was studied. A designed experimental approach was used to optimize resistivity and the phases formed. A 10 sccm N₂ flow (with 99 sccm Ar) deposited at 4 mTorr and 2 kW pressure gave an amorphous bcc-phase Ta(N) with a low resistivity of about 220 μΩcm. Further analysis would be done to study the barrier properties, after depositing copper and doing electrical, structural and chemical characterization.

1. INTRODUCTION

A. Copper Metallization

As device dimensions are being scaled down to deep submicron, the metallization technology is becoming increasingly important. Copper is a promising interconnect material because of its low electrical resistivity and high resistance to electromigration as compared to the commonly used aluminum and its alloys. However, Cu is a fast diffuser in Si and SiO₂. The presence of Cu-Si precipitates in critical regions strongly affects the reverse leakage current of p-n junctions. It degrades the device performance by introducing deep electronic levels into the Si bandgap leading to reduction in the carrier life. Also, there are no suitable CVD processes for Cu deposition. It oxidizes easily because of the ability to have self-passivation. It does not undergo anisotropioic etching, and cannot be etched by the normal RIE techniques. Cu also has poor adhesion to the dielectric layers.

B. Need for barrier layer

To eliminate the diffusion into the substrate, a layer diffusion barrier material which has less grain boundaries, good adhesion to Si and SiO₂, high thermal and electrical stability with respect to Cu is necessary. Various transition and refractory metals and their alloys, nitrides, silicides and oxides have been studied as potential barriers, and Tantalum Nitride compounds have been found to be promising candidates. A good diffusion barrier should have minimum interaction with copper so that it does not affect the resistance of the copper interconnect. TaN has a very high melting point (3087°C). It is thermodynamically stable with respect to Cu and has good adhesion to Si and SiO₂. TaN has a dense microstructure, shows good resistance to heavy mobility of Cu in Si and has electrical stability at high temps (upto 750°C).[1]

The objective of this project is to investigate the barrier properties of Ta and its nitrides for Cu metallization at RIT.

2. EXPERIMENTAL AND RESULTS

A. Experimental

The substrates were prepared from Si wafers on which 1000Å of oxide was grown in the Bruce furnace. They were patterned into horizontal stripes of alternate layers of Si and SiO₂ using a Kasper aligner. This would enable us to study the properties of TaN on both Si and SiO₂, and also use the four-point probes to measure sheet resistance on the TaN deposited on the SiO₂ regions, by providing an insulating substrate.

The TaN films were reactively sputtered in an AC twin cathode inverted magnetron configuration of the Ion Tech Cyclone sputtering system. The Ion Tech Cyclone is a fully automated system with short cycle times and high deposition rates. The AC inverted magnetron configuration has remarkable improvements over the RF and DC configurations. There is excellent target utilization and uniform deposition of even complex shapes.

A 7.5" Ta target was used, and the base pressure of the chamber was 5 x 10⁻⁶ Torr, and the working pressure was about 5.2 x10⁻³ Torr. A hysteresis plot was first obtained for nitrogen flow in the range of 0 to 50 sccm by increasing and decreasing the N₂ flow respectively and measuring the voltage of the target without using any substrate. The deposition was done at 2 kW forward power and a total pressure of 8 mTorr for 5 min. The gas mixture consisted of Ar at 99sccm. In the operating range, no hysteresis was observed as seen in figure 1. This is because of the high pumping speed of 1600 l/s obtained by a turbopump. There is no poisoning of the target, and the films were deposited in the high rate metal sputtering
regime. The films were then deposited under the same conditions, while the N\textsubscript{2} flow rate was varied from 0 to 40 sccm.

**Figure 1: Hysteresis behavior of TaN**

The thickness of the films was measured using a Tencor AlphaStep profilometer. Steps were made by marking a line on the wafers prior to deposition with a sharpie pen, and then rubbing it off after the deposition using acetone. Sheet resistance was measured by a four-point probe. The x-ray diffraction Analysis was done on Rigaku x-ray diffractometer with Cu K\textalpha\ radiation. The adhesion of the films to the substrate was tested using a tape test.

**Figure 2: Dependence of thickness on N\textsubscript{2} flow**

**B. Results and Discussion**

The resistivity of the pure Ta film is about 720 \(\mu\Omega\) cm. As the nitrogen in the film is increased to 5% there is a decrease in resistivity to 430 \(\mu\Omega\) cm. Increasing the N\textsubscript{2} content further to 20%, causes a gradual increase to 1200 \(\mu\Omega\) cm. The deposition rate was high at low levels of nitrogen, but there was a sharp decrease in deposition rate with nitrogen. At higher levels of N\textsubscript{2} there is a steep increase in resistivity due to low deposition rate and high sheet resistance. This is seen in figures 2 and 3.

**Figure 3: Dependence of resistivity on N\textsubscript{2} flow**

This change in resistivity is explained due to the change in the crystalline structure of the Ta\textsubscript{N\textsubscript{x}} phase, which was analyzed from the XRD patterns, and compared with those observed in the literature. The pure Ta shows the (002), (202), (413) peaks of tetragonal Ta. With slight increase in N\textsubscript{2}, bcc-Ta phase starts forming, observed by the (110) and (200) peaks [3], seen in figure 4, which explains the drop in resistivity.

**Figure 4: XRD Pattern with 5 % N\textsubscript{2}**

At higher N\textsubscript{2} levels of 10 –15 %, the bcc Ta(N) and at 20%Ta\textsubscript{3}N phases are formed as seen in figure 5. The Ta\textsubscript{3}N phase is supposed to have a good amorphous
microstructure. At 40 sccm N₂, the peaks are not sharp. Table 1 shows the various phases at different levels of N₂.

Further analysis needs to be done to analyze the phases, which have been reported as fcc TaN. When the films were tested with a scotch tape, they did not peel off. This means the adhesion of the films to the substrate was good

<table>
<thead>
<tr>
<th>N₂ flow (sccm)</th>
<th>Crystalline Phases</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Tetragonal Ta</td>
</tr>
<tr>
<td>5</td>
<td>TetragonalTa +bccTa(N)</td>
</tr>
<tr>
<td>10</td>
<td>bcc Ta(N)</td>
</tr>
<tr>
<td>15</td>
<td>bccTa(N) amorphous</td>
</tr>
<tr>
<td>20</td>
<td>bcc TaN</td>
</tr>
<tr>
<td>30</td>
<td>fcc TaN</td>
</tr>
<tr>
<td>40</td>
<td>Fcc TaN + Ta₃N₅</td>
</tr>
</tbody>
</table>

Table 1: Phases of TaN [3]

This interesting change in the nature of resistivity of the films was in agreement to the literature [2], but the overall resistivity was an order higher than the reported values. So a Design of Experiments methodology was used for optimization of process parameters for making the films. The following five factors were chosen to be investigated and a ½ fractional factorial experiment was run.

- N₂ flow rate: 5 and 20 sccm
- Pressure: 4 and 8 mTorr
- Power: 1 and 2 kW
- Substrate bias: 0 and 50 kV
- Time: 5 and 15 min

The responses measured were thickness, sheet resistance, and resistivity. The results were analyzed using the minitab software, and after doing the Yates anova analysis, the optimum parameters obtained to get low resistivity of 220 μΩcm and good structure were 10sccm N₂, gas pressure of 4mTorr, zero bias, power of 2kW for time 15 min.

3. CONCLUSIONS

The optimum conditions for the barrier layer would be a low pressure, high power, no bias, a slightly high time deposition. Also N₂ flow of about 10 sccm N₂ gives an amorphous phase which would be a good diffusion barrier. The next phase of study includes deposition of Cu seed layer followed by electroplating of Cu on the TaN films and testing the barrier properties by doing RBS analysis. Also, other barrier materials like TaSiN, which have better barrier properties would be studied.

ACKNOWLEDGEMENTS

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REFERENCES

Deconfounding the Effects of Cu and Cr on Perceived Fe Contamination in Si Using an SPV Technique

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Abstract—The effects of iron, copper, and chrome on minority carrier diffusion length measurements in p-type, boron doped, silicon were investigated using a surface photovoltage (SPV) technique. Attempts were made to reproduce previous results for iron and chrome, metals which form complexes with boron. Also an attempt was made to study the effect that copper contamination would have upon the SPV results. It was found that the iron results were reproducible, FeB could be photodisassociated, and that the chrome contaminated wafers were not affected by the photodisassociation, CrB pairs were not broken. The copper contaminated wafers were found to be affected by the photodisassociation step, which significantly reduced the measured diffusion lengths.

1. INTRODUCTION

The need for smaller and/or more efficient semiconductor devices has led to an increased effort to reduce, or in some cases even eliminate, impurities in silicon substrates. Perhaps the most important sect of these impurities are the fast diffusing metallics that have energy trap levels in silicon near midgap. These metallics effectively reduce carrier lifetimes and may also adversely affect the integrity of gate oxides. These facts create a need for an analytical technique that is very sensitive, requires little sample preparation, and has a quick turn around time. A technique was developed using surface photovoltage (SPV) minority carrier diffusion lengths in order to measure iron, perhaps the most common of these impurities. This technique is based upon the fact that in p-type, boron doped, silicon; iron complexes with boron. When the substrate is illuminated, or heated and quick quenched, these pairs are disassociated. This is often termed the activation step. The unpaired iron is a more efficient trap and the minority carrier lifetime is therefore reduced. Due to the measurable differences in diffusion lengths before and after activation, an iron concentration can be determined.

Other metals are known to have trapping properties that may also be effected during the activation step. The most completely studied of these metals is chrome. Chrome also complexes with boron, and when disassociated becomes a less efficient trap. The clouding of perceived iron levels due to chrome can be minimized by using the photodissociation method instead of the heating and quick quenching method. This is due to the fact that the CrB pairs do not photodisassociate as readily as the FeB pairs. Copper is another metallic contaminant that may effect SPV results. After a high temperature process (above 900°C) and a slow cool, copper tends to precipitate at the silicon surface. At the silicon-silicon dioxide interface, the copper does not influence the diffusion length measurements. After the photoactivation step, however, the copper reduces the diffusion length.

2. EXPERIMENTAL

P-type, boron doped, 150 mm, <100> silicon wafers that had a resistivity between 8 and 12 Ohm-cm; were oxidized in wet ambient at 950°C to grow a target oxide thickness of 500 angstroms. The diffusion lengths of the wafers were then measured to assure that the oxidation process did not lead to high initial metallic impurity levels, which would contribute to noise in the experiment. These wafers were then implanted with iron, copper and chrome at various doses and combinations of elements. The energies of the implants were adjusted so that the peak metal concentration was located at the silicon-silicon dioxide interface. The wafers were then annealed at 950°C for 45 minutes in nitrogen. Twenty-four hours after the anneal, the diffusion lengths were then measured using the SPV technique. A photodisassociation step was performed next and the diffusion length was remeasured. After waiting 24 hours for the FeB pairs to reform, the measurement, activation, and remeasurement process was repeated.
3. RESULTS AND DISCUSSION

The initial minority carrier diffusion lengths, after oxidation and prior to implantation, are given in Table I. The legend names in this document, M*D*, stand for the order in which the iron measurements were taken (M) and the diffusion length before and after activation (D1 and D2). Measurement one (M1D1 and M1D2) were prior to implantation, all others are after implantation and anneal.

Table I: Initial screening for [Fe], post oxidation.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>M1D1 (um)</th>
<th>M1D2 (um)</th>
<th>Initial [Fe] (cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPV-132 01</td>
<td>419</td>
<td>319</td>
<td>4.34E+10</td>
</tr>
<tr>
<td>SPV-132 02</td>
<td>426</td>
<td>360</td>
<td>2.32E+10</td>
</tr>
<tr>
<td>SPV-132 03</td>
<td>430</td>
<td>365</td>
<td>2.20E+10</td>
</tr>
<tr>
<td>SPV-132 04</td>
<td>429</td>
<td>363</td>
<td>2.26E+10</td>
</tr>
<tr>
<td>SPV-132 05</td>
<td>428</td>
<td>362</td>
<td>2.28E+10</td>
</tr>
<tr>
<td>SPV-132 06</td>
<td>430</td>
<td>366</td>
<td>2.16E+10</td>
</tr>
<tr>
<td>SPV-132 07</td>
<td>431</td>
<td>364</td>
<td>2.27E+10</td>
</tr>
<tr>
<td>SPV-132 08</td>
<td>431</td>
<td>366</td>
<td>2.19E+10</td>
</tr>
<tr>
<td>SPV-132 09</td>
<td>430</td>
<td>362</td>
<td>2.33E+10</td>
</tr>
<tr>
<td>SPV-132 10</td>
<td>429</td>
<td>362</td>
<td>2.31E+10</td>
</tr>
<tr>
<td>SPV-132 11</td>
<td>428</td>
<td>359</td>
<td>2.42E+10</td>
</tr>
<tr>
<td>SPV-132 12</td>
<td>429</td>
<td>362</td>
<td>2.31E+10</td>
</tr>
<tr>
<td>SPV-132 13</td>
<td>431</td>
<td>363</td>
<td>2.32E+10</td>
</tr>
<tr>
<td>SPV-132 14</td>
<td>434</td>
<td>365</td>
<td>2.31E+10</td>
</tr>
<tr>
<td>SPV-132 15</td>
<td>435</td>
<td>365</td>
<td>2.33E+10</td>
</tr>
<tr>
<td>SPV-132 16</td>
<td>433</td>
<td>364</td>
<td>2.32E+10</td>
</tr>
<tr>
<td>SPV-132 17</td>
<td>428</td>
<td>361</td>
<td>2.33E+10</td>
</tr>
<tr>
<td>SPV-132 18</td>
<td>428</td>
<td>360</td>
<td>2.37E+10</td>
</tr>
</tbody>
</table>

All of the wafers used for the experiment had a background iron concentration of less than 5.0E+10 atoms/cm³. This concentration was calculated using Equation 1 which defines the relationship between the change in diffusion lengths and iron concentration.

Equation 1: Calculation of [Fe] using SPV diffusion lengths before and after activation.

\[
Fe(cm^{-2}) = 1.05 \times 10^{16} (L_1^{-2} - L_2^{-2})
\]

A. Iron Analysis

Diffusion lengths of the wafers implanted with iron decreased dramatically. This was expected because the FeB complex is a fairly effective trap. When the wafers were exposed to light during the activation step, the pairs disassociated and the diffusion lengths dropped further because the interstitial Fe trap is more effective than the FeB pair. After the 24 hour recombination period, the diffusion lengths fully recovered and after photodisassociation returned to the same level as observed in Figure 1.

Figure 1: Diffusion lengths of Fe implanted wafers before and after activation, prior to and proceeding a 24 hour recombination period.

The corresponding diffusion lengths and iron concentrations are given in Table II.

Table II: Fe dose and resulting [Fe] calculated.

<table>
<thead>
<tr>
<th>Fe Dose (E+11 ions/cm²)</th>
<th>M2D1 (um)</th>
<th>M2D2 (um)</th>
<th>M3D1 (um)</th>
<th>M3D2 (um)</th>
<th>[Fe] (cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1E+11</td>
<td>202</td>
<td>58.8</td>
<td>202</td>
<td>58.9</td>
<td>2.77E+12</td>
</tr>
<tr>
<td>5E+11</td>
<td>85.8</td>
<td>25.7</td>
<td>85.8</td>
<td>25.6</td>
<td>1.46E+13</td>
</tr>
<tr>
<td>1E+12</td>
<td>63.6</td>
<td>20.8</td>
<td>63.3</td>
<td>20.6</td>
<td>2.21E+13</td>
</tr>
<tr>
<td>1E+11</td>
<td>194</td>
<td>55.8</td>
<td>193</td>
<td>55.8</td>
<td>3.09E+12</td>
</tr>
<tr>
<td>5E+11</td>
<td>84.2</td>
<td>25.3</td>
<td>84.0</td>
<td>25.2</td>
<td>1.50E+13</td>
</tr>
<tr>
<td>1E+12</td>
<td>63.3</td>
<td>20.6</td>
<td>63.0</td>
<td>20.5</td>
<td>2.23E+13</td>
</tr>
</tbody>
</table>

These values for the observed iron concentrations are slightly higher than would be expected at these doses by approximately a factor of two. The wafers used were approximately 675um thick so the resulting concentration should have been 1.48E+12 cm⁻³ for the lowest implanted dose. The calculated [Fe] of 3E+12 cm⁻³ indicates that the implant dose was actually 1.87E+11 cm² opposed to the targeted dose of 1E+11 cm².

B. Chrome Analysis

The diffusion lengths of the Cr implanted wafers were reduced after photodissociation. The diffusion lengths for each chrome dose are summarized in Table III.
Table III: Diffusion lengths of chrome implanted wafers before and after photodisassociation.

<table>
<thead>
<tr>
<th>Cr Dose (cm²)</th>
<th>M2D1 (um)</th>
<th>M2D2 (um)</th>
<th>M3D1 (um)</th>
<th>M3D2 (um)</th>
<th>[Fe] (cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1E+11</td>
<td>403</td>
<td>281</td>
<td>402</td>
<td>281</td>
<td>6.80E+10</td>
</tr>
<tr>
<td>5E+11</td>
<td>396</td>
<td>257</td>
<td>394</td>
<td>257</td>
<td>9.13E+10</td>
</tr>
<tr>
<td>1E+12</td>
<td>396</td>
<td>253</td>
<td>392</td>
<td>252</td>
<td>9.70E+10</td>
</tr>
<tr>
<td>1E+11</td>
<td>407</td>
<td>278</td>
<td>405</td>
<td>279</td>
<td>7.09E+10</td>
</tr>
<tr>
<td>5E+11</td>
<td>401</td>
<td>249</td>
<td>398</td>
<td>250</td>
<td>1.02E+11</td>
</tr>
<tr>
<td>1E+12</td>
<td>404</td>
<td>268</td>
<td>400</td>
<td>267</td>
<td>8.17E+10</td>
</tr>
</tbody>
</table>

The amount of chrome implanted into the wafer does not track with the perceived iron concentration. If the CrB pairs were disassociating, the diffusion length should have increased with chrome dose. Also, by comparing M2D1 to M3D1 in Table III, it can be seen that the diffusion lengths fully recovered after the twenty four hour recombination period. Which is not long enough for CrB pairs to reform. Therefore the “iron” that is calculated using the SPV method is believed to be iron that was contributed by the implantation process.

Table IV: Summary of copper implanted wafer diffusion lengths.

<table>
<thead>
<tr>
<th>Cu Dose (cm²)</th>
<th>M1D1 (um)</th>
<th>M1D2 (um)</th>
<th>M2D1 (um)</th>
<th>M2D2 (um)</th>
<th>M3D1 (um)</th>
<th>M3D2 (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1E+11</td>
<td>431</td>
<td>363</td>
<td>424</td>
<td>344</td>
<td>406</td>
<td>341</td>
</tr>
<tr>
<td>5E+11</td>
<td>434</td>
<td>365</td>
<td>426</td>
<td>316</td>
<td>372</td>
<td>301</td>
</tr>
<tr>
<td>1E+12</td>
<td>435</td>
<td>365</td>
<td>433</td>
<td>187</td>
<td>208</td>
<td>165</td>
</tr>
<tr>
<td>1E+11</td>
<td>433</td>
<td>364</td>
<td>426</td>
<td>317</td>
<td>370</td>
<td>306</td>
</tr>
<tr>
<td>5E+11</td>
<td>428</td>
<td>361</td>
<td>412</td>
<td>317</td>
<td>412</td>
<td>345</td>
</tr>
<tr>
<td>1E+12</td>
<td>428</td>
<td>360</td>
<td>414</td>
<td>192</td>
<td>215</td>
<td>171</td>
</tr>
</tbody>
</table>

Diffusion lengths of the copper implanted wafers did not fully recover after the recombination period. The level to which the diffusion length drops after photodisassociation is dependent upon the copper implant dose. The level to which the diffusion length recovers is attributed to iron because it’s not dependent upon the copper dose. This data is summarized in Table V.

Table V: Summary of copper effect on perceived [Fe].

<table>
<thead>
<tr>
<th>Cu Dose (cm²)</th>
<th>Initially Perceived [Fe] (cm³)</th>
<th>Cu Induced [Fe] Error (cm³)</th>
<th>Actual [Fe] (cm³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1E+11</td>
<td>3.03E+10</td>
<td>5.29E+09</td>
<td>2.50E+10</td>
</tr>
<tr>
<td>5E+11</td>
<td>4.73E+10</td>
<td>1.80E+10</td>
<td>2.93E+10</td>
</tr>
<tr>
<td>1E+12</td>
<td>2.44E+11</td>
<td>1.87E+11</td>
<td>5.76E+10</td>
</tr>
<tr>
<td>1E+11</td>
<td>2.88E+10</td>
<td>4.00E+09</td>
<td>2.48E+10</td>
</tr>
<tr>
<td>5E+11</td>
<td>4.26E+10</td>
<td>1.48E+10</td>
<td>2.78E+10</td>
</tr>
<tr>
<td>1E+12</td>
<td>2.24E+11</td>
<td>1.66E+11</td>
<td>5.77E+10</td>
</tr>
</tbody>
</table>

To achieve a better understanding of the surface to bulk concentration variations, the standard plot used to extract diffusion length by SPV was expanded to include more measurements at varying wavelengths. Shown in Figure 3 is one such plot for the wafer with the highest copper implant dose.

Figure 3 shows that there is a slight increase in copper concentration near the surface (indicated by the slight curving near the zero point). However this is not enough to significantly effect the resulting diffusion length that is inferred from the plot.

C. Copper Analysis

During the SPV testing sequence, wafers implanted with copper reacted very differently than either chrome or iron implanted wafers as can be seen in Figure 2.

The copper does not affect the initial diffusion length (See Table IV or Figure 2) which indicates that either the copper in it’s current form is not a very effective trap or is located at the surface where it would not be seen using SPV. However the ability to see an effect of copper after photodisassociation indicates that the iron must already be in the bulk. That is because it is highly unlikely that a light pulse would inject copper atoms from the surface into the bulk.
Taking all of this information into account, it appears that copper, already present in the bulk of the silicon, is being somehow altered during the photodisassociation step to form a much more effective trap. It is possible, however, that more than one trap is formed during this activation since the diffusion lengths measured do not fit the same type of equation as iron to arrive at a contaminant concentration. Another measurement technique, such as deep level transient spectroscopy (DLTS), will need to be used to determine exactly what trap or traps are formed.

4. CONCLUSIONS

Surface photovoltage is a fast and reliable way to determine iron contamination levels in p-type silicon. Chrome levels appear to have little effect upon diffusion length measurements and do not cloud iron results when a photodissociation step is performed to break FeB pairs. Copper concentration has an effect upon the perceived iron concentration in a sample and has the ability to lead to erroneously high results. A second measurement made after a 24 hour iron and boron recombination period, leads to a more exact iron measurement.

REFERENCES


ACKNOWLEDGEMENTS

The author acknowledges the Integrated Sensor Solution and Analytical Technology Divisions of the Eastman Kodak Company for their financial support of this project and Dean Seidler and Albert Filo of Eastman Kodak for their guidance in this work.

Steven V. Nagel, originally from Candor, NY, received a B.S. degree in Microelectronic Engineering from the Rochester Institute of Technology in 2000. He attained co-op work experience in the Image Sensor Solution division of Eastman Kodak in the dielectric films and DI water areas. He is joining Microchip Technologies as a process engineer starting in June 2000.
The Effect of Fluorine on Boron Diffusion

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Abstract – The role of fluorine in a BF$_2$ implant has been investigated by implanting BF$_2$, B alone and different combinations of B and F at equivalent implant energies. Each combination was designed to test for something, such as the effect of fluorine after B was implanted or the F damage before B was implanted. The wafers from each group received a spike anneal at 1075°C. The resulting boron profiles after implant and after spike anneal were obtained by SIMS analysis. Sheet resistance was measured and compared with the values calculated from the profiles. The junctions with boron implant had the smallest sheet resistance whereas those obtained with boron implant following F implant had the largest sheet resistance. The SIMS profiles supported these results. The profiles do suggest that the presence of fluorine reduced the transient enhanced diffusion of boron.

1. INTRODUCTION

MOS devices are shrinking in lateral dimensions, leading to the need for ultra-shallow source/drain junctions. These depths are projected to be less than 500Å for 0.18µm and beyond technology nodes. The technology to produce these ultra-shallow junctions with low sheet resistance has yet to be fully developed. The implant techniques used currently need to be modified to get junction depths that shallow. These modifications include low energy implants, pre-amorphization of the substrate to minimize channeling, dopant activation by spike anneals or at low temperatures and/or minimize transient enhanced diffusion (TED). Transient enhanced diffusion is due to excess interstitials caused by the implant damage. At the end-of-range, where the damage from the implant meets the crystalline structure, the interstitials occur and may cause the TED of dopants further into the substrate increasing the junction depth. This is particularly a concern for boron.

To minimize this effect, BF$_2$ is commonly used to introduce boron into silicon. The main advantages in using BF$_2$ include reduction in channeling due to amorphization of the surface, being heavier than B so it doesn’t travel as deep into the substrate and low temperature dopant activation by SPE (solid phase epitaxy) also due to amorphization. Another benefit of using BF$_2$ is that the beam current is higher in BF$_2$ gaseous source, therefore shorter implant time are made possible for heavy doses.

A cited paper shows a BF$_2$ ion implantation (compared to a B implant) produced a higher sheet resistance due to shallow junction depths [8]. This seems to be a common theme in other related papers. Many try to propose explanations to this phenomenon including the following. One found that the diffusion and interstitial population was consistently lower in the BF$_2$ implant compared to the B implant. This was attributed to residual F, increased stability of end-of-range defects, and the effect of amorphization on B clustering reactions. [4]. Another paper attributed it to lower energy. It claimed that it was one of the benefits of lowering the energy because of mobility reduction, retained dose and the fluorine depletion from the substrate. [2]. Some cited authors propose that the reduction in diffusion is due to a smaller concentration of interstitials. Although there has been much research and many proposed theories, there has been no final answer as to why fluorine retards boron diffusion.

2. EXPERIMENTAL DESIGN

The implants were done using 8-inch, n-type wafers with a resistivity of ~ 1 ohm cm. All the implants were done at Texas Instruments, using the LEAP in drift mode (no deceleration). The wafers were implanted for a total of six different splits. The first split was a BF$_2$ implant at a dose of 5E14 cm$^{-2}$ at an energy of 10keV. This was the implant that was to be studied. The second split was B implanted at a dose of 5E14 cm$^{-2}$ at an energy of 2.2keV. This was the equivalent energy for B [(11/49) of BF$_2$ energy]. The third split was F implanted at a dose of 1E15 cm$^{-2}$ at an energy of 3.9keV and then B implanted second at a dose of 5E14cm$^{-2}$ at an energy of 2.2keV (ratio of 2:1). This was done so the F could pre-amorphize the substrate before being implanted with B. The fourth split was implanted with F at a dose of 5E14 cm$^{-2}$ at an energy of 3.9keV and then was implanted with B at an energy of 2.2keV and a dose of 5E14 cm$^{-2}$ (a ratio of 1:1). This was done to study the extent of damage
fluorine causes to the substrate and how it effects the junction. The fifth split was implanted with B at a dose of 5E14 cm\(^{-2}\) at an energy of 2.2keV and then implanted with F at a dose of 1E15 cm\(^{-2}\) at an energy of 3.9keV (a ratio of 1:2). This was done to study the effect of F on Bboron diffusion. The sixth and final group was implanted with F only at an energy of 3.9keV at two different doses (5E14cm\(^{-2}\) and 1E15 cm\(^{-2}\)). This was done to study just the damage caused by F in silicon.

There were three wafers in each group except for the last one listed (this split only had two). After the implants, one wafer from each of the first five groups received a spike anneal at 1075°C (done using a laser pulsed for almost zero time). Table 1 shows the detailed experimental design for each wafer.

The sheet resistance was measured using four point probe for each group following the spike anneal and SIMS analyses were performed for both as-implanted and annealed samples at Charles Evans & Associates.

3. RESULTS

A. TRIM Simulations

Figures 1 and 2 show the simulated profiles for F (3.9keV) and B (2.2keV) respectively. Each shows a projected range of around 1BÅ, which is an underestimate. This is because TRIM does not take into account secondary effects such as channeling backscattering, or dynamic annealing.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Dose (cm(^{-2}))</th>
<th>Energy (keV)</th>
<th>Species (\rightarrow)</th>
<th>Spike Anneal @ 1075°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5E14</td>
<td>10</td>
<td>BF(_2)</td>
<td>no</td>
</tr>
<tr>
<td>2</td>
<td>5E14</td>
<td>10</td>
<td>BF(_2)</td>
<td>no</td>
</tr>
<tr>
<td>3</td>
<td>5E14</td>
<td>10</td>
<td>BF(_2)</td>
<td>yes</td>
</tr>
<tr>
<td>4</td>
<td>1E15</td>
<td>3.9</td>
<td>F</td>
<td>no</td>
</tr>
<tr>
<td>5</td>
<td>1E15</td>
<td>3.9</td>
<td>F</td>
<td>no</td>
</tr>
<tr>
<td>6</td>
<td>1E15</td>
<td>3.9</td>
<td>B</td>
<td>no</td>
</tr>
<tr>
<td>7</td>
<td>1E15</td>
<td>3.9</td>
<td>F</td>
<td>yes</td>
</tr>
<tr>
<td>8</td>
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<td>yes</td>
</tr>
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<td>9</td>
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<td>no</td>
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<td>12</td>
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</tr>
<tr>
<td>16</td>
<td>1E15</td>
<td>3.9</td>
<td>F</td>
<td>no</td>
</tr>
<tr>
<td>17</td>
<td>1E15</td>
<td>3.9</td>
<td>F</td>
<td>yes</td>
</tr>
</tbody>
</table>
B. Sheet Resistance

The measured sheet resistance for the different combinations is given in Table II.

Table II — The calculated and measured sheet resistance (plus standard deviation) for the different implant splits.

<table>
<thead>
<tr>
<th>Species</th>
<th>R_s-meas. (Ω/sq)</th>
<th>S.D.- meas. (%)</th>
<th>R_s-calc. (Ω/sq)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BF₂</td>
<td>390</td>
<td>1.0</td>
<td>376.2</td>
</tr>
<tr>
<td>2F + B</td>
<td>417</td>
<td>0.9</td>
<td>394.1</td>
</tr>
<tr>
<td>F + B</td>
<td>380</td>
<td>1.3</td>
<td>363.1</td>
</tr>
<tr>
<td>B</td>
<td>363</td>
<td>2.3</td>
<td>328.3</td>
</tr>
<tr>
<td>B + 2F</td>
<td>389</td>
<td>1.7</td>
<td>328.0</td>
</tr>
</tbody>
</table>

B. SIMS Results

The SIMS plots for different samples are shown in Figures 3-6. Figure 3 shows the boron profile after the spike anneal for BF₂ implant. The comparison between BF₂ and B implant shows that the B implant travels much further into the substrate (Figure 4). The B + 2F implant vs. 2F + B implant shows that the B + 2F implant travels deeper into the substrate. This is shown in Figures 5 and 6, the latter having a shallower slope.

Figure 3.-6. SIMS plot showing boron profiles for various implant conditions following spike anneal at 1075 °C.
4. DISCUSSION

The Sheet resistance was calculated from the boron profiles using the relation

\[ R_s = \frac{1}{q \int_{0}^{x_t} C_B(x) \mu_p(x) dx} \quad (1) \]

where the \( x \) position is taken from the SIMS results at every other Angstrom, starting at 2A into the substrate. The doping at each of these \( x \) positions, \( C_A(x) \) is also obtained from the SIMS analysis. The mobility is calculated using the doping value (at each \( x \) value) from the following equation

\[ \mu_p = 54.3 + \frac{407}{1 + 3.745E^{-18} * C_B(x)} \quad (2) \]

The integral in the sheet resistance calculation goes until the junction depth is reached. This depth is taken when the doping dropped down to \( 1E16 \text{ cm}^{-3} \). These calculated values are listed in Table II. The calculated sheet resistance is a little lower than the measured sheet resistance for a few possible explanations. There could be inactive dopant in the junction, which differs because the calculation assumes that all the boron in the profile is electrically active. Other reasons could be that the depletion region is not taken into account or that the mobility model assumed may not be accurate.

The table shows that the boron implant gives the smallest sheet resistance (363 \( \Omega/\text{sq} \)). This is because channeling and transient enhanced diffusion causes deeper boron penetration. The highest sheet resistance (417 \( \Omega/\text{sq} \)) was measured for the 2F + B implant. This is due to the pre-amorphization caused by the fluorine, which prevents channeling and produces shallower junctions. The F + B implant gives a sheet resistance value in between the BF2 implant and the B implant (380 \( \Omega/\text{sq} \)). This shows that the fluorine does help reduce the the TED of boron and that the more implanted (up until a certain limit), the more reduction seen in TED and junction depth. The B + 2F implant shows a similar sheet resistance value as the BF2 implant. This shows that the fluorine has a chemical influence on the boron diffusion. This finding was also reported in another cited paper [3]. This showed that fluorine effect on TED was independent of the effects of the implant and any pre-amorphization (reduction of channeling) that may occur. Another experiment showed that fluorine accumulated near the surface and end-of-range defects. The paper tried to explain the retardation of boron diffusion by saying that the interactions of F with the defects reduced the number of interstitials in the substrate. [6]

Another study tried to determine whether the influence of fluorine was chemical or damage related. To eliminate the damage factor, the substrate was pre-amorphized before the implant to see if fluorine still played a role in the boron diffusion. A chemical effect was determined to occur. Some possible explanations given in this paper were (1) F may bind with Si interstitials chemically and reduce B diffusing using them, (2) F may bind with B at low temperatures, preventing boron to form a mobile pair with an interstitial and (3) F may enhance interstitial recombination reducing the number of interstitials in the substrate for the boron to diffuse through. [7]. These are just a few of the many possible explanations found in the cited works of how fluorine effects the diffusion of the boron (chemically).

5. CONCLUSION

The effect of fluorine on boron diffusion has been studied. From the results, B gave the smallest sheet resistance. This is because channeling and TED caused deeper boron penetration. The combination of 2F + B gave the largest sheet resistance. This is due to the fluorine causing pre-amorphization, which prevents channeling, therefore producing a shallower junction. The group 1F + B gives smaller sheet resistance than BF2; but larger than B alone. This shows that fluorine does help in reducing TED and the more implanted (up until a certain limit) the more reduction seen in TED and junction depth. The final observation is that the sheet resistance for B + 2F is similar to BF2. This shows that the fluorine has a chemical effect on boron diffusion because the damage part of fluorine does not come into play.

REFERENCES


ACKNOWLEDGEMENTS

I would like to thank Dr. Amitabh Jain of Texas Instruments, for his guidance and support throughout the course of this study. I would also like to thank Dr. Santosh Kurinec of RIT for her advice and interest on this investigation. Finally, I would like to thank Suraj Bhaskaran of RIT for helping with TRIM simulations.
RIT Process and Device Simulation with Microtec

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Abstract—Microtec, a diffusion-drift model simulator by Siborg Systems, Inc., was used to simulate RIT's process for a 2-micron NFET (Long Channel), a scaled-down NFET (Short Channel), and our new advanced CMOS Process NFET. The accuracy of the simulator was tested with voltage threshold curves, sub-threshold characteristic tests, potential distribution plots, doping profiles, and oxide growth measurements. Microtec proved to be able to easily model RIT's device performance and process characteristics with only a small amount of modification.

1. INTRODUCTION

The purpose of the experiment is to investigate the performance of the Microtec Simulation tool from Syborg systems to verify the 2μm NFET process developed and manufactured at RIT. Initial investigation was difficult due to some of the limitations of the tool, but once a workaround was discovered work progressed quite well. The majority of the problems centered on the fact that Microtec will only simulate one oxide growth per section of the device. This made it very difficult to accurately model the process because even the implants are done through a screening oxide to achieve the proper profile and projected range. It was determined that the best method to model the devices was to break them up into three individual regions. The first region was the channel region which had the gate oxide growth on it and was not subjected to the V_T adjust implant. The second and third regions where very similar. The only difference is the drain is oriented around the x=2.5μm and the source is oriented around x=0μm. Both the drain and the source regions were simulated with the Kooi oxide growth and then implanted with the V_T Adjust implant.

2. Oxide Growth Measurements

Microtec doesn't calculate the oxide grown at the surface of the silicon. The value for the oxide grown was, instead, calculated by the amount of silicon consumed at the surface divided by 0.44. Figure 2 below illustrates the amount of oxide grown and the bird's beak.

Simulation showed a wet oxide growth result for the Filed Oxide of 11102Å compared to a target of 10000Å. For the Kooi oxide the result was 1061Å versus a target of 1000Å. The dry oxide growth of the gate oxide showed a very similar trend in the results with 536Å in simulation against a target of 500Å.
3. RIT "FACTORY NFET"

The process details for the RIT "Factory NFET" can be found in reference [1]. The gate oxide thickness was 532Å as indicated in part 2.

A. Doping Profiles

Figure 3 shows the net doping concentration as a contour plot for the x (across the device) and y (into the substrate). The differences in color represent a decade of change in the Doping concentration. It is clear from this contour plot that the Channel length of the device is about 2μm. This device for purposes of easy reference will be referred to as the RIT "Factory NFET" from now on.

B. Voltage-Threshold Calculation

The threshold voltage was calculated by extrapolating a line tangent to the linear portion of the drain current vs. gate voltage and recording its intersection with the Vg axis, as illustrated in Figure 5. The simulated V_T for the RIT "Factory NFET" was 1.22V versus a target of 1V. The most likely reason for the discrepancy was the amount of oxide charge was estimated below that of the devices created in our Factory.

C. Family of Curves

The "family of curves" in Figure 6 illustrates the long channel behavior of the device. The early voltage was measured to be greater than [200V]. The graph was obtained by applying a fixed voltage to the gate (indicated
by the Vg column to the right of the graph) and then ramping the voltage from 0 to 5V on the drain while measuring the current on the drain.

D. Sub-Threshold Characteristics

The sub-threshold swing in Figure 7 was modeled to be about 125mV/dec. An ideal device would be about 100mV/decade. The off-state leakage current was estimated at 10^{-14} A/μm. This estimation does not take into account reverse bias junction leakage for the device, which would dominate with the gate voltage near 0 volts.

4. SCALED-DOWN NFET

A. Doping Profiles

The laterally scaled NFET has a channel length of 0.5μm as illustrated in Figure 8, but is otherwise identical to the RIT "Factory NFET". The junction depth remained .75 μm and the oxide thickness was 532Å. The design of this experiment was to test the hypothesis that a scaled-down device would not perform adequately. In order to produce working devices at 0.8-0.5μm, there would be a need to design a new process.

B. Voltage Threshold Calculation

The threshold voltage for the scaled-down NFET was calculated in the same manner as was used for the RIT "Factory NFET". The value was 0.97V as can be seen in Figure 9. The most likely reason for the reduction of the threshold voltage from that value of the RIT "Factory NFET", was due to V_T Roll off.

C. Family of Curves

The family of curves in Figure 10 shows a much worse state of affairs. The extreme slop of the curves is due to channel length modulation and the Early voltage was extrapolated to be [2.1V].
D. Sub-threshold Characteristics

In Figure 11 it is clearly evident that the scaled-down device has serious problems. The RIT "Factory NFET" is included for comparison purposes. The Sub-threshold swing of the scaled-down NFET was calculated to be approximately 7.5 V/decade. The off-state current was simulated at 10^6 Amp per μm. Again it is important to note that this calculation doesn't take into account reverse bias junction current, but it offers a significant contrast to the Long channel device.

5. RIT's SUB μm CMOS

A. Device Structure

From the results of the Scaled-down NFET it is clear that a new process needs to be designed for RIT to produce working devices with channel lengths of 0.8-0.5 μm. Extensive credit needs to go to Suraj Bhaskaran for the figures and results in this section. Figure 11 illustrates a 2D cross section of this newly designed NFET and PFET. Some of the features of this new process include a Dual well, LDD structures, 150Å Gate oxide, Titanium Salicide contacts, 14 Thermal steps, 7 implants (but no V_ADJUST implant).

B. Voltage Threshold Calculation

The threshold voltage for the RIT Sub μm CMOS was calculated in the same manner as was used for the RIT "Factory NFET". The value was 1.02V as can be seen in Figure 13 versus a target of 1V.

C. Family of Curves

The family of curves in Figure 14 indicates a much better performing structure than the scaled-down NFET. Channel length modulation is still present in the device but has been reduced yielding an Early Voltage of approximately 20V.

D. Sub-threshold Characteristics

Figure 15
Figure 15 illustrates the improved sub-threshold swing of approximately 100mV/decade. This combined with the off-state leakage current of about $10^{-14}$ A/μm, illustrates the benefits of the new process that was designed for devices of this size.

6. CONCLUSION

Microtec is a very capable simulator that correctly reflected the results consistent with the RIT fabrication plant. In order to move from the original 2μm NFET to a 0.8μm-0.5μm NFET simulation verified it is necessary to design a new process. The new Microtec release due this summer will allow for even more accurate process and device simulations.

REFERENCES


ACKNOWLEDGMENTS

The author acknowledges Dr. Karl Hirschman, and Suraj Bhaskaran for guidance in this work and Syborg Systems for creation of the Microtec software.

Charles R. Overbeck, originally from Lebanon, OH received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at National Semiconductor and VLSI Technology. He is joining Apple Computer, Inc as a Design-For-Test Engineer starting July 2000.
The Beneficial Effects of Thin Film Stress in the Fabrication of a MEMS Device

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Abstract—Microelectromechanical systems (MEMS) are playing an increasing role in the semiconductor industry today. The modeling and manufacturing of mechanical devices on a microscopic level have made their way from the area of singularly fabricated devices for research into the bulk processing of the commercial market. Many of these commercial devices are of the optical variety. And there has also been successful work done in combining integrated circuits with MEMS. Presented here is a process for the fabrication of an optical device called a microshutter.

The device consists of a moveable electrode constructed of a stack of SiO₂/Al/SiO₂. The key to the successful micromachining of this device lays in the stress characteristics of the stacked layer. The physical qualities and methods of obtaining these stresses will also be discussed.

1. INTRODUCTION

A microshutter is a MEMS actuator that is capable of rolling a stacked layer of thin films into itself and unrolling it. This device may be used in regulating the transmission of light waves passing through an underlying substrate. Its practical applications lie in the field of electric display devices. The function of the microshutter will be discussed first, however.

The central aspect of the microshutter is a stacked layer of sputtered thin films. A layer of SiO₂/Al/SiO₂ is patterned to create a long rectangular “shutter” attached to a contact (image 1: appendix).

This layer will remain curled in on itself during the off state when there’s no external voltage applied to the device (image 2: appendix). This is due to the interaction of stresses in the different layers. When a voltage is applied to the device the layer rolls out just like a window shutter unrolls. Through control of the voltage it is possible to determine the rate of the curling and uncurling of the microshutter.

In order to utilize the microshutter in an electrical display there must be arrays of the devices fabricated. These arrays would be assembled on top of a glass substrate. The substrate would pass either white light or ultraviolet light, and an array of shutters would then regulate when this light was allowed to pass. The placement of color filters above certain arrays of microshutters would then allow the microshutters to control what color was viewed [1].

There are many issues involved in producing a successful microshutter. The most crucial is obtaining the correct stress characteristics in the thin film stack. This device utilizes a lower SiO₂ layer with compressive stress and a middle Al layer with tensile stress.

Compressive stress is the application of a force that squeezes a member together. In semiconductor processing this will cause a thin film to buckle and look like a bubble or dome from above [2].

Tensile stress is the application of a force that pulls a member apart. This is normally seen as cracking or lifting in thin films [2].

Both of these stresses are necessary for a functional microshutter. And they must be present in a substantial amount.

Stiction is another important issue that must be considered when making the device. When the microshutter is unrolled it will be making contact with the surface beneath it. The microshutter must not become stuck to the substrate; or else the device will be ruined.

The last problem to be discussed here is the charge transfer between the upper electrode and the lower electrode. When the stacked film that makes up the microshutter is at rest in the off state there is no voltage applied to it and charge transfer is not an issue. However, when a voltage is applied and it unrolls the close proximity to the lower electrode allows for charge to be lost.

This reduces the voltage on the upper electrode, and the electric field is weakened. Consequently the electrode will prematurely drift upward out of its rigid on state.

The fabrication of a microshutter and the crucial steps to combat the previous issues is presented here.
2. PROCEDURE

A. Design

Numerous variations of microshutters were included in the overall design. There were three groups of identical arrays that consisted of eight rows of eight square microshutters (metal: appendix 2). There were also three other groups of differing arrays. One contained rectangular microshutters, and another consisted of couplets of thin rectangular microshutters. The final array was composed of hammerhead shaped microshutters.

There was also a number of individual microshutters that were designed. They were all taken from the molds used for the microshutters in the arrays; there were squares, rectangles, hammerheads, and coupled rectangles.

The layout for the overall design of the microshutter involved six separate masks for four levels (appendix 2). The first level was a layer of silicon oxide that was patterned with the Top Contact Window mask for a contact to the lower electrode. The second level was a layer of aluminum that was patterned with the Contact mask in order to provide protection for the aluminum contact with a coating of photoresist.

The third level was a sacrificial layer that would remain underneath the microshutter. The third layer was defined with both the Active mask and the Dimple mask. The Active mask was used in order to define the size of the sacrificial area, and the Dimple mask was used patterned long thin lines into the sacrificial layer.

The fifth mask, Metal, was used to pattern the microshutter onto the stacked film of SiO2 / Al / SiO2. And the final mask, Contact Window, was used on the same level in order to provide a contact to the upper electrode.

B. Processing

The problematic issue of charge transfer from the lower electrode to the upper electrode was the simplest to correct. The growth of 1000Å of SiO2 was used as an insulating layer between the lower electrode, which in this case was the substrate, and the upper electrode, the stacked thin films.

Following the oxide growth patterning of a contact to the lower electrode was performed using the Top Contact Window mask on the GCA 6700 g-line stepper. The program used was MEMS1\TRENCH. The contact to the substrate was etched, and the wafer was then sputtered with a layer of aluminum.

This layer was patterned with the Contact mask using the MEMS1\ACTIVE program. The aluminum was etched in order to define a contact, and the exposed photoresist was left on the wafer in order to protect the aluminum contact from damage in later steps.

Spin coating a sacrificial layer of Shipley 812 photoresist was next. This layer was exposed first with the Active mask, using the MEMS1\METAL program. It was then exposed again before development of the first exposure with the Dimple mask, using the MEMS1\ALIGN program.

The patterning of the “dimples” in the sacrificial layer was done in order to combat the issue of stiction with the device. Lines running the length of the patterned sacrificial layer were created in order to reduce the contact that the bottom layer of the stacked thin films would have with the oxide layer. Exaggerated cross-sections of this layer are shown in appendix 1.

The “dimples” also provide the added effect of strengthening the stiffness of the stacked layer. This aids in preventing it from curling perpendicular to the direction that it is intended to roll up in [1].

The sputtering of the stacked film followed the coating of the sacrificial layer. The desired thickness for each level of the stacked layer was 300Å. The SiO2 / Al / SiO2 layer was sputtered in a Perkin-Elmer X-Randex Model 2400. Both of the silicon oxide layers were sputtered at 700W for 4 minutes with an argon flow of 30sccm at 10mTorr of pressure. The aluminum was sputtered at 100W for 5 minutes with an argon flow of 60sccm at 5mTorr of pressure. These recipes were run in order to obtain a compressive stress in the silicon oxide layer and a tensile stress in the aluminum layer.

Following the sputter the wafers were patterned with the second mask set using the Metal mask with program MEMS1\TRENCH. This defined the shape of the microshutters. A contact to the upper electrode of the stacked films was then exposed onto the layer before the previous pattern was developed. This was done with the Contact Window mask, using program MEMS1\ACTIVE on the GCA 6700 g-line stepper. The patterns were then developed in the photoresist and the stacked film was etched in phosphoric acid.

As in most MEMS devices the removal of the sacrificial layer is an important step and also the last step performed. The photoresist that still remained on the wafer, following the etching of the stacked layer, was the sacrificial layer beneath the microshutters and the covering of the aluminum contacts to ground.

These patches of photoresist were removed using an O2 plasma in an asher for ten minutes.
3. RESULTS

The sputtering of the silicon oxide resulted in 800Å for both the top and bottom layers. While there was 300Å of aluminum sputtered. The characteristics of these thin films are shown below:

<table>
<thead>
<tr>
<th>Material</th>
<th>Average Stress</th>
<th>Maximum Stress</th>
<th>Center Stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>-18 MPa</td>
<td>-115 MPa</td>
<td>-70 MPa</td>
</tr>
<tr>
<td>Al</td>
<td>126 MPa</td>
<td>235 MPa</td>
<td>147 MPa</td>
</tr>
</tbody>
</table>

The negative signs are used to denote the compressive stress of the silicon oxide, and the tensile stress is valued as positive.

The wet oxide growth for the insulation layer resulted in 1180Å of SiO₂.

4. DISCUSSION

The increased thickness of the insulating oxide layer was not a serious problem, since the insulating layer is not crucial to the function of the device. However, the increased thickness of the SiO₂ presented a difficulty.

The process used for depositing the silicon oxide did not provide a large compressive stress. Therefore the addition of weak silicon oxide would only help to prevent the microshutter from curling up when the sacrificial layer was released.

Possible modifications could be made to the recipe for the sputtering of the SiO₂ in order to increase its compressive stress. One method would be to bombard the surface of the silicon oxide with ions. The momentum transfer from the ions to the SiO₂ atoms would move them into closer proximity with each other. This would result in a compressed state for the film once the growth was completed. This method is known as “ion peening” [3].

Another method that could be used to create a higher compressive stress would be to add material beneath a deposited layer. Chemical reactions that occur during the deposition process could produce this stress if they were reacting for some time beneath the growth surface of the thin film. When the growth surface rises and the thin film begins to harden the extra material would cause the compressive stress beneath it. This is typically performed in a poor vacuum with oxygen purposefully added as a background gas in order to cause oxidation [3].

Another difficulty in the process besides obtaining the correct film stress was the simple alignment of masking levels. The program recommended for use with the mask set was CMOSMIXA.FAC, however the alignment marks were not located in the same place for this mask as they were for the masks used with the CMOSMIXA.FAC program. The MEMS1 program was able to find the alignment marks though.

Therefore large amounts of time were spent on simply trying to align subsequent levels of the device. Significant X and Y alignment errors were evident on the second level, though the following levels aligned correctly with the second level.

The main result of this was that the contacts to ground were made thinner due to the protective coating of photoresist being offset. There were also a number of sacrificial layers that did not line up correctly with the microshutters patterned in the stacked film that was deposited on top of them.

5. CONCLUSION

The microshutter was unable to be manufactured successfully due to the weak compressive stress of the SiO₂ layer and the increased thickness of this layer. Alignment issues with the GCA 6700 g-line stepper also prevented the successful placement of many devices.

The design and implementation of a process, along with the difficulties found, for this device have left it as a good project for future work. Possible enhancements would be fabricating the device on a glass substrate and adding the color filters as previously discussed.

REFERENCES


ACKNOWLEDGEMENTS

The author would like to thank Dr. William Grande for his support and direction in this project as well as Mathew Daniello and Debbie Demejo for their work on the microshutter masks.

Justin Brown, originally from Cape Cod, Massachusetts, received a B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at Intersil (formerly Harris Semiconductor) in Palm Bay, FL and Motorola in Austin, TX. He is planning on enjoying his summer and then working in the New England area for the fall of 2000.
Abstract— Monolithic integration of CMOS and MEMS is quickly proving to be a viable asset to current complex structures. However, synthesis of these technologies has proven to have multiple processing obstacles. Depending on the method used to create these devices, the hurdles include the effects of silicon etching and high temperature processing. For this experiment, previously processed CMOS wafers were obtained and a trench was etched into the silicon. “Family of curves” plots of the working CMOS wafers were taken before and after processing to study any changes in $I_D$. Results have shown that the processing of this integration will effect the family of curve plots, however this was not concluded as a result of a small sample size.

1. INTRODUCTION

Complementary Metal Oxide Semiconductors (CMOS) transistors are playing a dominant role in today’s society ranging from basic to complex structures. With the processing ideas behind CMOS transistors, a new idea about shrinking macro-mechanical devices was created, known as MicroElectroMechanical Systems (MEMS), including such devices as electro-motors, actuators, shutters, and more. As the demand for complex semiconductor devices increases, there is a need to integrate MEMS with driving, controlling, and signal processing CMOS electronics.

This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process. Performance of devices will be better by reducing impedance’s when testing MEMS sensor structures by having the system analysis in close proximity. Today’s systems have the MEMS device in their own package and subsequently are running wires to machines, such as Rochester Institute of Technology’s HP4145 Analyzer used in the Microelectronic Engineering department. For example, in the case of transducers which convert mechanical forces to capacitance energy, it is important to keep the distance from the transducer to the analyzing electronics as small as possible. This reduces stray capacitances and noise due to considerably deteriorating circuit performance.

In order to integrate these technologies, three different methods have been developed including CMOS first, MEMS first, and interleaving. The CMOS first method was developed by Berkeley researchers, and is used extensively with Texas Instruments for manufacturing of their Digital micro-Mirror Devices (DMD). With this method, the aluminum metallization of CMOS is replaced with tungsten so that the circuitry can withstand the following MEMS processing. However this method has some processing challenges when processing the MEMS. One such problem is it requires high temperature processing to dope and relieve mechanical stress in the polysilicon layers. The MEMS first approach, developed by Sandia National Laboratories, is a flexible, modular manufacturing process for the monolithic integration. Using this method, a trench is first etched into the silicon to a certain depth. Micromechanical structures are placed into the trench and thereafter filled with a sacrificial layer of low-temperature oxide (LTO). The LTO is then planarized so that the electronics are placed onto the wafer without the worry of destroying the MEMS structures, or thin photoresist stresses from the rough topography. The interleaving method, used by Analog Devices for their accelerometers, allows for processing of both the CMOS and MEMS throughout the entire course of manufacturing. The only major drawback to this is the rough topography from the micromechanical devices, which can ultimately cause larger critical dimensions for the circuitry.

This experiment will combine ideas from the MEMS first method with the CMOS first method. Working CMOS wafers will be used and a trench will be wet etched into the silicon wafer after a protective layer of silicon nitride is deposited onto the surface. Wet etch solution of potassium hydroxide (KOH) was used for a couple of reasons. First is that KOH etching is a well-established technology dating back to the early 1960’s. Secondly, it is orientation dependent; and for this case, the etch will be anisotropic. Thirdly, the non-etched regions can easily be protected by Si$_3$N$_4$, which is also a well-established technology at Rochester Institute of Technology.

This type of work offers numerous advantages to RIT’s microelectronic program. One such advantage will allow for student designed micromachines to be electrically...
tested, which historically has proven to be problematic due to poor electrical connections. Furthermore, the availability of PMOS, CMOS, and bipolar processes at RIT would allow the MEMS designer a great deal of flexibility because a technology could be selected that easily presents appropriate impedances to the micromachined devices.

2. PROCESS FLOW

The first part of this experiment was to acquire and test completed CMOS wafers. To do this, a box of 15 finished RIT CMOS Gate Array wafers were found and electrically tested. This first test was used to determine which wafers still work. This information will also be used to compare and contrast the wafers when processing in completed. Figure 1. is a wafer map that refers to the die location of the tested transistors.

![Wafer map](image)

Figure 1. Wafer map showing the locations of the electrical testing (numbered die). The colored blank areas refer to regions of thickness measurements. The rest are gate array dies.

The next step in the process is to perform an aluminum etch on the entire substrate. It is desired to have all the aluminum removed as a result of future high temperature processing. After this, a quick RCA clean is to be accomplished before a silicon nitride deposition. However, this RCA clean will not have a HF dip. The purpose of this clean is to remove any particulates on the surface that may have been left on the substrate after the aluminum etch. Therefore, the HPM, APM, and spin rinser will suffice. It has been determined in previous experiments that a deposition thickness of 10000 will satisfy the requirements for later processing.

Photolithography is the next step in the process. This step will be used to act as a mask when etching the silicon nitride. However, a hand made reticle is used for this processing using black tape to block the hv light. Referring to figure 1, the areas that are exposed are the die that are neither numbered or colored. Alignment is not critical in this stage for this experiment.

A quick plasma silicon nitride etch using SF6 gas is performed next using RIT's GEC Plasma Cell. This machines etches silicon nitride at a rate of 15000/minute. However, since the desired thickness is 10000, the etch time should be a third less. Following the plasma etch, a wet etch in hydrofluoric acid is rendered to remove any oxide in the etched region followed by an ash to remove the photoresist.

Now, a quick silicon etch in KOH is performed. The reason that a quick etch is done is that only a small trench depth is desired. This depth should not be too deep because future MEMS processing will be done in this area and a deep trench will cause unwanted stress on thin films, such as photoresist. After the etch, the wafers are to be cleaned in DI-water and finally spin rinse dried. This is to ensure that the wafers are properly cleaned and will not continue etching the wafer. Figure 2. shows the wafer after the silicon etch.

![Image](image)

Figure 2. Theoretical look at a cross section of a die after the KOH etches. Visible are the oxide and nitride layers used in masking the non-etched regions.

Next, the second photolithographic level is done for contact cut lithography. This step is used to create open regions for the aluminum to come in contact with the active area of the transistor. However, the major difference between this lithography step and the previous is that a larger amount of photoresist is used to prevent streaking. As a result of not filling in the etched silicon region, the holes must be filled with photoresist, or the thin resist will streak and cause highly non-uniform coatings.

Another silicon nitride etch is done to create the contact holes to the active area region. As with the previous nitride step, the etch time will be short. Again, after the etch, a quick HF etch is done to remove any native oxide that may be on the substrate.

An aluminum sputter deposition is next using RIT's CVC601 sputterer. A low base pressure is desired to achieve a high level of uniformity on the substrate. To help attain the low pressure at a faster rate, a preheat of the system is to be done. The expected thickness of the aluminum after the deposition is 50000.

The final photolithographic step is now performed to pattern the aluminum and create contact pads. As with the second photolithographic level, a large amount of photoresist is used to prevent any streaking. The wafers are then put into a wet phosphoric acid to etch the aluminum at 50°C for two minutes. Plasma etching is not needed here because the dimensions are so large. The
resist is then ashed off so that a sinter can be performed. A sinter is the step that creates good ohmic contact of the aluminum to the transistor. Sintering is performed in RIT's Bruce Furnace at 450°C for 30 minutes.

Finally, all of the wafers are electrically tested again to determine whether this process will effect the transistors. Results are compared to the original figures and an analysis is completed. Figure 3. shows a cross sectional view of the wafer after processing in complete.

Figure 3. Cross sectional view of the wafer after all processing is complete.

3. EXPERIMENTAL PROCEDURE

Of the 15 wafers originally obtained, only 5 of them were working. Additionally, of the 5 that were working, one wafer broke while trying to remove an identifying sticker. In addition to the four remaining wafers, 2 more were used for experimentation or measurements, along with 3 dummy wafers.

Preliminary research was performed on the first aluminum etch to determine the length of time. Originally, the phosphoric bath was heated to 50°C, where the wafers would etch for 2 minutes. After a preliminary investigation, 2 minutes of etch time was not enough since not all of the aluminum was removed. Most of the aluminum was removed, however a strange pattern was discovered which showed that the aluminum was etching faster near the edge of the wafer. This indicated that it is possible that the aluminum is thicker in the center of the wafer and didn't receive a uniform deposition, when originally processed. It was then determined that a higher temperature bath of 70°C would remove the aluminum faster, without ruining the devices. This was concluded to be true after another test wafer was etched for 45 seconds.

Following a standard RCA clean, a nitride deposition was performed using the ASM 6″ LPCVD. The furnace was heated to 800°C with a deposition pressure of 360mTorr. Two separate gases were used during the deposition, NH₃ and SiH₂Cl₂. A new bottle of dichlorosilane was used in this experiment and was discovered that the concentration was about half of normal processing at RIT. To compensate, a longer deposition time of 35 minutes was calculated to achieve the target thickness of 1000O. However, the deposition rate was faster than anticipated and an average thickness of 1250O per minute was found.

All photolithography steps were hand coated and developed. Each step began with a 250°C dehydration bake for 2 minutes to insure that there was no water on the surface for promoting resist adhesion. Next, the photoresist, Shipley 812, was applied to the substrates and spun at 4500rpm for 60 seconds. A 90°C soft bake was done on the wafers for 60 seconds. Next, the wafers were exposed using the GCA 6700 g-line stepper for 0.4 seconds. A post-exposure bake was performed at 120°C for 60 seconds. The wafers were then developed in CD-26 developer. A final hard bake was performed at a temperature of 125°C for 60 seconds.

A nitride etch was done using the GEC Plasma Cell using SF₆ gas. An etch time of 1 minute was used as a result of the increased thickness as compared to the desired. As indicated earlier, the etch rate of this machine is 5000 per minute and the thickness of the nitride was 12500. The over etch was felt to be okay, and would be used to make sure that all nitride was removed in the desired areas. This was the condition for both the etching steps.

The HF etch step was determined to be a long etch. Preliminary investigation found that the thickness of the underlying oxide to be approximately 75000. It was then determined that an etch of 25 minutes in length should clear all areas. Nanospec readings confirmed that this time was enough.

The silicon etch in KOH was performed at a temperature of 70°C. Preliminary investigations found that a 10 second etch would produce a depth of ~2μm. This depth will be too shallow since most micromechanical structures are larger than this. Therefore, etch times of 30 and 60 seconds were investigated. After the etch, the wafers were cleaned in DI-water and spin rinsed clean.

Sputter deposition was done using the CVC601 in the RIT Microelectronic facilities. The conditions for the sputter deposition are listed in table 1.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Pressure</td>
<td>3.60E-05</td>
</tr>
<tr>
<td>DC Watts</td>
<td>2000</td>
</tr>
<tr>
<td>Gas</td>
<td>Ar</td>
</tr>
<tr>
<td>Sputter Pressure (mTorr)</td>
<td>4.6</td>
</tr>
<tr>
<td>Preheat Temp. (degrees C)</td>
<td>300</td>
</tr>
<tr>
<td>Preheat Time (min)</td>
<td>20</td>
</tr>
<tr>
<td>Deposition Time (min)</td>
<td>20</td>
</tr>
<tr>
<td>Expected Thickness (Ang)</td>
<td>5000</td>
</tr>
</tbody>
</table>

Table 1. Sputter conditions.

The actual thickness of the deposited aluminum was found to be 6800O.
The second aluminum etch was performed using the standard recipe of 50°C, however this time the etch time was found to be 105 seconds. This is believed to be a result of changing the phosphoric acid, causing a change in the concentration.

Finally, the wafers were sintered using the Bruce Furnace at a temperature of 450°C for 30 minutes. A standard recipe set up by RIT was used in this experiment without any deviations. After the sinter, wafers were again tested and compared to the original results.

4. RESULTS AND ANALYSIS

Electrical testing had proven to show that MEMS processing after CMOS processing does effect the performance of the transistors. Refer to figure 4, which shows the results of die #7 of a wafer that received a 60-second silicon etch. The graphs in figure 4 are representative of all the working transistors. When comparing the results of the original to the post processing, the first thing that was noticed was that the $I_d$ value decreased by a 3x factor. It is believed that this is a result of the nitride deposition, since it was done at a temperature of 800°C under vacuum for 35 minutes. It is theorized that this temperature caused the dopants to diffuse further into the silicon, causing extra resistance. In accordance to Ohm's law,

$$I = \frac{V}{R}$$

the current will decrease as a result of the increasing resistance, while the voltage remains constant. The second thing that was noticed was that the Early voltage ($V_A$) had decreased after processing. For the transistor listed above, the $V_A$ changed from −25.4 volts before processing to −54.0 volts after processing. The third thing that was noticed was that the barrier layer had changed causing the turn-on voltage ($V_T$) to increase. It is believed that this was caused by a poor sinter, causing poor ohmic contact. Therefore, an additional sinter was perform and tested again. Figure 4-c shows the results after the second sinter. It is noticed that there wasn’t much of a change in the electrical performance, and it appears that the second sinter had no affect on the barrier layer. It could be concluded that this was not a result of a poor sinter but of something else, however additional testing should be done to confirm this.

Figure 5 shows an NMOS transistor after the experiment. The small squares within the larger squares represent the nitride contact cut, while the larger squares represent the original contact cut. The difference in size is a result of the nitride receiving a plasma etch, while the original cut was done with a wet etch. Also, closer inspection shows that there was some alignment problems with this experiment. Figure 6 shows the result of the etched silicon hole after sputter deposition of aluminum. The rough topography of the etch is a direct result of the mask that was made with black tape. It should be noted that the pattern is part of the gate array device.
Matthew J. Daniello, originally from Rome, NY, received a B.S. in Microelectronic Engineering from Rochester Institute of Technology in May, 2000. He attained co-op work experience at Eastman Kodak Co as a Photolithographic Process Development Engineer. He is joining White Oak Semiconductor as a Process Engineer starting June 2000.

5. CONCLUSION

This experiment is the first of many to come since RIT is trying to ramp up their efforts in the integration of MEMS with CMOS. These preliminary results show that a lot of effort and consideration are needed if the CMOS first method is to be implemented into practice. Despite the resulting outcome of the transistor performance, more experiments need to be conducted to verify the validity. Additionally, further experiments should also consider using the MEMS first approach and then compare the results.

REFERENCES


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Process Development for an Anti-Reflective Micromechanical Modulator

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Abstract- The purpose of this Senior Design project is to design and develop the process for an Anti-Reflective Micromechanical Modulator at RIT’s facility, based on AT&T Bell Laboratories presented device, OFC ’94). The device is fabricated using common semiconductor materials and is used to reflect a laser signal. There are 2 states of operation: the optically ON state, which reflects the signal, and the optically OFF state, which cancels the signal out through destructive interference. A three-layer mask process was designed on RIT’s IC Layout software, the levels being the Active, Metal, and Sacrificial Evacuation areas. The process steps include 4 Lithography steps, Thermal Oxide, LPCVD Nitride, Spin On Glass, and Chemical Mechanical Planarization. Some processing issues that are dealt with are the CMP of the SOG, the photo patterning of metal on a planar surface, and the removal of the sacrificial material/freeing the membrane. The optical operation of this device is not within the scope of this project.

1. INTRODUCTION

The Anti-Reflective (A-R) Membrane is an optical micromechanical device, which has two states of operation. The optically ON state reflects a laser signal. The optically OFF state, through destructive interference, cancels the signal. The anti-reflective membrane is designed to be one-quarter the signal wavelength thick, and the height of the membrane from the substrate is some multiple of one-quarter wavelength.

The device layout is not a new design. Preston designed a structure similar to the one used in this paper, in which he called “Deformable Membrane Mirror Light Modulator” (MLM) in 1968. His paper was referred to by a more recent patent from Optron Systems, who’s structure was based on the MLM in 1995 (US Pat. 5471341). A competing structure was introduced by Texas Instruments as being a Digital Micro-mirrored Device (DMD) which received a patent the same year, 1995 (US Pat. 5457566). My structure is based on the device presented by AT&T Bell Labs during the 1994 Optical Fiber Communications conference, as shown in Figure 1. The potential uses for the A-R Membrane are projection television systems, optical computer systems, multispectral infrared target simulation, and optical communications, which was AT&T Bell Labs’ use.

2. MASK DESIGN AND LAYOUT

Using RIT’s IC Layout software, the mask was designed to have multiple structures with varying dimensions. These included two, three, and four electrode devices while varying both membrane and electrode lengths and widths. Also included in the design were simple array structures of the two-electrode design. Both membrane and electrode dimensions varied. Finally on the device, a Thermal Actuator was designed, with similar, but the realization of this device was not in the scope of this project and is left as future work.

The main two-electrode device, with labeled materials, is shown in Figure 2.

As an example of the varying design, the structure in Figure 2 varied in Length of membrane (from 20um to 200um), in Width of membrane (from 10um to 70 um), the width of the electrodes (from 4um to 20um) and the Ove
Hang of the electrodes (from 8um to 23um). This was done similarly for the other device structures.

3. PROCESS DEVELOPMENT

The designed process contains three mask layers, but requires four photolithography steps (the second step is used to clear the aluminum from the alignment die for proper alignment of the metal etch layer). The process steps are as follows:

1. p-type starting substrate
2. Standard RCA clean
3. Thermal Oxide growth ~4000Å
4. Nitride Deposition ~1000Å -CMP barrier
5. Photo-pattern Sacrificial Trench
6. Dry Etch Nitride -SF6 50 Watt, 1min
7. Wet Etch Oxide -Buffered Oxide Etch
8. Strip Resist –Ash
9. Spin On Glass -Accuglass 512, 2000rpm, 1min
-120°C hotplate, 2min
-425°C cure, 60min, N2
10. Chemical Mechanical Polish
   -Concentric Groove Rodel IC1000-A1
   -Bayer Levisil 100, 45%
   -6PSI, 60rpm, 1min polish +30 sec rinse
11. Nitride Deposition ~1000Å Membrane
12. Aluminum Deposition ~2500Å Electrodes
13. Photo-pattern Metal
14. Wet Aluminum Etch -Hot Phosphoric Acid ~1.5 min
15. Strip Resist –Ash
16. Photo-pattern Sac. Removal Windows
17. Wet Etch -Buffered Oxide Etch Sac. Material ~5min
18. Strip Resist –Acetone and blow dry

Because the optical operation of this device was not within the scope of this project, the trench height and membrane thicknesses are arbitrary.

The final resist strip should not involve any heat; otherwise the membrane will adhere to the substrate through stiction. Other forms of releasing the membrane need to be investigated.

4. PROCESS ISSUES

The most significant process issue was that of the planarization of the sacrificial material. The material first proposed for the sacrificial layer was a Low Temperature Oxide (LTO), but in order for the film to start planarizing itself during deposition, the film thickness would have to be on the order of microns, causing a deposition time of hours, and lengthened polish time. But there was a risk in choosing the SOG, as the expiration date was June ’94. But this ended up begin the wisest choice due to the planarity of the material and the potential selectivity for the CMP process.

The other issue, which RIT doesn’t have the capability or the equipment to tackle is that of stiction.

5. RESULTS AND CONCLUSIONS

The polishing results of the LTO are as shown in Figure 3. It shows the post polish data, both visual and profile, of the resulting sacrificial trench. It is clear that the next step (nitride membrane deposition) on top of a non-planar surface such as this would not result in a working device. There is ~2000Å of dishing, and as the photo shows, there is still LTO on top of the nitride CMP barrier. The polishing of this material was unsuccessful.

![Figure 3. Top view and height profile following the CMP LTO](image_url)

The following table shows the step height across the same features as in Figure 3, but the sacrificial material is Spin On Glass. This table represents the final profile heights after CMP.

<table>
<thead>
<tr>
<th>Device Wafer</th>
<th>Step Height (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D22</td>
<td>165</td>
</tr>
<tr>
<td>D23</td>
<td>580</td>
</tr>
<tr>
<td>D24</td>
<td>215</td>
</tr>
<tr>
<td>D25</td>
<td>218</td>
</tr>
</tbody>
</table>

As for device results, two devices worked. The processing issue that is holding MEMS devices such as these from working at RIT is that of stiction. Some proposed methods of avoiding stiction are (1) evaporation drying of DI water, (2) evaporation drying of methanol,
two different sublimation drying techniques, or supercritical drying with CO$_2$.

AKNOWLEDGEMENTS

I would like to acknowledge Professor W. Grande for his wealth of knowledge and experience in the MEMS field and for being this project’s Advisor, Dr. Fuller for the process advisement of the Spin On Glass, and to the equipment support. This project couldn’t have been completed on time without the help of the “Nightshift Seniors” spending too much time in the fab.

REFERENCES


Jason Neidrich, originally from Rochester, NY, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op experience from Rochester Institute of Technology in CMP under Dr. R. Lane, at Advanced Vision Technology, and Xerox in the Ink Jet Business Unit, CMP. He is joining Texas Instruments as a process engineer in the Digital Light Processor group in June 2000.
Copper Interconnect Development
At RIT

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Abstract—Aluminum is the current metal of choice for metallization in the IC industry. However, serious electromigration problems, and inferior thermal stability limit its performance and reliability. Copper is an attractive alternative having higher electrical conductivity and improved electromigration performance compared to Aluminum. However, Cu is a fast diffuser in Si, SiO2, and interlevel dielectrics (ILD). To eliminate this issue, a layer of diffusion barrier (DB) material which is conducting, chemically passive with Copper, has good adhesion properties with Cu and ILD and has high thermal stability is required.

Damascene process for Cu was utilized to pattern the wafers in this study. Ta, TaN, Ti and TiN were used as barrier layers. The DB were deposited using pulsed DC sputtering (Ta and Ti) and reactive sputtering (TaN and TiN). A seed layer of Cu was deposited in the same sputtering tool. The wafers were electroplated with Cu and polished using CMP. They were then analyzed using SEM and a high-resolution optical microscope. No electrical tests were conducted at this stage due to lack of multilevel masks.

INTRODUCTION

With the advancement in microelectronics field, properties of thin films and their processing, especially in the field of metal interconnects have gained more interest and demand within the past few years. A high performance interconnect is urgently needed to quench the demands dictated by Moore’s Law.

Cu has an intrinsically higher electrical conductivity compared to Aluminum. As a result there will be a gain in virtually all the chips that will utilize Cu interconnect. This alone is a big motivation for transferring to Cu interconnect technology.

A. Issues in Metallization

1. RC Delay [1]

The carrier transient time across the length of the channel decreases with the device dimension reduction. These carrier charges capacitatively couple with the ILD, leading to RC delay. For a MOS circuit, the RC delay is defined in terms of the circuit response, which is given by:

\[ V_{out} = 1 - e^{-t/RC} \]

where, \( V_{out} \) is input voltage of the circuit, \( t \) is the time, \( R \) is the total resistance of circuit, \( C \) is the total capacitance of the circuit. RC time constant can be determined by the following equation:

\[ RC = \rho L^2 z_{ILD} / t_{M} / t_{ILD} \]

where, \( \rho \), \( t_{M} \), \( L \), \( z_{ILD} \), and \( t_{ILD} \), respectively are – the resistivity, thickness, length of interconnection, and interlevel dielectric permittivity and thickness.

With the increase in chip speeds, RC time delay becomes a bigger issue than ever before.

2. Electromigration [1]

Electromigration occurs when a conductor is subjected to high current densities at opening conditions where atomic diffusion is high, leading to a mass transport association with atomic flux divergence. The enhance and directional mobility of atoms are caused by (a) the direction influence of the electric field on the ionized atoms and (b) the collision of electrons with atoms, leading to a momentum transfer and atom movement. The atomic flux due to electromigration in the single crystal or large-grained crystal, where the grain-boundary contribution to atomic diffusion can be neglected, is given by as:

\[ J_{atoms} = NDZ* qj / (\rho kT) \]

Where \( N \), \( D \), \( Z^* \), \( q \), \( j \), \( \rho \), \( k \), and \( T \) are atomic density, atomic diffusivity, effective charge on the moving ions, electron charge, current density, electrical conductivity, Boltzmann’s constant, and temperature in degree Kelvin respectively. Electromigration can lead to break in interconnections and functional failure of the integrated circuits at large.
B. Copper Metallization

Aluminum has been the most commonly used material for metallization. It has a relatively low electrical resistivity, it has halide compounds with a relatively high pressure which are suitable for reactive ion etching (RIE). It can form a protective oxide film that can withstand various thermal processes and has good adhesion to oxide.

With the reduction in feature sizes, planarization of Al occurs via high temperature process. This places a stringent demand on the integrity of the barrier to prevent junction spiking caused by Al/Si interdiffusion. For metallization of VLSI circuits, Al has a major drawback – electromigration. For ultra-large scale integration (ULSI), the electrical resistivities of Al and its alloys are not low enough. As the circuit geometry shrinks, Al and its alloys will need to be replaced by other interconnect materials.

Copper offers low resistivity (1.7 μΩcm) compared to Aluminum (2.7 μΩcm). Cu also offers ease of deposition, and a higher melting point than Al. Cu also has electromigration orders of magnitude lower than Aluminum.

Even though Copper offers many advantages, it is has its own sets of issues.

Cu diffuses rapidly in Si and acts as an electron trap. Three acceptor levels in the middle of the Si band gap at 0.24 eV, 0.37 eV and 0.52 eV with respect to valence edge are formed. These levels provide a mechanism for excess minority carrier recombination with excess majority carriers. This in turn induces a generation-recombination leakage current in p-n junctions and degrades the performance of the transistors leading to a reduction in the current gain.

Copper forms the silicide Cu3Si by reacting with the substrate at temperature less than 200 °C. After the formation of the Cu3Si phase, the underlying Silicon in that Cu3Si/Si structure is readily oxidized even at room temperature, resulting in rapid growth of a layer of SiO2.

Unlike Aluminum, Copper is readily oxidized to form Cu2O and CuO phase at low temperature and no self-protective oxide layer is formed to prevent Cu from further oxidation. CuO and Cu2O degrade the electrical and mechanical properties of Copper. The lack of self-passivation layer makes Copper thin film susceptible to oxidation during processing.

Copper layer exhibit poor adhesion on both oxide and polymer substrate. In general, interfacial adhesion is strongly related to the bonding, surface morphology and stress relaxation at the Cu/substrate interface.

The aforementioned Copper issues can be reduced or completely eradicated with the use of diffusion barriers, passivation layers and adhesion promoters.

In this study the effort to understand diffusion barriers and their adhesion properties were the key focus of attention at RIT. CMP and step coverage were the other aspects that were looked at as well.

EXPERIMENTAL

The procedure had 5 primary steps, namely:

i. Oxide Growth
ii. Pattern Formation and Oxide Trenching
iii. Barrier/Seed Layer Deposition
iv. Electroplating of Copper
v. Chemical Mechanical Planarization (CMP) of Cu

Oxide Growth

Four-inch p-type bare Si wafers were used to grow the initial oxide. At RIT a horizontal Bruce Furnace is utilized to grow thick wet oxide.

Following furnace conditions were used to grow a ~10,000 Å of SiO2.

<table>
<thead>
<tr>
<th>Move</th>
<th>Time</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boat in</td>
<td>00.0 min</td>
<td>25 °C</td>
</tr>
<tr>
<td>Push In</td>
<td>12.0 min</td>
<td>800 °C</td>
</tr>
<tr>
<td>Stabilize</td>
<td>15.0 min</td>
<td>800 °C</td>
</tr>
<tr>
<td>Ramp to 1100 °C</td>
<td>30.0 min</td>
<td>1100 °C</td>
</tr>
<tr>
<td>O2 Flood</td>
<td>05.0 min</td>
<td>1100 °C</td>
</tr>
<tr>
<td>Soak</td>
<td>3-hr 30.0 min</td>
<td>1100 °C</td>
</tr>
<tr>
<td>N2 Purge</td>
<td>05.0 min</td>
<td>1100 °C</td>
</tr>
<tr>
<td>Ramp Down</td>
<td>55.0 min</td>
<td>25 °C</td>
</tr>
<tr>
<td>Pull Out</td>
<td>15.0 min</td>
<td>25 °C</td>
</tr>
</tbody>
</table>

Pattern Formation and Oxide Trenching

MIT Cu-damascene test mask was used for this purpose. This mask includes lines and spaces and boxes ranging from 1μm – 30 μm in size.

A GCA stepper was utilized to transfer the pattern from the mask onto the wafer. Standard RIT photo-steps were used to coat, expose and develop the photoresist.

The wafers were then subjected to a HF dip for 5 minutes. This process trenched the oxide in the areas where the substrate was exposed after the photoresist development.

The wafers were then placed in an O2 plasma Asher to remove the unexposed photoresist remaining on the wafers.

Barrier/Seed Layer Deposition

A CVC601 sputter tool was used for deposition purposes in this study. This tool has the ability to handle 4 different substrates up to 8" in size. Depending upon the target placement and utilization within the tool, it was at
times possible to sputter Cu-seed layer just after the barrier layer deposition.

The various parameters for different barrier layers are given below in Table 1.

### Table 1

<table>
<thead>
<tr>
<th></th>
<th>Ta</th>
<th>TaN</th>
<th>Ti</th>
<th>TiN</th>
<th>Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target</td>
<td>8&quot;</td>
<td>8&quot;</td>
<td>4&quot;</td>
<td>4&quot;</td>
<td>4&quot;</td>
</tr>
<tr>
<td>Power (W)</td>
<td>1000</td>
<td>1000</td>
<td>650</td>
<td>650</td>
<td>400</td>
</tr>
<tr>
<td>Time (min)</td>
<td>25</td>
<td>25</td>
<td>20</td>
<td>20</td>
<td>18</td>
</tr>
<tr>
<td>Gas</td>
<td>Ar</td>
<td>Ar.N₂</td>
<td>Ar</td>
<td>Ar.N₂</td>
<td>Ar</td>
</tr>
<tr>
<td>Gas Ratio</td>
<td>5.5:1</td>
<td>1</td>
<td>5.5:1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Pressure (Mt)</td>
<td>5</td>
<td>5.5</td>
<td>5</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>Thickness (Å)</td>
<td>1150</td>
<td>1200</td>
<td>1250</td>
<td>1100</td>
<td>1100</td>
</tr>
</tbody>
</table>

The gas flow into the chamber was 200 sccm. The best vacuum achieved was \(4.2 \times 10^{-5}\) mTorr. Various gas ratios were looked at before coming up with the final Ar:N₂ ratio for the TaN and TiN deposition.

### Electroplating of Copper

A ReynoldsTech non-rotational plating cell was used for this purpose. The wafers were sent to ReynoldsTech to be plated since an identical tool at RIT, is currently in the process of being installed.

Figure 1 shows a diagrammatic layout of the specified tool.

The electroplating parameters that were used during electroplating were:

- Plating Temperature 26.0 °C
- Copper Sulfate conc. 10oz/gal
- Sulfuric acid conc. 25 oz/gal
- Chloride 0 oz/gal

### Table 2

<table>
<thead>
<tr>
<th></th>
<th>Current</th>
<th>Voltage</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stage 1</td>
<td>0.2 A</td>
<td>2.5 V</td>
<td>5 min</td>
</tr>
<tr>
<td>Stage 2</td>
<td>1.0 A</td>
<td>7.5 V</td>
<td>15 min</td>
</tr>
</tbody>
</table>

A ~2 μm thick Copper layer was deposited on top of the seed layer.

**Chemical Mechanical Planarization (CMP) of Cu**

CMP was done using a Strasbaugh single wafer tool. A Rodel IC 1000/Suba V pad was used to polish the wafers.

The condition were as follows:

- Table rpm 48
- Carrier rpm 46
- Pressure 5 psi
- Time 8 min

Alumina based slurry (pH 1.5) was used for this purpose. The composition of the slurry was as follows:

- DI water
- BTA
- \(H₂O₂\)
- \(HNO₃\)

### RESULTS/ANALYSIS

Only adhesion and deposition related parameters were studied in this phase of this work. Due to the lack of instrumentation and dual level masks, a complete electrical and multi-level property investigation of the process could not be conducted. Using a scanning electron microscope (SEM) and a high-resolution optical microscope, the samples were analyzed. Majority of the SEM analysis was done at University of Rochester – Optics Lab. Following were the various substrate images obtained for this study.

The TaN wafer broke prior to the CMP. This resulted in excluding it from post CMP analysis.

On visual inspection the Ta, TaN and Ti wafers show a good film of electroplated Cu. When the wafers were cleaved for X-sectional analysis, the TiN wafer showed extremely high level of peeling.

Most of the analysis was conducted on the Ta barrier layer wafers. This was due to two reasons – firstly, TaN wafer polished properly and secondly, time constraint. If
there was more time available then other wafers would have been analyzed.

In Figure 2 (page 5) 30µm features/20µm spaces (Cu) are seen. The features are oxide islands and the channels are Cu filled. There appears to be slight dishing within the channels and can be seen by looking at the changing gradient of the color. This will later on be confirmed using a profilometer. A similar pattern with wider spacing between the islands can be seen in Figures 3 & 4 (20µm feature/30µm spacing).

The reverse situation where the islands (boxes) are Cu and the spacing between them are oxide, can be seen in Figure 5 (page 5). There appears to be minimal dishing. This could be attributed to smaller size for the feature.

Figure 6 shows 10µm lines and spaces. They appear to be very well defined and filled on optical observation. The next image, Figure 7, shows even thinner lines (5µm) and they too appear to be in excellent condition. Even further level of gap filling and feature resolution was observable. In Figure 8, 9µm lines and 1µm spaces were resolved, filled and polished.

A case of underpolish can be seen in Figure 9 that was observed after CMP in and around the center of the wafer.

Figure 10 (page 6) shows the X-sectional SEM image of this Ta barrier layer wafer. As can be observed from this image, there appears to be no peel of any sorts and a good adhesion between the substrate and Cu. T (1) relates well with the visual inspection upon cleaving wafer, where TiN wafer had Cu peel off and Ta, TaN did not show any kind of Copper peeling.

Figure 11 (page 6) shows the flip side of the above situation. This was a TiN wafer. The Cu appears to have been lifted completely off. There seems to be no adhesion between the substrate and Copper.

The electrical properties were not looked at in this study.

CONCLUSION

This study was conducted to look at the feasibility of understanding of the electrical properties of the different layers and levels.

FUTURE WORK

The need to further develop and understand the Copper interconnect process at RIT will require the following:

- Better analysis (SEM 's)
- Electrical testing
- Optimization of deposition parameters (barrier and seed layer)
- Tool startup (Electroplating, CMP)
- Multilevel mask for damascene process
- Investigation of low-k dielectrics
- More information and support from the industry

ACKNOWLEDGMENTS

The author acknowledges Dr. Santosh Kurinec for her valuable support and advice and guidance in this work, R Battaglia and R Persaud for their help and support, Microelectronic staff and faculty, Brian McIntyre, Jason Meiring, Steven Sudirgo, Mark Bossard Dr. Lane and ReynoldsTech.

REFERENCES


He is joining National Semiconductor Corporation as a CMP Process engineer starting June 2000.
Image Appendix

Figure 2

Figure 3

Figure 4

Figure 5

Figure 6

Figure 7
Development of LTO LPCVD Process for 6" Wafers at RIT

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Abstract—Low Temperature Oxide (LTO) thin films were prepared using a Low Pressure Chemical Vapor Deposition process. By employing statistically designed experiments, the number of experimental runs required was minimized. The full-factorial experimental design was set up to examine effects temperature, gas flow and pressure had on deposition rate, wafer to wafer uniformity, within the wafer uniformity and within run uniformity. The average deposition rate found to be 112Å per minute. The LTO baseline process conditions optimized based on the results of this project are: Temperature of 410°C, pressure of 330mTorr and gas flow ratio of 0.55.

1. INTRODUCTION

Low Temperature Chemical Vapor Deposition of silicon dioxide thin film is used in numerous VLSI manufacturing process. This type of film is typically used as insulation between poly silicon /metal layers, metal layers in multilevel systems, as diffusion and ion implantation masks, or as final passivation layers. At the Rochester Institute of Technology, low temperature silicon dioxide film use as insulation film in multi-layer metallization for CMOS and MEMS integrated circuits. The main objective of this experiment to set up a 150mm (6") wafers process for Low Temperature Oxide (LTO) at RIT's new Low Pressure Chemical Vapor Deposition (LPCVD) ASM system. The process was characterized by applying traditional statistical studies of response surface techniques. By employing statistically designed experiments, the number of experimental runs required was minimized. The experimental design was set up to examine effects temperature, gas flow and pressure had on deposition rate, wafer to wafer uniformity, within the wafer uniformity and within run uniformity. In this design, a two level full factorial screening experiment was conducted where the temperature, gas flow and pressure were varied.

LPCVD system had three zones temperature variables. From preliminary runs and based on some already known facts, first zone temperature was set up constant at 390°C, which helped to minimized the number of the runs in this experiment. The total number of runs was 9.

LTO PROCESS CHEMISTRY

1) Initiation with excited oxygen radical, represented by square brackets, to form silyl radical.

\[
\text{SiH}_4 + [\text{O}] \rightarrow [\text{SiH}_2] + \text{H}_2\text{O}
\]

2) Branching to form an intermediates Si-H-O compound:

\[
\text{SiH}_2 + \text{O}_2 \rightarrow [\text{SiH}_2\text{O}] + [\text{O}]
\]

\[
\text{SiH}_2\text{O} + \text{O}_2 \rightarrow [\text{SiH}_2\text{O}_2] + [\text{O}]
\]

3) Regenerating and terminating:

\[
[\text{SiH}_2\text{O}_2] + \text{O}_2 \rightarrow \text{SiO}_2 + \text{H}_2\text{O} + [\text{O}]
\]

4) Overall Reaction is

\[
\text{SiH}_4 \text{ (gas)} + \text{O}_2 \text{ (gas)} \rightarrow \text{SiO}_2 \text{ (solid)} + 2\text{H}_2 \text{ (gas)}
\]

The oxygen-silane gas ratio is calculated by gas flow of oxygen divided by total flow of the gas (Oxygen +Silane). The gas flow of Oxygen was varied from 96sccm to 117sccm and gas flow of silane kept constant at 81sccm. Mass flow controllers regulated the gas flows.

2. EXPERIMENTAL DESIGN

(a) Full – Factorial Design

The LPCVD system had three zones temperature variables; first zone temperature kept at constant while varies other two zones temperature. Table 1 shows the design set up used in this experiment.

Table 1. Experimental Conditions.

<table>
<thead>
<tr>
<th>Experimental Factor</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition Temperature</td>
<td>400 to 420 C</td>
</tr>
<tr>
<td>Deposition Pressure</td>
<td>272 to 400 mTorr</td>
</tr>
<tr>
<td>Gas Ratio (Oxygen / Silane)</td>
<td>0.54 to 0.59</td>
</tr>
</tbody>
</table>

(b) Responses
At each treatment combination, there were 5 wafers measured to analyze the wafer to wafer, within wafer, and within run uniformity. Deposition time was 15 minutes for all treatment combinations. Thickness measured on Ellipsometer for 9 positions per wafer. The design and data analysis were performed with the RS/6 software at RIT. Table 2 illustrates the response variables for this LTO process. Table 3 was generated from RS/6 software randomly at each treatment combination.

Table 2. Response Variables

<table>
<thead>
<tr>
<th>Response</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition Rate (A/min)</td>
<td></td>
</tr>
<tr>
<td>Wafer to Wafer uniformity</td>
<td></td>
</tr>
<tr>
<td>Within Wafer uniformity</td>
<td></td>
</tr>
<tr>
<td>Within run uniformity</td>
<td></td>
</tr>
</tbody>
</table>

Table 3. Design of Experiment Worksheet

<table>
<thead>
<tr>
<th>RUN#</th>
<th>TEMP/ZONE2</th>
<th>PRESSURE/Torr</th>
<th>SiH4 (sccm)</th>
<th>O2(sccm)</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>400</td>
<td>272</td>
<td>81</td>
<td>96</td>
<td>0.54</td>
</tr>
<tr>
<td>2</td>
<td>420</td>
<td>272</td>
<td>81</td>
<td>117</td>
<td>0.59</td>
</tr>
<tr>
<td>3</td>
<td>420</td>
<td>400</td>
<td>81</td>
<td>96</td>
<td>0.54</td>
</tr>
<tr>
<td>4</td>
<td>400</td>
<td>272</td>
<td>81</td>
<td>117</td>
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</tr>
<tr>
<td>5</td>
<td>420</td>
<td>400</td>
<td>81</td>
<td>117</td>
<td>0.58</td>
</tr>
<tr>
<td>6</td>
<td>410</td>
<td>336</td>
<td>81</td>
<td>106</td>
<td>0.57</td>
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<tr>
<td>7</td>
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<td>81</td>
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<td>8</td>
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<td>272</td>
<td>81</td>
<td>96</td>
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</tr>
<tr>
<td>9</td>
<td>400</td>
<td>400</td>
<td>81</td>
<td>117</td>
<td>0.58</td>
</tr>
</tbody>
</table>

Equation (2)
Wafer to wafer (Unif) = 0.09700 + 0.02925 (Temp) + 0.02400 (Press * Gas).

Equation (3)
Within wafer (Uni) = 0.1724 + 0.0515 (press) + 0.0362 (Gas) - 0.0422 (Temp*Press) - 0.0225 (Temp*Gas) + 0.0195 (Press *Gas).

Equation (4)
Within wafer (Uni) = 0.1724 + 0.0515 (press) + 0.0362 (Gas) - 0.0422 (Temp*Press) - 0.0225 (Temp*Gas) + 0.0195 (Press *Gas).

4. RESULTS

(a) Deposition Rate

The contour plot of figure 1 shows minimal variation and optimum deposition rate can be obtained at a temperature of 410C, pressure of 330mTorr and fixed gas ratio of 0.566. Therefore, temperature will be fixed at 410C for uniformity analysis.

Figure 1. Contour plot of Deposition Rate at a fixed gas ratio.

(b) Wafer to wafer uniformity

The contour plot of figure 2 shows that low gas flow ratio and high pressure give ample variations. Gas ratio ranging from 0.55 to 0.57 and low pressure of (340mTorr) give minimum variation, which would be an optimum point for this process.
5. CONCLUSION

The objective of this project was to characterize the LTO process at RIT and to create a baseline LTO process. The LTO baseline process conditions recommended, based on the results of this project, are: 410°C of deposition temperature, pressure of 300mTorr and gas flow ratio of 0.55. These conditions were obtained from run number six. This optimum result average deposition rate calculated as 112Å per minute.

REFERENCES


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Karthika Sivagurunathan, originally from Sri Lanka, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2000. She attained co-op work experience at Harris Semiconductor. She is joining Analog Device Corporation as a process engineer.