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The papers which follow summarize the results of research performed by the graduating seniors from the Microelectronic Engineering Program at the Rochester Institute of Technology (RIT). In their final quarter (ten weeks) of study, the students submit a proposal for a research topic covering the relevance of their project to both the Microelectronics field and the Engineering program at RIT, as well as a tentative timetable and budget. After a faculty critique, the project is either accepted as proposed or revised. Thereafter, the student executes the research independently over the course of the quarter. The students meet weekly with the course coordinator to monitor progress, obtain supplies, and revise the experiment as results develop. In addition to the research, their results are presented orally at the Annual Microelectronic Engineering Conference and in written form in this journal. The student is free (and encouraged) to seek the guidance of other faculty members, both in and outside the Microelectronic Engineering Faculty, researchers at other institutes, or industrial colleagues.

The course is designed to model the type of activities involved in graduate study programs, hence the limited supervision of the student. It also provides the student with the opportunity to exercise the skills obtained over the last five years and/or to develop new skills. The main area of concern for the course coordinator is guidance in the areas of technical writing and oral presentation. A series of seminars, on areas of Microelectronics, that are not adequately covered in the course work, complement the experimental work. This provides the undergraduate students with an opportunity to prepare for their presentations by listening to the work of others. Overall, the Senior Seminar and Research Course offers the RIT student an unique experience to obtain competence in both technical performance and in the presentation of their work in written and oral media. These are critical areas in Engineering that are often neglected in a conventional curriculum.

We hope the reader will find this journal informative and ask your indulgence concerning any technical errors which may appear herein. While a strong effort is made to eliminate any mistakes in theory or practices, some escape our detection due to the nature of the course. We invite your comments and questions regarding any of the papers. Further details of the experiments are available upon request from the Microelectronic Engineering Office at RIT. We encourage input from others not directly involved with the Microelectronic Engineering Program at RIT so we may see ourselves through the "eyes" of others. It is this feedback which helps keep us current in our goal to provide quality engineers to the Microelectronic industry. Future issues of the Journal will continue to report on efforts to expand and improve our activities in Microelectronic Engineering.

Michael A. Jackson
Course Coordinator
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RADIATION EFFECTS ON PMOS DEVICES
Camille G. Bates
5th Year Microelectronic Engineering Student
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ABSTRACT

A Cesium-137 gamma radiation source was used to irradiate PMOS capacitors and transistors with doses of 7.50E4, 1.50E5, 3.0E5. The devices were tested for C-V and I-V data before and after irradiation. Results show that all doses created changes in the electrical characteristics, however comparison to literature was inconclusive.

INTRODUCTION

Radiation can be broken down into three different groups. Group 1 is photons which consist of gamma-rays and x-rays. Group 2 consist of electrons, protons, alpha particles, beta particles and ions. The third group consist of neutrons. These three groups cause the two major forms of radiation damage seen in electronic devices, namely displacement and ionization damage.

Displacement damage is the displacing or dislodging of atoms from their lattice site causing them to take up interstitial positions within the crystal. The former site of the now displaced atom in the lattice is a vacancy. This displaced atom, if it acquires enough energy can cause the displacement of other atoms compounding the defects within the lattice structure. Those atoms, that have not slipped back or recombined, go on to form defect complexes which act as recombination or trapping centers for minority carriers, ultimately reducing minority carrier lifetime.

Figure 1 illustrates three types of simple defects in a lattice. [11]
The results are somewhat different for ionization damage. Generally ionization in the silicon portion of the structures causes no permanent change and can be neglected. The effects caused by ionization are more severe in oxides where charged traps are produced and filled during irradiation. The ionizing process is illustrated in Figure 2 along with corresponding shifts in C-V curves.

At \( t=0 \) the condition prior to irradiation is shown. At \( t=0 \) the ionizing energy is delivered to the SiO\(_2\), and the electron hole population is generated. Immediately after ionization, the process of electron-hole recombination will occur, but so will electron transport. Electron mobility in SiO\(_2\) at room temperature is approximately 20 cm\(^2\)/v-sec while hole mobility is approximately 2\( \times \)10\(^{-5}\) cm\(^2\)/v-sec. Because of the applied voltage, any electron that does not undergo recombination will be swept to the gate and removed in picoseconds, leaving behind less mobile holes. These holes will begin a transport process towards the Si-SiO\(_2\) interface. Some holes will pass into the silicon, while others will become trapped at defect centers near the interface of the gate oxide and the bulk silicon. Figure 3 depicts actual shifts in gate voltage as a result of ionizing radiation as a function of dose for a p-channel transistor.

![Figure 2](image2.png)

**Figure 2** illustrates the ionizing process along with corresponding C-V curves. 

![Figure 3](image3.png)

**Figure 3** illustrates radiation effect on a p-channel transistor as a function of dose.
A Cesium-137 gamma radiation source was used to irradiate samples. The maximum dose output of the supply was 27000 rad(si)/hr with a photon energy of 662kev. Doses of 7.50E4, 1.50E5 and 3.0E5 were used. These doses were chosen in an attempt to simulate the results in Figure 3. Capacitors and transistors with oxide thicknesses of approximately 1000A were used. These capacitors and transistors were fabricated using RIT's standard PMOS process. After each radiation dose both capacitors and transistors were tested returning to the exact same devices on the wafer. Id vs Vg curves were obtained using the HP 4145A parameter analyzer and C-V curves were obtained using Princeton Applied Research Model 410 C-V plotter.

RESULTS/DISCUSSION

Figure 4 is representative of the three curves generated for the three transistors tested.

![Figure 4](image)

The curves for Figure 4 gave results similar to Figure 3, leading to the conclusion that ionization is the probable cause of damage. The actual gate voltage shifts were somewhat lower than predicted however this is believed to be due primarily to the dose output of the source varying by approximately 10% as a result of a malfunction of the rotating platform that is supposed to ensure uniform doses over the entire sample.

The results for the capacitors were somewhat peculiar. Theoretically what was expected to occur was an increasingly negative shift in the flatband voltage with increasing irradiation. Figure 5 is a representative of the three capacitors tested. The data was extremely repeatable for all three capacitors. The C-V curve for the first dose shifted more
negative which is in agreement with theory. Any subsequent dose actually shifted the additional curves more positive.

This is contradictory to what was expected. If an examination of the equation for the flatband voltage is performed it is evident from this equation that when each individual term is taken into consideration, the metal work function, the surface state density and the field oxide charge, that the shift in the flatband voltage should continue to be negative.

$$V_{\text{Flatband}} = \Phi_m - \frac{Q_{ss}}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{X_{ox}} \frac{x}{X_{ox}} P(x) \, dx$$

Figure 6 is an illustration of the photon interaction as a function of photon energy. The Cesium-137 radiation source has a photon energy of 662 keV which puts it in the range of causing Compton scattering. As a result it can be summarized that the photon has a greater amount of energy than is needed to free an electron from the target material which is clearly in the line of ionization.

![Illustration of the photon interaction as a function of photon energy.](image)
CONCLUSION

Radiation damage was observed in the curves of both transistors and capacitors, however in the case of the capacitors it was evident that there was more occurring in terms of radiation damage than simply ionization. A more careful examination of this phenomenon must be sought for it is known that it is possible for a device to undergo a type of self anneal "REBOUND" in which case the post radiation exposure gradual annealing of the oxide trapped charge may cause the device characteristics to behave contradictory to theoretical expectations.[3]

ACKNOWLEDGEMENTS

Dr. Wagner of RIT's physics department for all of his time and patience in allowing me access to the Cesium-137 source, Mike Jackson for all of his assistance with supplies and suggestions and Dr. Fuller for his assistance in understanding the nature of this experiment.

REFERENCES


ABSTRACT

Standard Oil's BN-975 planar diffusion sources were used to fabricate integrated resistors. Dopant transfer was done in a N2:O2:H2 ambient at 975 C. Two methods of removing the crystal defect layer formed at the surface, low temperature oxidation (LTO) and a nitric acid soak, were evaluated. Successful layer removal was achieved with the LTO. The nitric acid soak met with limited success.

INTRODUCTION

Boron nitride wafers can be used as diffusion sources for p-n junctions. This method of diffusion alleviates the uniformity and repeatability problems associated with spin-on sources and gases. It is also a much safer alternative to the carrier gas system in which the dopants are found in toxic, poisonous and corrosive liquids and gases. Ion implantation, a fourth method of impurity doping, is limited by low throughput. Planar source processing also results in fewer defects in the p regions which leads to increases in carrier lifetime and current gain and a reduction of leakage current [1].

When boron nitride is used as a diffusion source, it is mixed with silicon dioxide and formed into thin wafers. These wafers are approximately the same diameter as the wafers to be diffused. The amount of silicon dioxide used depends on the desired temperature range. Lower temperature ranges require less silicon dioxide [2]. Prior to use as dopant sources, the source wafers must first be oxidized or activated. This oxidation converts some of the boron nitride to boric oxide (B2O3). The boric oxide is transferred from the source wafers to the device wafers and serves as the source of boron for the diffusion. Once activated, the sources are good for 300 hours of use. Between runs, they must be stored at 400 C in dry N2. Prior to runs, they must be stabilized for thirty minutes at 800 C in dry N2.

Transfer of dopant occurs during the sourcing step which is done during a controlled injection of up to four volume percent H2 gas into N2 and O2 diffusion tube ambient. This is known as the hydrogen injection process. Typically, the sourcing step is only one to two minutes long since the B2O3 dopant glass is
almost instantly converted to boric acid (HBO2) [4]. Due to the higher vapor pressure of HBO2 compared to B2O3, the dopant is transferred to the silicon surface of the target wafer [1]. Chemical reactions for source oxidation and target deposition are shown below [2,3].

\[
4\text{BN} + 3\text{O}_2 \rightarrow 2\text{B}_2\text{O}_3 + 2\text{N}_2 \quad [1]
\]

\[
\text{B}_2\text{O}_3 + \text{H}_2\text{O} \rightarrow 2\text{HBO}_2 \quad [2]
\]

\[
2\text{HBO}_2 + 2\text{Si} \rightarrow 2\text{SiO}_2 + 2\text{B} + \text{H}_2 \quad [3]
\]

The HBO2 glass that is deposited on the target wafers must be reduced in a nitrogen ambient. Excessive amounts of HBO2 can lead to greater field oxide penetration. Furthermore, sticky build-ups can occur on the quartz boat and inside the diffusion tube. The HBO2 glass is reduced during a dry nitrogen soak step. As a result of the soak step, a thin insoluble layer of silicon boride, SiB, is formed at the silicon surface. At this point, the boron has been diffused into the silicon and the crystal damage has been trapped in the SiB/Si interface [5].

The SiB layer must be removed by oxidation. A thin layer of silicon below the SiB layer is also oxidized and removed. Consequently, the defects trapped in the SiB layer are also removed. Oxidation can be accomplished by a low temperature oxidation. Typically, LTO's are done at temperatures between 700-800 °C for times of ten to thirty minutes [1]. A nitric acid soak done at 90 °C for 30 minutes will also oxidize the SiB surface [5].

The wafers can be four point probed prior to the LTO growth. The resistance that is measured is the resistance of the SiB layer in parallel with the diffused layer below it [5]. A four point probe performed after the LTO will yield the true sheet resistance of the diffused layer.

This project involved the activation of the BN-975 planar sources and the use of them to deposit boron on device wafers. Specifically, the problem of removing the SiB layer that is created during the diffusion process was addressed. Two methods for removing this layer were compared and evaluated.
EXPERIMENT

A masking oxide of 3000-4000A was grown on three inch n-type (100) silicon wafers with resistivities of 7.5-12.5 cm. The wafers were coated with KTI-820 photoresist and exposed using a mask which allowed one half of each wafer to be completely diffused with boron and the other half to be patterned with diffused resistors, as shown in Figures 1 and 2.

Figure 1: Mask Pattern  
Figure 2: Device Pattern

The completely diffused half of each wafer provided areas for four point probe measurements and for ellipsometer measurements immediately following the planar source diffusion. After development, the silicon wafers were diffused at a temperature of 975 C for three different soak times of 15, 30 and 45 minutes.

The wafers were deglazed in 10:1 hydrofluoric acid for two to three minutes. The wafers then underwent either a LTO for 10, 20 or 30 minutes and an HF etch (18 wafers) or they were soaked for 30 minutes in nitric acid at 90 C (6 wafers). Four point probe measurements were taken prior to the masking oxide growth, after the deglazing and after the LTO or the nitric acid soak. Ellipsometer measurements were taken prior to and after the LTO. Junction depths were measured after the removal of the Si-B layer using the groove and stain technique.
RESULTS/DISCUSSION

For each diffusion time, four point probe measurements were taken prior to the SiB layer removal and after oxidation. Results of sheet resistance as a function of diffusion time can be seen in Figures 3 and 4. These graphs show three sigma variance and the uniformity of the deposition is evident.

Successful SiB removal for all three diffusion times was achieved with the LTO method. SiB removal is indicated by the rise in the measured sheet resistance after the HF etch. The ten minute LTO yielded the shortest HF etch time, but the SiB layer was not completely removed. Additional oxide had to be grown in order to completely oxidize the layer. The thirty minute LTO yielded the best initial results.

The nitric acid soak met with limited success, since only the SiB layer created during the shortest diffusion time was removed during the nitric acid soak. Additional soaking up to thirty minutes did not remove any significant amount of the SiB layer. The soak was discontinued at this point since it had failed to be an effective oxidation method. However, with additional work, a variation of the nitric acid soak may yield successful results. A higher soak temperature or a nitric acid soak followed by an HF etch may remove the SiB layer.
CONCLUSIONS

A preliminary process for boron diffusion and SiB removal for the BN-975 planar sources was achieved. The LTO method yielded the best results. However, preliminary data indicates that the nitric acid soak may work under certain conditions.

ACKNOWLEDGEMENTS

Scott Blondell for his continuous help with the diffusion furnaces and the pattern generator, Robert Pearson for his help in obtaining the activation and injection process procedures and Mike Jackson for obtaining supplies and offering suggestions. The BN-975 planar diffusion sources are products of Standard Oil Engineered Materials of Niagara Falls, NY and were donated to RIT.

REFERENCES


DESIGN OF A FOUR-BIT MICROPROCESSOR A.L.U. USING PMOS 10-μm METAL GATE TECHNOLOGY

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ABSTRACT

A four-bit ALU chip based on a metal gate PMOS process and 10-μm minimum geometries was designed. The operations performed by the ALU included ADD w/carry, SUBTRACT (2's complement), INCREMENT, DECREMENT, and the logic functions AND, OR, XOR, and COMPLEMENT. Due to space limitations no data or shift registers were included on the chip. PMOS NOR gates and inverters were used in the hardware implementation of the logic design. The ALU chip was laid out by using the ICE (Integrated Circuit Editor) design tool.

INTRODUCTION

The Arithmetic and Logic Unit (ALU) of a microprocessor consists of a combinational digital system that can perform basic mathematical and logical functions in parallel on each corresponding bit of data taken from an accumulator register and one other register, with the result fed back to the accumulator. This project consisted of the design of a 4-bit ALU chip using the existing RIT PMOS process, with 10-μm design rules and four masking levels (p-type diffusion, oxide, contact cuts, and metal gate). The Integrated Circuit Editor (ICE) was used to lay out the chip design. The chip size used was 5000um X 5000um. The hardware implementation of the ALU consisted of only PMOS NOR gates and inverters, with their combinations acting as universal logic gates representing the OR, AND, XOR, and COMPLEMENT functions of the logic design of the system. The ideal length to width ratios for the NOR gates and inverters were determined based on the SPICE analyses of Jim Taylor of RIT, who designed an RIT PMOS standard cell library[1].

Due to space limitations no data or shift registers were included in the chip design. This ALU was a strictly combinational circuit, with no clock signal used. All the data and previously decoded operation instructions must be input to the ALU pads. The connections to the outside world are power and ground, four data lines each for the two inputs, four lines for the resulting output, Cin and Cout (carry-in and carry-out) pads, and three 'select' lines carrying the specific instruction to be performed by the ALU. The Arithmetic and Logic Unit's functions include ADD, ADD w/carry, SUBTRACT (2's complement), INCREMENT, DECREMENT, and logic functions AND, OR, XOR, and COMPLEMENT. Major functional blocks included in the design were full adders, 2-1 and 4-1 line multiplexers, and a combinational circuit that expanded the capabilities of a full adder to include SUBTRACT, INCREMENT, and DECREMENT operations.
Figure 1 shows the pinout of the ALU designed in this project. It has four lines each for the data input by the accumulator (A) and one other register (B), and four lines for the output (F). The Cin line and the SELECT lines combine to specify the instruction set shown in Table 1. Line S2 is the 'mode select' that differentiates between the logic block and the arithmetic block of the circuit by using a 2-1 multiplexer for each bit in the circuit.

FIGURE 1: PINOUT OF THE ALU

<table>
<thead>
<tr>
<th>DATA</th>
<th>A0</th>
<th>S0</th>
<th>S1</th>
<th>S2</th>
<th>DATA OUT (F)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>A</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>F0</th>
<th>ARITHMETIC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>4-BIT</td>
<td></td>
<td></td>
<td>F1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ARITHMETIC</td>
<td></td>
<td></td>
<td>F2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOGIC</td>
<td></td>
<td></td>
<td>F3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UNIT</td>
<td></td>
<td></td>
<td>Cout</td>
</tr>
<tr>
<td>B</td>
<td>B1</td>
<td></td>
<td></td>
<td></td>
<td>VDD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GROUND</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TABLE 1: INSTRUCTION SET

<table>
<thead>
<tr>
<th>OPERATION</th>
<th>SELECT</th>
<th>OPERATION</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>S2 S1 S0 Cin</td>
<td></td>
<td>F= A+1</td>
<td>INCREMENT</td>
</tr>
<tr>
<td>0 0 0 0 0</td>
<td></td>
<td>F= A</td>
<td>TRANSFER A</td>
</tr>
<tr>
<td>0 0 0 1 0</td>
<td></td>
<td>F= A+B</td>
<td>ADD</td>
</tr>
<tr>
<td>0 0 1 1 0</td>
<td></td>
<td>F= A+B+1</td>
<td>ADD w/carry</td>
</tr>
<tr>
<td>0 1 0 0 0</td>
<td></td>
<td>F= A+B</td>
<td>COMPLEMENT</td>
</tr>
<tr>
<td>0 1 0 1 0</td>
<td></td>
<td>F= A-B</td>
<td>SUBTRACT</td>
</tr>
<tr>
<td>0 1 1 0 0</td>
<td></td>
<td>F= A</td>
<td>TRANSFER A</td>
</tr>
<tr>
<td>0 1 1 1 0</td>
<td></td>
<td>F= A</td>
<td>DECIMAL</td>
</tr>
<tr>
<td>1 0 0 0 0</td>
<td></td>
<td>F= A A</td>
<td>AND</td>
</tr>
<tr>
<td>1 0 0 1 0</td>
<td></td>
<td>F= A A</td>
<td>OR</td>
</tr>
<tr>
<td>1 1 0 0 0</td>
<td></td>
<td>F= A B</td>
<td>EXCLUSIVE OR</td>
</tr>
<tr>
<td>1 1 1 0 0</td>
<td></td>
<td>F= A B</td>
<td>COMPLEMENT</td>
</tr>
</tbody>
</table>

12
One of the four bits of the logic block is shown in Figure 2. The four logic functions are performed in parallel. Next the desired operation is selected by the 4-1 line multiplexer according to the S0 and S1 instructions as was shown in Table 1.

FIGURE 2: LOGIC BLOCK (ONE BIT)

One bit of the arithmetic block is shown in Figure 3. As with the logic block, the other three bits are identical. With the full adder, the Cout of one bit becomes the Cin of the next higher order bit. The full adder is used for parallel addition with carry. The combinational circuit placed in front of the full adder was designed to expand the full adder's capabilities to include the INCREMENT, DECREMENT, and SUBTRACT operations.

FIGURE 3: ARITHMETIC BLOCK

Combinational circuit

\[ Y = BS + BS \]
As shown in Figure 3, the inputs to the arithmetic block are \( A_1 \) and \( B_i \). The accumulator input \( (A_1) \) gets fed straight to the full adder. The \( B_i \) input gets manipulated prior to its entry to the full adder by the combinational circuit according to the logic table in Table 2. Conversion from \( B \) into \( Y \) follows the logic equation

\[
Y = BS + BS
\]

This equation was developed with a Karnaugh map based on the following logic table.

**TABLE 2: ARITHMETIC BLOCK LOGIC TABLE**

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1 S0 Cin B</td>
<td>Y = 0</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>Y = 0</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>Y = 0</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>Y = B</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>Y = B</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>Y = B</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>Y = B</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>Y = 1</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>Y = 1</td>
</tr>
</tbody>
</table>

If \( Y = 0 \), the output is either \( F = A \) or \( F = A + 1 \), depending on the set value of \( Cin \). If the combinational circuit leaves \( B \) unchanged, the regular full adder operation of ADD or ADD w/carry is the output. If \( Y \) becomes the complement of \( B \) and \( Cin \) is set to 1, 2's complement subtraction is the result. If \( Cin = 0 \) and all four bits of the second register are set to equal 1, the decrement operation results because \((1111)\) is equal to the 2's complement of \((0001)\).

The logic design of a full adder is shown in Figure 4. This is a standard circuit found in several textbooks, such as Ref. 3 and Ref. 4 in the bibliography.

**FIGURE 4: LOGIC DIAGRAM FOR FULL ADDER**
In the actual Integrated Circuit Editor (ICE) layout of the chip, only PMOS NOR gates and inverters were employed. Figure 5 shows how the OR, AND, and XOR gates of the logic design were implemented in hardware. An OR gate was made by inverting the output of a NOR gate. An AND gate was made by inverting both inputs of a NOR gate. Whenever two inverters occurred in series, they were cancelled out, as was done in the hardware representation of the exclusive-or gate in Figure 5.

**FIGURE 5: LOGIC IMPLEMENTATION: NOR GATES AND INVERTERS**

1. **OR:**
   
   ![OR diagram]

2. **AND:**
   
   ![AND diagram]

3. **XOR:**
   
   ![XOR diagram]

Figure 6 shows the hardware implementation of one bit of the ALU design. The arithmetic block shows the combinational circuit and the full adder, with sum S and Cout as outputs. The logic block shows the four logic functions that are fed to the 4-1 multiplexer, with an output of F. The S and F outputs along with mode select S2 would next go to a 2-1 line multiplexer not shown in Figure 6, and the final output would result.
FIGURE 6: ONE BIT OF THE ALU

FIGURE 7: 4 CHIP BUILDING BLOCKS

- Inverter
- 2-input NOR
- 4-input NOR
- 3-input NOR
RESULTS

Figure 7 shows the four types of gates used in the ICE layout: inverters and 2, 3, and 4-input NOR gates. The design was based on 10-um design rules and incorporated four mask levels: diffusion, oxide, contact cuts, and metal. All of the gates used PMOS enhancement drivers with active load transistors. The optimum length to width ratios for each gate were based on the SPICE analyses of Jim Taylor of RIT(2). These L/W ratios are listed below.

<table>
<thead>
<tr>
<th>LOAD DRIVER</th>
<th>LOAD</th>
<th>DRIVER</th>
</tr>
</thead>
<tbody>
<tr>
<td>INVERTER</td>
<td>L=50um W=10um</td>
<td>L=10um W=40um</td>
</tr>
<tr>
<td>2 input NOR</td>
<td>L=40um W=10um</td>
<td>L=10um W=20um</td>
</tr>
<tr>
<td>3 input NOR</td>
<td>L=50um W=10um</td>
<td>L=10um W=20um</td>
</tr>
<tr>
<td>4 input NOR</td>
<td>L=50um W=10um</td>
<td>L=10um W=20um</td>
</tr>
</tbody>
</table>

The exact ICE layout of the hardware design of Figure 6 is shown in Figure 8. This ICE plot shows the arithmetic and logic function blocks of one bit of the ALU. The dimensions of the one bit in Figure 8 are 1300um by 2400um. The four identical bits, one in each corner of the 5000um by 5000um chip, were brought together in the finished design found in the appendix. The pads were located in the center of the chip so that they would fit an automatic probe card arrangement for testing the logic of the chip after it was fabricated.

CONCLUSION

The design of the four bit ALU was completed. Built into the logic design was the capability to add on two shift registers to the arithmetic block. The design conforms to the current fabrication capabilities at RIT, including maskmaking, wafer processing, and testing.

REFERENCES

FIGURE 8
ONE BIT OF THE ALU
CMOS PLA LAYOUT GENERATION

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ABSTRACT

A dynamic AND - dynamic OR type of PLA was designed using a CMOS process and the layout was done on a CALMA system using 1.5um design rules. A PLA with 200 transistors was completed and can be used to perform desired logic functions.

INTRODUCTION

Programmable Logic Arrays have been used for many years as a means of customizing logic design. PLA's, as they are known, provide a flexible and efficient way of synthesizing arbitrary combinational functions in a regular structure. The circuit is based on a representation of Boolean functions as a set of sum-of-products terms. The AND plane produces the distinct product terms in the expressions; the OR plane collects these terms to produce the desired outputs. PLA's can be fabricated in either bipolar, using ECL gates or CMOS using both P and N type gates.

There are three distinct types of PLA's that can be implemented and used for different designs, depending on the size of the PLA, the desired speed, and the timing sequence. They are the dynamic-dynamic, the dynamic-static, and the static-dynamic. The two terms are descriptive of the two separate planes, AND-OR, that provide the logic AND function or the logic OR function. Dynamic means that the plane is always performing some type of function while static means it performs a function only on specified clock pulses.

Figure 1 shows the block diagram for a typical PLA. The chart on the next page shows some typical uses, timing, sizes and current consumption comparison of the three types of PLA's. The timing diagrams are shown in Figure 2 (2). As can be seen the uses of the PLA would be according to the design specifications for the outputs being valid or the inputs being stable.

The main concept of a static plane is that the inputs/outputs are sampled while the pull-up transistors are
<table>
<thead>
<tr>
<th>Comparison Description</th>
<th>Dynamic '86' Dynamic '91'</th>
<th>Dynamic '86' Static '81'</th>
<th>Static '81' Dynamic '91'</th>
</tr>
</thead>
<tbody>
<tr>
<td>USES</td>
<td>Sample inputs at one clock phase produce outputs in same phase after clock cycle</td>
<td>Sample input @ one clock phase, produce outputs in the following phase</td>
<td>Sample input @ one clock phase; produce outputs in the following phase</td>
</tr>
<tr>
<td>When planes are operating</td>
<td>All planes are on one phase, 0 or the other phase.</td>
<td>Both planes are on the evaluation phase.</td>
<td>During 1st phase, where inputs sampled, miniters are in phase 0 or 1, or static phase on 0 or operating phase.</td>
</tr>
<tr>
<td>Size of PLA</td>
<td>Many miniters, inputs and outputs</td>
<td>Limited max. number of miniters, inputs, outputs</td>
<td>Many miniters &amp; devices inputs used one every one sampling phase.</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>Low, due to no static plane</td>
<td>High due to static operation of 0th.</td>
<td>High due to static operation of 0th.</td>
</tr>
<tr>
<td>Buffers b/t planes</td>
<td>Clocks buffers sampling</td>
<td>NONE</td>
<td>Two Inverters</td>
</tr>
<tr>
<td>Output Buffers</td>
<td>Same as b/t planes</td>
<td>Junctioned CMOS structure</td>
<td>Same as D.D.</td>
</tr>
<tr>
<td>Sizing of '00' plane</td>
<td>Increase length of outputs metal line</td>
<td>Increase width of source diffuser</td>
<td>Increase to b/t</td>
</tr>
<tr>
<td>Placement of precharge for dynamic plane</td>
<td>Between planes with input buffers to 00</td>
<td>OUTSIDE of '00' plane</td>
<td>LOWER SIDE OF '00'</td>
</tr>
</tbody>
</table>

**TABLE I: COMPARISON OF THREE PLA'S**
disconnected. This means that every line that is a logic "1" discharges and every line that is a logic "0" is floating. The main problem with this is the pull-ups try to charge all lines, including the lines being pulled down. If the pull-down transistors are not strong enough, noise margin degrades. If the pull-ups are not strong enough then the charge of the output line is slow and if the pull-ups are too strong the circuit will consume a lot of power. One possible solution to this problem is to make the pull-up transistor with a W/L ratio of 1.

![Block Diagram of PLA](image)

FIGURE 1: BLOCK DIAGRAM OF PLA

The focus of this project was on layout of the cells for the PLA utilizing the CALMA system here at RIT. By making cells, others can customize the PLA to perform a desired logic function. The dynamic-dynamic PLA was chosen because of the ease of the clocking scheme along with its interesting nature. Defining the PLA, including the schematic of the cells used, the number of inputs and outputs, and also the clocking scheme was a part of this project. Cell explosion schematics are shown in Figures 3 and 4 (3). Figure 3 is the cell explosion for the input buffer and Figure 4 is the output buffer.

The PLA designed was for a CMOS double-metal process using the refractory-polysilicon techniques. The refractory-poly process uses metal placed on top of the polysilicon to reduce the resistance. This also insures that the double-metal process is
used. The double-level metal was used because of its low power consumption and short path delays.

The first step in the design process is developing the device at the schematic level. The majority of schematic capture tools available today require a designer to start with at least a behavioral description of the circuit. The PLA description for this design was arbitrary and was for demonstration purposes only. This is true because the purpose of this project was to create the standard cells necessary to help others redesign the PLA for a specific function. Assuming the device to be fully custom, the next step is to layout the physical geometries for each masking level associated with the transistors in the schematic. Here is where the CMOS, double level metal, polysilicon gate process was chosen.

DESIGN

PLA's are essentially uncommitted logic gates where the user determines the final logic configuration of the device. The basic programmable array is the AND-OR logic in the familiar sum-of-products (SOP) representation. A conventional schematic representation is shown in Figure 5. Its programmable logic equivalent is shown in Figure 6 (4).

![FIGURE 5: PLA SCHEMATIC REPRESENTATION](image)

One reason for using the SOP expressions is their straightforward conversion to very simple logic gates. In their purest and simplest form they go into two level networks which are networks for which the longest path through which a signal must pass is two gates long (5).

Today programmable logic typically implements from 4 to 20 SSI and MSI logic devices. This allows a reduction of size for a system as well as an increase in logic power. Also with the use of programmable logic, the designer is not limited to standard off the shelf parts and, therefore, can use non-standard structures. Another reason for its use is that designers can compress multiple levels of logic into a two level AND-OR structure, thus simplifying the design and in many cases obtaining speed and/or power advantages (6).
The PLA for this project was designed for the CMOS double level metal process. The design rules used are for the 1.5um polysilicon lines, and the masking steps for the process are listed below in Table II. A cross section of the process can be seen in Figure 7 (7). The reason for using double level metal is because if the PLA gets very large, to cut down on the resistance of the poly gates, metal two can be tapped into the poly and it is like having two resistors in parallel.

**Table II Masking Steps for Double Level CMOS**

1. N-well
2. Field Oxide
3. N-well protection
4. Polysilicon
5. N+ regions
6. P+ regions
7. Contact cuts
8. Metal One
9. Via Cuts
10. Metal Two

The schematics, shown in Figures 5 and 6, were drawn by hand since logic simulation had been done already in November 1987 while on co-op at National Semiconductor in Santa Clara, the program used for simulation was SPLA (8). The reason for simulation was part of the work that was being done in studying PLA's in general. The next step in the design was layout. This was done on the CALMA system in the CAD/CAM lab in the microelectronics building at RIT. The library name used for this project and where the cells can be found is called CMOSCDB.
All cells have been drawn, schematics have been constructed and connections to form the PLA has been completed. The PLA is drawn such that it is rectangular. The pad arrangement has not been set because of the way the PLA can be rotated to provide extra space. The number of transistors is approximately 200.

CONCLUSIONS

A dynamic - dynamic PLA has been done and the layout is completed. It can now be programmed to do any logic function that is desired. The cells used can be modified to provide the best implementation for that desired function.

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A METHOD TO IMPROVE STEP COVERAGE OF CONVENTIONAL POSITIVE WORKING PHOTORESIST

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ABSTRACT

Positive resist coated wafers were immersed in a dilute alkaline base developer, such as 5:1 AZ351, for a short period of time prior to exposure. The purpose of this sequence was to improve development rate discrimination of conventional positive photoresist, which will enhance step coverage. A SEM comparison of a 5 micron line/space pair pattern of AZ1350 resist on a 1.2 micron step, showed this pre-treatment yields improved step coverage compared to a conventional process.

INTRODUCTION

Currently with positive working photoresist, processing difficulties arise transferring an optical image onto a wafer surface with large topographic features (greater than one micron). Multilayer resist schemes have been proposed with the purpose of resolving these problems, but with added expense and technical complexity as well [1,2].

The resist coverage problem can be seen by looking at the cross sectional profile of applied resist, as seen in Figure 1a. During application, the resist spreads out uniformly across the wafer, and areas with large topographic features will have a thinner resist coating. With any resist, a 20:1 development discrimination between the exposed and unexposed areas is desirable [3]. For positive resist, this means the unexposed areas will be reduced an amount equal to one twentieth of the exposed areas when placed in developer. The area of concern is the unexposed region with the thinnest resist coating, since when placed in developer any thickness loss may be significant, as seen in Figure 1b.

FIGURE 1a: Unexposed Resist          FIGURE 1b: Unexposed Resist

Profile of resist pre-development

Profile of resist post-development
For a nominal initial resist thickness of 1.4 microns, and topographic features on the wafer being in the order of 1.2 microns, the resist thickness coverage will only be 2000 angstroms on top of the tallest features. The development needed to clear a resist thickness of 1.4 microns, results in a thickness loss of 700 angstroms in the unexposed areas using a 20:1 development rate discrimination. In the valleys this is only a 5 percent thickness loss, but on top of the step this amounts to a 35 percent thickness loss. A thinning of resist can lead to masking problems and in extreme cases, there will be a discontinuity over the step.

In order to increase the development rate discrimination, which will reduce the thickness loss in the unexposed areas thus increasing the step coverage, a simple pre-exposure treatment has been proposed [4]. It involves the immersion of a photoresist coated wafer, in a dilute alkaline base developer, such as 5:1 AZ351, for a short time, typically between 15 and 30 seconds prior to exposure.

The theory of the pre-exposure treatment is based on the chemistry which takes place during development. Conventional positive working resists consist of two key components, novolak and naphthoquinone diazide (NQD), as seen in Figure 2. The novolak acts as the binder which controls the resist coating quality. The NQD is the photoactive component which is responsible for the change in solubility of the resist upon exposure.

The exposed areas of the resist undergo a transformation of being a base insoluble sensitizer, to a base soluble acid during exposure [3]. When placed in developer the exposed areas are easily dissolved. A synopsis of the chemistry is shown in Figure 3. The unexposed areas, not altered, still consist of novolak and NQD. Novolak by itself is very soluble in developer and approximately 4000 angstroms per minute can be removed [3]. A slower rate of dissolution in the unexposed areas is believed to be a result of a base induced coupling between the novolak and the NQD. The crosslinking reaction is shown in Figure 4.
In conventional developing it is believed this coupling reaction does not happen to completion, due to the developer being amply used in developing the exposed resist. Thus fresh developer is not locally available to the unexposed areas so the coupling can not effectively take place. The pre-treatment allows adequate time for the crosslinking to take place on the surface, thus reducing the solubility of the resist at the surface, while the bulk still retains its photoactive characteristic. The result is increased development discrimination, which stated earlier, will preserve the resist coating on top of large topographies.

This study is an investigation on the effect of a pre-exposure treatment on step coverage. KTI 820 and Hoechst AZ1350 resists were examined.

EXPERIMENT

Large topographies were created by thermally growing a 1.2 micron layer of silicon dioxide, masking a 5 micron line/space pattern and utilizing a wet etch to create the step. After a plasma ash and subsequent clean the wafers were ready for further processing.

The wafers were primed with HMDS and coated with Hoechst AZ1350 photoresist with a nominal thickness of about 1.4 microns. A prebaked at 90 degrees celsius was carried out for 30 minutes in a convection oven. At this point the wafers were divided into two groups. One group of wafers were immersed in 5:1 AZ351 developer for a time varying between 15 and 30 seconds, rinsed in DI water for 2 minutes, air dried and then were selectively exposed. The other group went directly to exposure.

A Kasper contact mask aligner was used for exposure, which emits strongly at the G,H, and I lines of the ultraviolet light spectrum. The wafers were exposed using a 5 micron line/space pair mask, which was aligned perpendicularly to the oxide steps. The wafers were developed in 5:1 AZ351 developer for 60 seconds. The exposures needed were approximately 90 mJ/cm² for the pre-treated wafers, and 80 mJ/cm² for the standard group. A scanning electron microscope was used to evaluate the resulting profiles.

A similar procedure was done with KTI 820 coated wafers, but
processing difficulties precluded the completion of this study.

RESULTS/DISCUSSION

The step coverage of the conventionally processed wafers compared to that of the pre-treated wafers can be visually examined in Figures 5 and 6 respectively. These are scanning electron micrographs, taken at a 5000 magnification. The pre-treated wafer, which utilized a 30 second immersion time, shows a better coverage over the step.

The processing difficulties incurred with KTI 820 resist were two fold. First, there was an initial adhesion problem with the pre-treated wafers. Secondly, adequate time should be allotted for excess HMDS to evaporate or this could lead to process deviations. In this case the resist sensitivity fluctuate depending on the amount of HMDS applied. It should also be noted if KTI 820 were used, the viscosity would have to be adjusted so that the difference in resist thickness to oxide height is in the order of 2500 angstroms or less so that a noticeable difference in step coverage can be more readily be seen.

CONCLUSIONS

A pre-exposure treatment using a dilute alkaline base, such as AZ351, was shown to improve the step coverage in AZ1350 resist. The enhanced step coverage is believed to be a result of increased development rate discrimination between exposed and unexposed areas of the resist.

ACKNOWLEDGEMENTS

A special thanks to Scott Blondell and Ronald Quiett for their help in acquiring SEM pictures; to Kathy Hesler for her help in obtaining resist information, and helpful assistance; and to Mike Jackson for his instructive feedback on the project.

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FIGURE 5: Resist processed in a standard manner

FIGURE 6: Resist processed with a pretreatment
ABSTRACT

This project was a preliminary study of an aluminum/dielectric/aluminum multilayer metallization scheme. Polyimide and spin on glass were compared using high frequency CV analysis on fabricated capacitors. The simple processing involved showed that good crack-free and adhesive films could be formed with both materials although the polyimide was the more ideal CV characteristics. Test masks were generated to measure via resistance and dielectric breakdown in a bi-level structure. The Spin on Glass processing was unsuccessful because of underetching of vias. The polyimide processing was successful displaying good breakdown characteristics but high via resistances.

INTRODUCTION

The new VLSI (very large scale integration) era is requiring longer interconnect paths as the density and complexity of the circuits increase [1]. In circuits of several hundred transistors single level metallization becomes severely limiting.

The necessity for multilevel metallization is clear if we consider the circuit performance characteristics. The effect of this increase is best described by the equation [1]:

\[
RC = \frac{(R_sL^2E_{ox})}{X_{ox}}
\]

where, \(R_s\) is the sheet resistivity of the connection, \(L\) is the length of the connection, \(E_{ox}\) is the permittivity of the dielectric and \(X_{ox}\) is the thickness of dielectric. It can be seen from the above equation that time delays are due to a square relation of the length of interconnects becoming an increasingly limiting factor in performance.

The traditional dielectric for the purposes previously stated has been some type of CVD oxide [2]. Recently, cost and reduced complexity in processing has prompted study of alternative dielectrics. It is the previous work of Robert Newcomb [3], Christopher Knaus [4] and Eric Westerhoff [5] that has shown that both polyimide and spin on glass can be used as an intermediate dielectric layer. This further research is intended to extend their work so that these methods may become workable and comparable. In the past incomplete via cleanout, cracking, and adhesion have been the limiting problems. A modified curing
method will be used to attempt to solve the cracking and adhesion problems. It shall also be necessary to determine the best method for via cleanout in the multilevel test scheme.

The comparison of the spin on glass and polyimide dielectrics can begin by determining the capacitor voltage characteristics of the dielectrics in a standard capacitor structure. In current process technology, capacitance-voltage measurements are standard and required in determining dielectric properties [6]. The analysis to be performed can be utilized to determine oxide capacitance, threshold voltage, and flatband voltage.

One of the important considerations of the multilevel process is the dielectric strength of the intermediate layer. Each layer must be able to simultaneously hold any necessary voltage with no fear of parasitic conduction through the dielectric. This can be accomplished by simply overlaying the two metal layers thereby forming a capacitor structure. Figure 1 is an example of this dielectric breakdown structure. The dielectric breakdown being measured by applying a voltage on one metal with respect to the other until a predetermined current density is measured.

![Figure 1: Cross section of breakdown structure [3].](image)

The final test structures which are presented in Appendix A, the ICE (Integrated Circuit Editor) layout, contains six different area capacitors on a die where four wafers will be processed at four different dielectric thickness's.

Another equally important characteristic is the proper formation of vias. Geometric considerations cause via resistance to increase with decreasing via size. This via resistance can adversely effect the time delay of circuits. The expected low resistance of aluminum will necessitate the need for long via chains. This method simply involves dividing the measured resistance by the total number of vias to determine the individual via resistance. The basic structure of the via chains is presented in Figure 2.
Figure 2: Cross section of via chain structure [3].

It shall be necessary to compare via resistance as a function of dielectric thickness and via size. For these reasons wafers of different thickness (different spin speeds) dielectrics must be prepared where each contains the varying sized via chains.

A thick thermal oxide (over 10,000 angstroms) will be grown prior to the first metal evaporation, isolating the first level metal from the substrate making measurements of both dielectric breakdown and via resistance easier. This however will make ellipsometry measurement, to determine the dielectric thickness impossible. Fortunately however, the dielectric breakdown structures will have a measureable capacitance which when combined with the calculated capacitance voltage values of permittivity (Eox) will allow us to indirectly determine the thickness's of the test structures.

EXPERIMENTAL

The process sequence shall be presented in abbreviated form, where the full description is left for appendix B. This sequence was to first make capacitors to take CV measurements, it could then be seen if in a simply process, crack-free films with good adhesion dielectric properties were possible using these materials. The CV plots are presented in appendix C.

Using the generated test masks (Appendix A) both polyimide and spin on glass bi-level structures could be processed for varying thickness's of the dielectrics.
Four three inch polyimide coated wafers were processed at four different spin speeds given below in order to obtain four different thicknesses of the dielectric:

<table>
<thead>
<tr>
<th>Spin speeds (RPM's)</th>
<th>expected film thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>greater than 1.0 micrometers</td>
</tr>
<tr>
<td>3000</td>
<td>greater than 1.0 micrometers</td>
</tr>
<tr>
<td>5000</td>
<td>approx. 1.0 micrometer</td>
</tr>
<tr>
<td>7000</td>
<td>less than 1.0 micrometers</td>
</tr>
</tbody>
</table>

Also processed were four, three inch, spin on glass wafers. Each received four different spin speeds, given below, in order to obtain four different thicknesses of the dielectric.

<table>
<thead>
<tr>
<th>Spin speeds (RPM's)</th>
<th>expected film thickness (angstroms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>2000</td>
</tr>
<tr>
<td>2000</td>
<td>1680</td>
</tr>
<tr>
<td>3000</td>
<td>1350</td>
</tr>
<tr>
<td>4000</td>
<td>1150</td>
</tr>
</tbody>
</table>

Please refer to references [7] and [8] for information regarding the choice of process cure times and temperatures.

The conclusion of this experimental portion was the measurement of the via resistance and dielectric breakdown characteristics of the materials. The HP-parameter analyser was used in both cases with the plots presented in appendix D.

RESULTS

The CV plot results presented in appendix C show that the Spin on glass had extreme surface state problems prior to sinter. Ten minutes at 400 C seemed to improve the dielectric to aluminum contact sufficiently to alleviate this problem. The polyimide did not show the extreme pre-sinter surface states but seemed to also improve post-sinter. Both the polyimide and spin on glass CV curves are very positively flat band shifted. The dielectrics are clearly not ideal situations but demonstrated sufficiently good process and high frequency CV characteristics to warrant continuation of the experiment.

The final test structures were more successfully processed in the case of the polyimide dielectric compared to the spin on glass. The spin on glass was severely underetched during the HF via etch. The high temperature bake (400 C) intended to improve film quality (prevent cracking) caused an apparent densification of the film which increased expected etch rates in the HF. For this reason subsequent data of the bi-level metal structure is presented for the case of the polyimide only.

In both cases however it was not possible to measure the thickness of the dielectrics used in the capacitors with ellipsometry techniques. This would be necessary to determine the permittivity of the materials. The lack of these permittivity
values prevented the determination of thicknesses of the dielectrics in the test structures. This is the reason why subsequent data is presented with respect to spin speeds and not thickness'.

The breakdown voltages presented in Table 1 were determined by choosing a current density of $16\text{nA}/\text{um}^2$ where this value must be calculated from the relation of equation 4.

$$J = \frac{I}{A} \quad (4)$$

where: $J$=current density
$I$=current
$A$=cross sectional area of capacitor

The $I$-$V$ characteristics of the data for Table 2 is presented in appendix D.

**TABLE 1**

<table>
<thead>
<tr>
<th>Capacitor area (um$^2$)</th>
<th>Breakdown Voltages (Volts)</th>
<th>Spin speeds</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40 $\times$ 300</td>
<td>26.64</td>
<td>25.50</td>
</tr>
<tr>
<td></td>
<td>21.08</td>
<td>16.32</td>
</tr>
<tr>
<td></td>
<td>26.00</td>
<td>13.00</td>
</tr>
</tbody>
</table>

The data of Table 1 shows the expected trend of decreasing breakdown voltage for decreasing film thickness (increasing spin speeds). Graphs 1 of the 15$\times$300 um structure is representative of the relation discussed.

Graph 1: Breakdown voltage vs. dielectric spin speed

Table 2 contains measured resistances of selected areas of the four via chains for three different spin speeds.
TABLE 2

<table>
<thead>
<tr>
<th>via dimension (um)</th>
<th>individual via resistance in ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>spin speeds</td>
</tr>
<tr>
<td>30</td>
<td>3000 5000 7000</td>
</tr>
<tr>
<td>20</td>
<td>9.50e9 10.5e9 7.44e9</td>
</tr>
<tr>
<td>10</td>
<td>4.20e9 4.26e9 3.04e9</td>
</tr>
<tr>
<td>5</td>
<td>5.63e9 4.40e9 3.43e9</td>
</tr>
</tbody>
</table>

The 30 and 20 micrometer via resistance was measured using 12 of the 114 via chain (the resultant resistance plots presented in appendix B) and dividing the total measured resistance by 12. Similarly the 10 and 5 um via resistance was measured using 30 of the 600 via chain (the resultant resistance plots presented in appendix B) and dividing the total measured resistance by 30.

Table 2 demonstrates the expected trend for decreasing via size of increasing via resistance for each measured pair (5 compared to 10 um and 20 compared to 30 um). Added to this is the fact that no breakdown is apparent in the I-V characteristics from which the resistance was determined. Examining table 2 it is seen that although the vias appeared cleared when visually inspected during processing an aluminum oxide must have formed (prior to the evaporation of the second level metal) which resulted in the unduly high resistances.

It should be also noted that the working masks can only be aligned to certain die areas because of problems encountered with the GCA photo-repeater. The photo-repeater produced differing spaces between die. Therefore die were properly aligned must be searched for on the wafer.

CONCLUSIONS

The CV plot data demonstrated the feasibility of both spin on glass and polyimide as dielectric materials. Subsequent processing of test structures demonstrated the polyimide as a viable bi-metal dielectric. When using properly dated materials, a sufficiently high curing method (such as to prevent cracking), and an adhesion promoter (VM651), both good adhesion and a crack-free surface was obtained. Further work using these materials should include:

a) Examining etch rates of spin on glass to eliminate undercutting during the via etch.

b) An HF etch prior to second level metal evaporation to remove a suspected oxide formed over the first level aluminum.

c) Studying the thickness vs. spin speeds of both dielectrics discussed in this paper.
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AUTOMATED DESIGN RULE CHECKING

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ABSTRACT

A Fortran Coded Design Rule Checker was written to analyze the output file of the RIT Integrated Circuit Editor (ICE) program. The design rules for the RIT 4LEVELPMOS process have been successfully implemented for a die size of 1900 by 1900 square micrometers.

INTRODUCTION

When allowing for the design of Integrated Circuits (ICs) that are virtually unlimited in scope and creativity, a means of automated Design Rule Checking (DRC) becomes a necessity. The Integrated Circuit is made up of individual layers, such as Diffusion, Thin Oxide, Contact Cuts, and Metal. These layers combine together to form electrical circuits. A Design Rule Checker is a computer program that analyzes the layers, individually and together, to see if there are any design flaws, such as metal lines placed too close together, or contact cuts being designed too small. In keeping pace with the growing field of IC fabrication, a Design Rule Checker will need to be versatile in handling different technologies, increased layout complexity, and unusual layout designs.

The design rules that are checked are a combination of processing constraints and circuit requirements, that if violated, would result in non-functioning or defective ICs. Spacing and width checks are two examples of processing constraints. Circuit requirements would incorporate checks like: are there more than one output leads connected together, do all the power leads connect to the power rails, and are there too many input leads being driven by a single output lead (fanout).

Four basic methods of Design Rule Checking have been developed and published. They are: Corner Base, Expanding Polygon, Deterministic Finite State Automata, and Raster Scan method. The Corner Base method performs the checks on the corners of each structure (or box). At the corner, the program examines the four quadrants around the corner, and based on the presence or absence of the different layers, an error message is given. The Expanding Polygon method digitizes the individual structures into polygons. By performing logical operations and expansion/shrink steps on the layers with these polygons, error messages are sent when the polygons overlap each other. The third method, Deterministic Finite State Automata, scans a small structure through a rasterized file. A numerical state, possible an error state, is assigned to the center location. The value is determined by a "Look-up" table that is dependent
upon the presence or absence of different layers in the other locations of the scanning structure. The fourth method was actually the first method developed. The Raster Scan method rasterizes the individual layers into separate binary arrays. Then a square window (the size of the window depending upon the geometry of the rule being tested) is scanned throughout the individual arrays. The patterns of 1's and 0's, within the window, are compared to stored patterns within the program. Certain patterns flag errors, while other patterns indicate that there is nothing wrong within the window. For a more detailed explanation of any of the above methods, see references 1 through 3.

In this project, a Design Rule Checker was developed to analyze IC designs created using the RIT developed, Integrated Circuit Editor (ICE) program. The RIT 4LEVELPMOS Process was chosen for its simplicity (four processing layers: Contact Cut, Diffusion, Metal, and Thin Oxide).

The user generates his/her design in ICE, by interweaving boxes of the different processing layers together. ICE is capable of making boxes that are placed in either the X direction or the Y direction. Diagonal boxes, curves, and circles can not be designed by using ICE. When the design is complete, a CIF file is generated. (CIF stands for Caltech Intermediate Form.) From this CIF file, a raster file is generated by another computer program, called RASTER (developed by Thomas Kucmierz, another 5th Year Microelectronic Engineering Student). The RASTER program reads in the CIF file and converts the boxes into pixel elements. These elements compose a two dimensional array. Upon completion of reading the CIF file, the array is written to an output file, which is the Raster file. Each element in the raster file represents a defined amount of space on the actual IC surface. For example, the first version of these programs are breaking an entire 1900 micrometer by 1900 micrometer IC into 190 by 190 array elements, making each element representing ten square micrometers. Each element contains information of every layer that is present within that location. (The first page of the appendix has a 40 by 40 portion of an input RASTER file.)

Design Rules for version (1.0) of the DRC are:

1.) All boxes can not be smaller than 10 micrometers.
2.) All boxes must be on 10 micrometer increments of each other.
3.) Width of Diffusion boxes cannot be smaller than 30 micrometers. Resistors are often designed smaller than 30 micrometer widths. This program is a checker, so the results can be ignored since it can not interfere with ICE in generating the output files.
4.) Minimum spacing between Diffusion boxes is 10 micrometers.
5.) Width of Thin Oxide boxes cannot be smaller than 10 micrometers.
6.) Width of Metal boxes cannot be smaller than
30 micrometers.

7.) Minimum spacing between Metal boxes is 10 micrometers.

8.) Contact Cuts (CC) are to have at least 10 micrometers of: Diffusion, Thin Oxide, and Metal surrounding the Contact Cut. (For example, you have a 20 micrometer Contact Cut box. There would need to be a Diffusion box of at least 40 micrometers under neath the CC, a Thin Oxide box of at least 40 micrometers the CC goes through, and a Metal box of at least 40 micrometers to cover the CC with.)

9.) For transistors, there must be at least 10 micrometers of Thin Oxide Indentation over the Diffusion area to allow for misalignment of the Thin Oxide layer. If there is no margin of error for the Thin Oxide, then all the transistors, unless perfectly aligned, would have incomplete gate regions and would not function.

* Note: These rules may seem to be a re-instatement of the first rule, but they are presented since they may be changed in future changes of the Design Rules, that do not change the over-all minimum width rule.

The method employed within this DRC is based on the Raster Scan, except that instead of a window check, there is a "physical" check. The program checks one design rule at a time. It scans the binary array for the presence of the layer in question. At each spot the program scans the physical area around the spot, to see if the rule was violated. If so, an Error array keeps track of the error number that is associated with the design rule being checked.

The output of this DRC is a multi-page, partitioning, of the Error output array and the transistor location array. Included are two tables listing the error code messages and a description of all the transistors. (See appendix for examples of the four output items: Error Array, Error Code table, Transistor Description table, and Transistor Location Array.)

EXPERIMENT

Figure 1 indicates the steps the program executes. There are three subroutines: WIDTHC, SPACE, and SURROU. WIDTHC checks the width of each box. It has two parameters passed into it, the layer to be checked and the minimum width length. SPACE checks the spacing between boxes. It has two parameters, the layer to be checked and the minimum spacing between the boxes. SURROU checks to see there is adequate surround boxes around the contact cuts. The two parameters passed into it are the layer to check for the surround around, and the minimum amount of surround needed.
READ in RASTER File

Partition Layers into different arrays

Call WIDTHC (Diffusion, 30 microns)
Call SPACE (Diffusion, 10 microns)
Call WIDTHC (Metal, 30 microns)
Call SPACE (Metal, 10 microns)
Call WIDTHC (Thin Oxide, 30 microns)
Call SURROU (Metal, 10 microns)
Call SURROU (Oxide, 10 microns)
Call SURROU (Diffusion, 10 microns)

Locate all gate regions and assign values to them

Group all the same gate regions into one transistor number

Find opposite ends of each transistor region, then determine transistor parameters:
  X-Y location, Length, Width, Direction

Check Oxide Indentation over Diffusion Rule

Write out the Output file

Figure 1

RESULTS & DISCUSSION

On a Sunday evening, with twenty two users on a VAX-8650 mainframe, this DRC took twenty seconds elapse time, with eleven CPU seconds. (The CPU time is the actual amount of time the computer devotes it’s attention to a given task.) The input raster file was seventy two blocks of memory. The output file was two hundred seventeen blocks of memory. (Each block contains five hundred twelve bytes, which is equivalent to five hundred and twelve letters of the alphabet, that is 512 letter A’s in a line.) The actual, executable machine language code took 427,000 bytes of memory. The VAX-8650 allows for over two billion bytes per task. This indicates that larger arrays (therefore larger IC’s) can be analyzed.
It has been suggested that the program should generate an error output file that would be formatted like a CIF file, and would contain boxes around the areas where Errors were found. This would allow the user to go back into ICE, recall his/her original work, then overlay this new CIF file over his/her original design, to easily locate where the errors are. Implementation of this process would require a complete understanding of the CIF format, and an understanding of how this DRC works, but should not be difficult to do.

If this DRC is going to be used on totally different technologies, such as NMOS or CMOS, it is recommended to make copies of the original source code and modify the copies to the technology needs. Trying to incorporate all the different technologies into one program would make the program hard to understand and would make the program very big with many duplicate parts.

CONCLUSIONS

The developed DRC worked. It was written to make future expansion easy to implement. Additional layers can be tested by adding new Error messages for the layers, and subroutine calls to check the new layers.

ACKNOWLEDGMENTS

Robert Pearson for his personal time he spent when explaining and defining the needs of the Microelectronic Engineering Department.

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DETERMINATION OF MINORITY CARRIER LIFETIMES
USING THE CAPACITANCE-TIME TECHNIQUE

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Rochester Institute of Technology

ABSTRACT

Capacitance-Time (C-T) plots were generated using a Micromanipulator model 410 CV system with a Yokogawa 3022 A4 X-Y recorder (with time base activated). MOS capacitors were pulsed instantaneously from accumulation into deep-depletion. The capacitance was then recorded as the samples relaxed back to their equilibrium state (Cmin). The method used to analyze the C-T data was known as a ZERBST analysis. A FORTRAN program was created to handle the differentiating required for the ZERBST plot. Preliminary results indicate that this set-up will accurately determine minority carrier lifetimes.

INTRODUCTION

Capacitance-Time (C-T) methods can be an extremely useful tool in the monitoring of process flows in any modern microelectronics facility. Thru the analysis of C-T plots, one can determine the minority carrier lifetimes of given MOS structures. The monitoring of lifetimes will indicate if a given process is going astray.

C-T measurements can be obtained using a simple MOS capacitor. The depletion region of a capacitor can be forced into a non-equilibrium condition by pulsing the capacitor from accumulation to inversion by using a square wave as a toggle voltage. This rapid change in bias causes a non-equilibrium to occur in the depletion region of the capacitor. It is this very fact that allows one to record the C-T response of a structure. One is not allowing the minority carriers to be generated fast enough to offset the rapidly changing bias on the gate. In time, the capacitor will relax to its equilibrium value (Cmin). The recording of this event is a C-T plot, as shown below (1).

![Figure 1: Typical C-T Plot](image-url)
The minority carrier lifetime ($T_g$) of a device can be defined as "the average time an excess minority carrier will live in a sea of majority carriers." (2). Zerbst proposed a method of evaluating the C-T response so as to determine $T_g$. It is worth noting that Zerbst's analysis is the most widely accepted C-T analyzation technique used today. Zerbst's derivation is given below, as outlined in Nicollian and Brews' MOS PHYSICS and TECHNOLOGY (3).

The following equation takes into account the total voltage drop of a capacitor in the deep-depletion mode of operation. By Gauss's law:

$$C_{ox}(V_g - \psi(T)) = q(N_i(T) + \int_0^W Nb(x)dx)$$  \hspace{1cm} (1)

where:

- $C_{ox}$ = Oxide Capacitance
- $V_g$ = Gate Voltage
- $\psi(T)$ = Instantaneous band bending
- $N_i(T)$ = Instantaneous inversion layer carrier density
- $Nb(x)$ = Dopant density at position $x$
- $W(T)$ = Instantaneous value of depletion layer width

Differentiating Equation 1 with respect to time yields:

$$\frac{dN_i}{dT} = -C_{ox}\frac{d\psi}{dT} - Nb(W(T))\frac{dW}{dT}$$  \hspace{1cm} (2)

The depletion width at a given capacitance $C(T)$ is given by:

$$W(T) = \varepsilon_s i(1/C(T) - 1/C_{ox})$$  \hspace{1cm} (3)

Zerbst related the surface generation velocity ($S$) to $W$ by neglecting the voltage drop across the inversion layer:

$$\psi(T) = \frac{q}{\varepsilon_s} \int W(T)dx$$  \hspace{1cm} (4)

Differentiating Equation 4 yields:

$$\frac{d\psi(T)}{dT} = \frac{qW(T)Nb(W(T))dW}{\varepsilon_s}$$  \hspace{1cm} (5)

Combining Equations 2, 3, and 5 yields:

$$\frac{dN_i}{dT} = -\frac{Nb(W)\varepsilon_s}{2C_{ox}} d/dT(C_{ox}/C(T))^2$$  \hspace{1cm} (6)

Equation 6 is Zerbst's relation between the rate of change on the inversion layer carrier density and the rate of change of depletion layer width. Zerbst then related the generation in the bulk and surface to the inversion layer charge density as:

$$\frac{dN_i}{dT} = \frac{Ni}{T_g} (W(T) - W(T=\infty)) + NiS$$  \hspace{1cm} (7)

where: $T_g$ = minority carrier lifetime
Substitute Equations 3 and 6 into 7 yields:

**ZERBST Equation:**

\[
\frac{d}{dT} \left( \frac{C_{ox}/C(T)}{C_{min}} \right)^2 = \frac{2N_i}{N_b} \left( \frac{C_{ox}}{C_{min}} (C_{min}/C(T) - 1) \right) + \frac{\varepsilon_{ox} S}{\varepsilon_{Si} T_{ox}} \frac{1}{T_{ox}}
\]

A Zerbst plot can now be generated by plotting:

\[ \frac{d}{dT} \left( \frac{C_{ox}/C(T)}{C_{min}/C(T) - 1} \right)^2 \text{ VS } \frac{C_{min}/C(T)}{C_{min}/C(T) - 1} \]

This plot will have a slope \( (2N_i\varepsilon_{ox}C_{ox})/(N_b\varepsilon_{Si}C_{min}T_{ox}) \)

Thus, once a C-T measurement is performed, the minority carrier lifetime can be determined.

**EXPERIMENTAL**

The C-T response of MOS capacitors were measured using a Micromanipulator model 410 CV plotter in conjunction with a Yagowawa A4 X-Y recorder. Samples were pulsed from accumulation into deep-depletion by manually altering (instantaneously) the voltage across the gate. The X-Y recorder was then activated (time base mode), thus measuring the capacitance of the system as the capacitor relaxed back to Cmin. The experimental set-up is shown in Figure 2:

**Figure 2:** C-T measurement set-up.

**RESULTS**

A typical C-T response that resulted from the measurement of MOS capacitors is shown in Figure 3.

**Figure 3:** Measured C-T Response.
Figure 4: C–T Plot

Figure 5: ZERBST Plot of C–T from Figure 4.
A Zerbst analysis was attempted on this C-T data. However, the differentiation required could not be performed on this data. This data needs to be measured and then down-loaded by computer to the VAX. Observation of Figure 1 indicates that there is not enough resolution between points to accurately determine the derivative at each point. To assure the operation of the program that differentiates the data, C-T data from Schroder's ADVANCED MOS DEVICES (4) was entered as input, this is shown in Figure 4. The resulting ZERBST plot that was generated (using a FORTRAN program to perform the differentiation) is given in Figure 5. This produced a minority carrier lifetime of 470 microseconds.

CONCLUSION

In this study, a method of measuring minority carrier lifetimes (\(T_g\)) was presented. There was not enough resolution in C-T measurements performed in this work to perform Zerbst's analysis. However, a program was written that implemented Zerbst's analysis effectively on C-T data. It appears that one needs to differentiate C-T data that is down-loaded from actual measurements (rather than extract data by hand) in order to achieve meaningful results. Once this is carried out, it appears that this method will be a convenient technique for measuring \(T_g\) of a device.

REFERENCES


16 x 1 nMOS STATIC RANDOM ACCESS MEMORY DESIGN

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ABSTRACT

A Static Random Access Memory (SRAM) was designed using a 2 micron minimum geometry, nMOS fabrication process on an Apollo design station. In addition to the SRAM integrated circuit, test structures were included to help characterize the process and design. The chip contained over 200 transistors on a die size of 800 square microns. Simulation results predicted an access time of 50 nano-seconds. The pads were configured to fit a 20 pin probe card to facilitate automatic testing.

INTRODUCTION

The design of any complex integrated circuit needs to be reduced into its component parts. A hierarchical approach can be used in which circuits are built from the bottom up. Cells are made to represent the commonly used parts and combined to form the final circuit. *MentorGraphics is a design software company that has implemented this approach to VLSI design.

As shown in Figure 1, the first phase of any hierarchical design is the creation of the basic cells. These schematics are then entered into the computer through the NETED software package. NETED is a schematic capture program which converts circuit diagrams into nodelists. These nodelists, in conjunction with a transistor Models file, define the circuit, interconnections, and the device characteristics of the nMOS transistors.

Circuit simulations are performed with the MSIMON software package. This program is similar to SPICE but optimized for MOS devices. For each cell, input waveforms had to be determined in order to provide thorough simulation of all combinations of inputs. Results often indicate the need for changes to the circuits. After the cells operate correctly, they are combined and tested in larger groups.

After correct circuit simulation layout is performed. This is the transformation of the schematics into the various levels

* NETED, MSIMON, CHIPGRAPH and DRACULA are proprietary products of MentorGraphics Corporation.
FIGURE 1: DESIGN FLOWCHART

FIGURE 2: STATIC MEMORY CELL
of an integrated circuit. In the nMOS process the following layers were needed: n+ diffusion, n implant, poly-silicon, contact cuts and metal. The CHIPGRAPH program is used to graphically represent these layers. Standard cells for the more commonly used circuits are laid out first, then combined. The remainder of the circuits were added on to this array and created the actual SRAM chip. Input/Output pads were carefully placed for convenient automatic probing based on RIT's probe card configuration.

After layout each cell was verified using DRACULA, a design rule checker, configured to check the layout against Mead-Conway design rules. DRACULA catches the human errors associated with a large scale integrated design.

EXPERIMENT

The fundamental cell in the 16 x 1 SRAM was the memory cell, shown in Figure 2. This cell consists of two cross coupled inverters with depletion mode transistor loads and two pass transistors. This cell uses the bit lines BL and BL which contain the data signal, its complement, and the Row Select,(RS). When a memory cell is going to be accessed RS goes high, which biases the pass transistors and allows data to flow into or out of the cell.

The sense amplifier, shown in Figure 3, also uses two cross coupled inverters, however there is a pass transistor to ground controlled by the SENSE signal and no pass transistors on the bit lines. The sense amplifier's function is to boost the output signal during the read cycle and to be off during the write cycle and dormant states. This is important because the bit lines are run in poly-silicon and through pass transistors so losses are expected to occur between memory cell and outputs.

The SENSE and RS signals are provided through two line decoders, one of which is shown in Figure 4. This circuit provides a 2 to 4 decoder function. Using one as a row decoder and the other as a column decoder, all 16 memory cells can be individually addressed. The line decoder is a pass transistor network which only functions when the chip enable,(CE) line is high. A0-3 are the address lines.

These components were combined to provide a 4 x 1 memory element. This combined 4 memory cells, sense amp, and line decoder. Additional control logic for Write Enable, (WE), was added as a component of the SENSE signal and DATA was connected to the bit lines. The circuit was then simulated by providing force pulses which would write a '1', read a '1', write a '0', read a '0'.

Once these functions were performed successfully, this column was replicated four times to create a 16 x 1 memory array. This circuit was simulated, modified and the final circuit is shown in Figure 5, in which the actual circuits are represented.
FIGURE 5: SRAM FUNCTIONAL DIAGRAM
symbolically in the various blocks labeled cell, sense amp and row decoder.

Layout followed a similar technique starting with the creation of basic cells. Special effort was made to have the SRAM cell and sense amp be the same size in order for the control lines to run together efficiently. The cells were then replicated and combined to form the correct functional groups. Many revisions were performed to achieve a compact design. Finally power and ground lines were added creating the need for further modification.

Test structures including; enhancement and depletion mode transistors, a 4:1 ratio inverter, diffusion, implant and poly-silicon resistors, a 21 stage ring oscillator, two inputs of a line decoder and a single memory cell were added to allow for design and fabrication checks. The pads were configured to fit an existing probe card making automatic probing possible.

RESULTS

Figure 6 shows the delay between the forcing of the chip enable signal and the row and column select (R0 and C0) lines going high. This creates a fundamental constraint of 50 nano-seconds access time for this chip. Figure 7 shows the resulting output for all the possible actions in a memory cell. Cycle A with the WE line pulsed high indicates the writing of a '1' into the memory cell when the R0 signal is high. During the B cycle the WE signal is low signifying a Read Enable, when R0 goes high the output is valid and the corresponding '1' is read from the cell on the output, (OUT) pad. Cycle C and D represent the writing of a '0' and the reading of a '0' respectively.

Figure 8 contains the layout of the memory cell. The BL and BL lines are run vertically in polysilicon, while Vcc, Gnd and RS are run horizontally in metal. The regions in which polysilicon overlap diffusion a transistor is created. This layout corresponds clearly with the cell schematic of Figure 2.

Figure 9 is the layout for the line decoder. Due to the nature of pass transistor networks this logical function is accomplished with the minimum consumption of silicon real estate. On each of the four columns the upper two transistors comprise the AND function and the lower two create the NOR function.

Figure 10 contains the sense amplifier and its associated control logic. The signal lines are run horizontally in metal across the bottom driven by super buffers. Super buffers are capable of very large drive currents and help overcome parasitic line losses and threshold drops that occur through pass transistors. They do detrimentally add delay onto the read and write cycles.
Figure 6: Row/Column Select vs CE

Figure 7: Read/Write Cycle

Voltage vs Time Graphs
FIGURE 8: SRAM MEMORY CELL LAYOUT
CONCLUSION

The final chip is shown in Figure 11. The actual SRAM portion of the chip fills 800 square microns and contains over 200 transistors. The IC requires four address lines, 2 control lines, 2 Input/Output lines in addition to power and ground. The circuits simulated successfully and predicts an access time of 50 nano-seconds for a given Read/Write operation. It is anticipated that this project will be fabricated at RIT in the future.

ACKNOWLEDGEMENTS

The successful completion of this project would not have been possible without the support of RIT's Computer Engineering Department who provided the computer resources. Appreciation goes to Dr. George Brown who gave technical support along with Larry Reuben and Bob Appleby who helped me get around the brick walls.

FIGURE 11: SRAM IC LAYOUT
RESPONSE SURFACE METHODOLOGY USING EXPERIMENTAL DESIGN

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ABSTRACT

A Central—Composite Full Factorial design was performed in aiming to optimize the develop and bake processes on KTI 820 resist and KTI 934 developer using the GCA Wafertrac. The responses looked at were critical dimension and resist thickness after development with the independent variables of postbake temperature, postbake time and developer time. Analysis of the data was done using SAS as a software tool.

INTRODUCTION

Response surface methodology, or RSM, is a collection of mathematical and statistical techniques useful for analyzing problems in which several independent variables influence a dependent variable or response. Often, they are employed to optimize the response.

The first step in RSM is to find a suitable approximation of the relationship between the response or the random variable and the set of independent variables. A low-order polynomial in some range of the independent variable is employed. If the response is well modeled by a linear function of the independent variables, then the approximating function is the first-order model. If there is curvature in the system, then a polynomial of higher degree must be used. The method of least squares is used to estimate the parameters in the approximating polynomial. Response surface analysis is then done in terms of the fitted surface. If the fitted surface is an adequate approximation of the true response function, then analysis of the fitted surface will be approximately equivalent to analysis of the actual system. If not, revisions to the initial guess will be decided on from the results obtained. RSM is a sequential process and the objective is to quickly and efficiently lead the experimenter to the general vicinity of the optimum. Once this region has been found, a more elaborate analysis is performed to locate the optimum.

To effectively use RSM three things must be kept in mind: 1) a through understanding of Experimental Design, 2) an appropriate statistical software tool and 3) a good understanding of the process to be optimized.
The three basic principals of experimental design are replication, randomization, and blocking. Replication requires the repetition of the experiment at it's center points which allows experimenter to estimate the experimental error. This becomes a unit of measurement for determining whether the observed differences in the experimental data are actually statistically different and thus gives an accurate representation of the effects of the different factors. Randomization requires both the allocation of the experimental materials and the order of the experimental runs to be randomly determined. Thereby "averaging out" the effects of extraneous factors. A 'Block' is defined as a portion of the experimental material that should be more homogenous that the entire set of materials. Blocking involves making comparisons among the conditions of interest within each of these blocks. Thus, blocking is defined as a technique used to increase the precision of an experiment.

The purpose of the experiment was two fold. First, to determine the effects of three factors: 1) Postbake temperature (ranging from 120-140C, in increments of 5C), 2) Postbake time (ranging from 90-130secs, in increments of 10secs), and 3) Develop time (ranging from 21-25secs, in increments of 1sec) on the responses: 1) Critical dimension (4um pitch) and 2) Resist thickness after development. The second, was to find the optimum operating conditions to simultaneously maximize the resist thickness after development and minimize the critical dimension loss.

EXPERIMENT

The resist evaluated was KTI 820 and the developer was KTI 934 with a one to one dilution with DI water. The resist thickness after development was measured on a Lietz system at Kodak and the critical dimensions were measured on the Nanoline system at RIT.

The model used was based on the assumption that all third order and above interactions were negligible or did not exist. This assumption is based on prior knowledge of the system and was believed to be an accurate assumption. The model for this experiment is stated below.

THICKNESS, CD's = F [ POSTBAKE TEMPERATURE
POSTBAKE TIME
DEVELOPER TIME
(POSTBAKE TEMPERATURE)
(POSTBAKE TIME)
(DEVELOPER TIME)
POSTBAKE TEMPERATURE * POSTBAKE TIME
POSTBAKE TEMPERATURE * DEVELOPER TIME
POSTBAKE TIME * DEVELOPER TIME ]
The selection of an experimental design is based on the complexity of the model. The design selected was a Central Composite - Full Factorial 2 design. This was selected based on the complete information that could be obtained from using this design type with the least number of runs. They were 8 Factorial Point runs, 6 Axial Point runs and 4 Center Point runs, for a total of 18 runs.

An interactions table was set-up and the 18 runs were determined. The runs were randomized to keep with the general principles of experimental design. A listing of the runs and the randomized sequencing is shown in Table 1 below. (For a complete understanding of how the table was set-up and how the runs were randomized please refer to Reference 3.) The basic processing sequence began with growing a wet thermal oxide of approximately 5000 Å. This was followed by applying resist on the wafers at 5000 rpm for 30 secs with the standard RIT program which would give us an initial resist thickness of 1.4µm. The randomized runs with the various different develop and bake cycles were performed next. The resist thickness after development and critical dimensions were then measured at three points on each wafer, top, center and bottom.

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Table 1. - DESIGN RUNS
The measured resist thickness after development and the critical dimensions measured were recorded in Table 2. Measurements were taken from three locations on each wafer, top, center and bottom.

Table 2 below, TAD refers to the thickness after development and CD refers to critical dimension.

<table>
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<th>BOT (A)</th>
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</table>

Table 2 - Experimental Data
Implementing the obtained data on SAS we obtain a F value, and a PR value for each dependent variable, that is, AVGCD (average critical dimension), STDCD (standard deviation of the cd values), AVGTAD (average resist thickness after development) and STDTAD (standard deviation of the resist thickness after development). The F value is defined as the ratio of how well the model fits the experimental data to the actual experimental data and so for a good approximation we would like this number to be very large.[2] The PR or probability value is defined as the probability or the confidence of the model and ideally would be in the range of .05, which is a 95% confidence level. A summary of these values is presented in table 3.

<table>
<thead>
<tr>
<th>DEP VARIABLE</th>
<th>F-VALUE</th>
<th>PR-VALUE</th>
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<tbody>
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<td>AVGCD</td>
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<td>AVGTAD</td>
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<tr>
<td>STDTAD</td>
<td>0.76</td>
<td>0.6539</td>
</tr>
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TABLE 3 - SAS ANALYSIS VALUES

Clearly we see that the model is insignificant and this could have been due to one of many reasons. We could have had a lot of variability in the process or the factors that we looked at could not have explained the variability. Also, the range of values we looked at may not have been in the correct area. A lack-of-fit analysis followed and this was to determine if we had accounted for all the terms that we should have. This was to check if the assumption made regarding three factor and above terms being negligible was a valid one. From the F value and sum of squares value obtained we were able to justify making that assumption.

Finally, to decide on an optimum run or set of runs, we compared the means and the standard deviations of both the resist thickness after development and the critical dimensions. The run that gave us the least resist thickness loss and the best critical dimension with the lowest standard deviation was Reference run 9 with a resist thickness after development of 13603A (STD = 66.98) and critical dimension of 1.9um (STD = .03).
CONCLUSION

The optimum run was determined to be reference run 9 with the following parameters. Bake temperature = 120°C, Bake time = 110 sec, and Develop time = 23 secs. The resist thickness after development was measured as 13603 Å with a standard deviation of 66.98 and the critical dimension measured was 1.9 μm with a standard deviation of 0.03.

As a follow up to this experiment I would decrease range on the bake temperature and increase the range on the develop time.

ACKNOWLEDGEMENTS

I would sincerely like to thank Sue Zygo of Eastman Kodak for all her insight and support. I would also like to thank Mike Jackson and Kathy Hesler of the Microelectronic Engineering department at RIT for making this project possible.

REFERENCES


DEVELOPMENT AND EVALUATION OF CHLORINATED GATE OXIDES

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ABSTRACT

The effect of TCA tube cleaning and oxidation on mobile ion contamination for the growth of gate oxides was investigated. It was found that the TCA tube clean had a major effect in reduction of mobile ions, while the TCA gate oxide process employed had a negligible effect.

INTRODUCTION

It has been reported that chlorine doping can be used to improve the electrical performance of thermally grown oxides. Improvement over dry oxides has been reported in the following areas: 1) increased minority carrier lifetimes, 2) increased growth rates, 3) mobile ion passivation, 4) decreased size and density of oxidation induced stacking faults, and 5) increase in the average breakdown fields realized [1]. Possible drawbacks to a chlorinated oxide include complication of process, safety, degradation of oxide at very high chlorine levels, and possible etching of substrate in more highly doped areas.

There are many chlorine sources commercially available for use in the microelectronics industry, but the obvious choice for reasons of safety, ease of use, and purity is (1,1,1) Trichloroethane → (TCA). Other possible sources include Cl₂ gas, HCl gas, and TCE (trichloroethene). TCA is much safer than either TCE or HCl chlorine sources. Using TCA eliminates the possibility of extremely costly HCl leaks caused by the corrosion of regulators, and the loosening of gas jungle fittings. As far as worker safety is concerned, TCA is the safest of the chlorine source chemicals. OSHA lists the PEL’s of these chemicals as the following: J.C.S. TCA = 350 ppm, TCE = 100ppm, HCl = 5ppm [2]. Permissible exposure levels (PEL’s) given above correspond to an employee’s permissible average exposure in any eight hour shift of a forty hour week [2]. TCA also offers the advantage of being much cleaner than HCl. TCA can be made up to 99.9999% pure, many orders of magnitude lower in contamination than current electronic grade HCl [3]. TCA is not subject to the variability of contaminants such as iron and moisture which are common in HCl [2]. Purity is the factor cited in uniform and controlled growth of oxides with high dielectric strength and minority carrier lifetimes [2].

For this experiment a J.C. Schumacher TCA system was employed. This system uses nitrogen as a carrier gas for the TCA. The N₂ is bubbled through a temperature controlled bubbler apparatus and the TCA/N₂ mixture is combined with an excess of O₂
before entering the furnace.

The crux of the evaluation of the new gate oxide process will be in terms of the effect that chlorine in the oxide has on mobile ion (i.e. sodium) contamination. The hypothesis that chlorinated oxides offer the advantage of mobile charge gettering over dry O₂ growths will be investigated. The reduction in mobile charge seen in chlorinated oxides is said to work via sodium gettering in the oxide itself. The neutralization of positively charged mobile ions observed in TCA oxide is generally attributed to reactions of the mobile ions with the chlorine incorporated in the oxide as it is thermally grown. As far as exactly how the gettering works, the precise mechanisms of the mobile charge neutralization are not yet well understood. The best proposal at this point in time is that the mobile ions simply become trapped when they reach the vicinity of chlorine incorporated in a Si-O-Cl bond, where chlorine is substitutional for oxygen [4].

To determine if TCA does indeed getter Na⁺ ions, a C-V bias/stress test will be implemented on oxides grown by the dry O₂ process (pre tube clean), dry O₂ (post tube clean), and the new TCA process (post tube clean). In the bias stress test the wafer is heated to 200 degrees C. to facilitate the movement of mobile ions in the oxide. At the same time, a positive bias is applied to a particular MOS cap. The bias and the high temperature are held on the MOS cap for 5 minutes to insure complete movement of all mobile ions. The positive bias applied works to move all of the positively charged mobile ions away from the SiO₂/Al interface and toward the Si/SiO₂ interface. This has a tendency to shift the flatband voltage to the left, (toward more negative voltages). After 5 minutes, the chuck is cooled to room temperature and the bias is taken off of the MOS cap. A plot of C-V characteristics is then obtained to obtain a (-)Vfb value. The whole process is then repeated with a positive bias to yield a (+)Vfb value. The mobile ion density can then be computed using Equation (1) below:

$$Na^+ = (\frac{C_{ox}}{q}) \cdot \text{ABS}(V_{fb(-)} - V_{fb(+)}) \quad (1)$$

where Cox is computed using Equation (2), Na⁺ is the mobile charge density in ions/cm², and the Vfb's are obtained as described above from the bias stress C-V plots.

$$C_{ox} = \frac{C_{max}(\text{from CV plot})}{\text{Area of MOScap}} \quad (2)$$

The effective mobile ion concentrations calculated using the above formulas will be compared, to determine if the new oxide process has indeed improved RIT's gate oxides and if the TCA tube clean has had any effect.
A standard set of MOS caps was fabricated using the temperatures, times, gas flows, etc were all recorded and are contained in the process sheets found in Appendix II. (For a outline of all processes used see Appendix I.) The growth was basically a 1000 degree C., dry O2, 1 hour oxidation followed by a N2 anneal at the same temperature for 30 minutes. These conditions yielded an oxide thickness of approximately 650 Angstroms. These capacitors were then tested on a Princeton Applied Research (Model 410) high frequency C-V measurement system equipped with a Temptronic TP36 Thermochuck system, for the thermal stress bias test. First the MOS caps were measured to get a pre-stress C-V curve. The gate voltage was swept from (+)20 to (-)20 volts DC with a 1MHz AC signal. For consistency all measurements were taken with the lights on. After the pre-stress C-V curve was obtained, the MOS cap being evaluated was biased to -15 volts to move all of the mobile charge in the oxide to the SiO2/Al interface. This bias remained applied while the wafer was heated to 200 degrees C. for 5 minutes. After the wafer was cooled back down to room temperature, the bias was removed and a second shifted C-V curve was obtained. The entire stress bias routine was then repeated with a +15 volt bias. Once again another shifted C-V curve was plotted on the same axis. The change in flatband voltage was then read from the C-V plots ((+) bias value - (-) bias value). This shift in flatband voltage was then converted to an effective total mobile ion concentration using the equations outlined in the theory.

The next step was to ‘condition’ the oxide tube with TCA so that existing mobile ion contamination would not effect the results of the TCA process. During the clean, temperatures were kept higher than the standard gate oxide temperatures to incorporate more chlorine in the tube, and in turn increase the efficiency of the mobile charge passivation taking place. Immediately after the tube was cleaned another set of wafers was oxidized with the current dry O2 gate oxide process, as a means of a truly fair comparison with the TCA oxides.

In the final phase of the project ‘new’ MOS caps were fabricated using the new TCA gate oxide process (as outlined on the TCA gate oxide process sheets contained in Appendix I. This oxide was grown immediately following the second dry O2 process in the cleaned tube to make the comparison truly valid. The ‘new’ MOS caps were then tested in the same manner as the ‘old’ MOS caps. The data obtained for the older gate oxide process MOScaps, was then compared to the data obtained for the new gate oxide process. Appropriate conclusions were drawn as to the effectiveness of the new TCA gate oxide process as far as mobile charge is concerned.
RESULTS AND DISCUSSION

The results shown in Table 1 indicated a $1.96 \times 10^{12}$ ions/cm$^2$ (32%) improvement in mobile ion contamination after the tube clean (via comparison of the pre and post clean dry O$_2$ results). The TCA gate oxide process showed a reduction in mobile charge of $0.07 \times 10^{12}$ ions/cm$^2$ (8%) over the standard dry O$_2$ gate oxide process. It is unlikely that the new TCA Gate oxide process reduced the effective mobile ion levels in the TCA MOS caps, as the standard deviation of the measurement was greater than the resultant improvement. However, it was clearly evident that the TCA tube clean employed did have a profound effect on reducing mobile ion levels.

Table 1: Mobile Ion Levels and Vfb Shifts

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Process 1</th>
<th>Process 2</th>
<th>Process 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vfb shift</td>
<td>8.74 volts</td>
<td>2.76 volts</td>
<td>2.56 volts</td>
</tr>
<tr>
<td>Na$^+$ (ions/cm$^2$)</td>
<td>$2.87 \times 10^{12}$</td>
<td>$0.91 \times 10^{12}$</td>
<td>$0.84 \times 10^{12}$</td>
</tr>
<tr>
<td>Na$^+$ Std. Dev.</td>
<td>$0.23 \times 10^{12}$</td>
<td>$0.14 \times 10^{12}$</td>
<td>$0.12 \times 10^{12}$</td>
</tr>
</tbody>
</table>

Where:
- Process 1 = standard process
- Process 2 = standard process after TCA clean
- Process 3 = TCA gate oxide process

Although the TCA gate oxide process had little effect on reducing mobile charge, the other possible benefits such as increased minority carrier lifetimes, increased average breakdown voltages, and decreased stacking faults should be evaluated before the process is ruled out as a viable alternative to the standard dry O$_2$ gate oxide process.

CONCLUSIONS

The TCA tube clean process was found to be an effective way of reducing mobile charge. Although the TCA gate oxide process employed was found to have little effect on mobile ion contamination in a single run, I recommend that the process should be used as a means of keeping the system clean between major tube cleans.

ACKNOWLEDGEMENTS

Special Thanks to Steve Ward, Gary Runkle, and Scott Blondell for their help with installation of the TCA system! Very special thanks to Wayne Moses, Tom McAlpin, and J.C. Schumacher for the donation of a complete TCA system.
REFERENCES


3) "Product Application Note # 14: TCA Requirements for thin High- Integrity Oxides.", J.C. Schumacher Company, 1986.


APPENDICES

Appendix I : Processes Employed
Appendix II : Processing Sheets for MOS Caps
Appendix III : Sample Experimental C-V Curves

APPENDIX I : Processes Employed

I) Standard Dry O2 Gate Oxide Process Parameters
   Oxide Thickness Target; 650 Angstroms
   Tube temperature; 1000 degrees C.
   O2 Flow Rate; 5 lpm.
   Time; 60 minutes

II) TCA Gate Oxide Process
   Oxide Thickness Target; 650 Angstroms
   Tube Temperature; 1000 degrees C.
   Initial Dry O2 Protective Oxide Growth
   O2 Flow Rate; 3.2 lpm.
   Time; 10 minutes
   TCA Oxide Growth
   Bubbler Temperature; 25 degrees C.
   N2 flow Rate; 160 sccm.
   O2 flow Rate; 3.2 lpm.
   Time; 35 minutes
   O2 Purge
   O2 Flow Rate; 3.2 lpm.
   Time; 5 minutes

III) Gate Oxide Anneal
   Tube Temperature; 1000 degrees C.
   Time; 20 minutes
   N2 Flow Rate; 6 lpm.

IV) TCA Tube Clean
   Tube Temperature; 1100 degrees C.
   Time; 3 hours
   Bubbler Temperature; 25 degrees C.
   N2 Flow Rate; 250 sccm.
   O2 Flow Rate; 5 lpm.
CMOSFET DEVICES - DESIGN, FABRICATION AND TESTING

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ABSTRACT

Metal-gate CMOS (Complimentary Metal Oxide Semiconductors) devices were designed, fabricated and tested. The design was actually a simplified test chip, with diffused resistors, individual NMOS and PMOS transistors, and various gates (inverter, NOR, NAND, etc). The fabrication took place with the use of a p-type well in order to fabricate both types of transistors on the same n-type substrate. Testing yielded only working resistors, as difficulties in the metallization step of fabrication caused the thickness of the gate oxide to reduce significantly enough to cause a direct short between the drain and source regions of both transistor types. This did not allow for a direct determination of necessary future ion implantation correction doses, but estimates for a range of feasible results were determined.

INTRODUCTION

The 1980’s have become known as the era of VLSI. With the number of transistors per chip reaching into the range of one million and above, power dissipation has become a fundamental limitation. This is where CMOS technology is advantageous. The power characteristics for CMOS are extremely low in comparison to NMOS technology, which dominated the 1970’s. In the infancy of CMOS, lower speed and poorer packing density, as well as process complication, did not allow for a favorable comparison with NMOS circuitry. However, with the shrinking of transistors to as small as 0.5 micron channel-lengths for VLSI applications, the current delivered by p-channel devices can now approach the current capabilities of n-channel devices of the same size. New techniques used for interconnects and other new approaches to CMOS (retrograde wells, epitaxy, device isolation, etc.) have allowed for very dense circuits to be fabricated. Processes for CMOS and NMOS technologies are now both very complicated, with the difference in complexity being reduced to almost nothing.

The prominence of CMOS in industry leads to the great interest in this project at R.I.T. The technology used in this project is an expansion of the existing metal-gate PMOS process. The metal-gate is considered fairly primitive in industry, but it is to be used at R.I.T. until the capability of polysilicon for a self-aligned process is developed. Another major step in commercial processing is ion implantation, which is necessary for two reasons: one is the fact that CMOS devices should be relatively lightly doped for proper operation and, secondly,
enhancement mode devices are necessary, with ion implantation the only way possible to shift threshold voltages in the proper manner to obtain these devices. One goal of this project is a first estimate of the necessary implant doses for the shifting of the threshold voltages in such a way that enhancement mode devices are obtained for NMOS and PMOS transistors.

The CMOS design, shown in Figure 1, consisted of diffused resistors for each diffusion level, individual PMOSFET and NMOSFET transistors, as well as CMOS devices (including an inverter, a ring oscillator, and various gates). The reason for using diffused resistors in the design is for the ability to monitor each diffusion step for the necessary characteristics, i.e. sheet resistance and surface concentration. Individual n- and p-channel devices were designed for both a thin oxide and a thick oxide below the gate. This allows for the threshold voltages for both actual devices to be determined directly, and also the threshold voltage of the field oxide in the same manner. The other devices in the design will be tested to characterize the basic CMOS device performance in simple circuits.

The actual fabrication of these devices was performed following the six-level process utilized by James Pollard previously at R.I.T. The NMOS devices were fabricated by first developing a relatively lightly doped p-type well in the n-type substrate. The n-type drains and sources were then diffused into this region. The PMOS device was processed by simply diffusing boron into the n-type substrate.

As seen in Figure 2, the cross-section of a CMOS device, heavily doped p+ and n+ regions have been placed next to the oppositely doped device. This is done in order to prevent a phenomenon known as latch-up. Latch-up is a problem which occurs in CMOS when a four-level pnpn structure is formed during processing. This two-transistor bipolar configuration can destroy normal circuit operation. The addition of these "plugs" helps to isolate the individual devices and thus prevent latch-up.
The reason for using a p-type well instead of an n-type well is highly process dependent. In industry, both types of wells are commonly used. However, here at R.I.T., n-type wafers are most often used, and thus the pwell is used. Another reason for using the pwell is that this well has to be relatively deep in order to contain the n-type drain and source. Boron is the dopant used to develop the pwell, and the fact that it is slower in diffusing than phosphorous, which would be necessary to develop an nwell, allows for a more controllable deep drive-in.

EXPERIMENTAL

The CMOS design was generated using a computer-aided design program called ICE (Integrated Circuit Emulator). Each of the six necessary process levels are defined within this software as CIF files, which are used stored in a file from which it is possible to generate a master reticle and ultimately from this reticle, a working mask for each level of the process. Prior to fabrication, the process was characterized using SUPREM, with full results summarized in Appendix A. SUPREM allows the calculation of junction depths for each diffusion and respective sheet resistances and carrier concentrations for each level of diffusion. SPICE simulations were also done on the individual devices and on the CMOS inverter with full results in Appendix B. The following table is a summary of the results from SPICE and SUPREM.

<table>
<thead>
<tr>
<th></th>
<th>Junction Depth</th>
<th>Sheet Resistance</th>
<th>Threshold Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwell</td>
<td>7.2 μm</td>
<td>2576 ohms/sq</td>
<td></td>
</tr>
<tr>
<td>NMOS</td>
<td>3.8 μm</td>
<td>3.88 ohms/sq</td>
<td>-0.26</td>
</tr>
<tr>
<td>PMOS</td>
<td>2.0 μm</td>
<td>75.0 ohms/sq</td>
<td>-1.11</td>
</tr>
</tbody>
</table>

The fabrication sequence took place via the process shown in Appendix C. Field oxides of 5000 angstroms, grown in atmospheric steam, were commonly used throughout the process. Photolithography took place with the use of KTI 820 photoresist and ZX-934 developer. The GCA Wafertrac was used to coat and prebake the wafers, while batch development was used after exposure on the Kasper contact aligners. Spin-on dopants were used for each of the three diffusion steps, with a short predoped step, followed by the stripping of the spin-on glass prior to a drive-in step.

Ellipsometer readings were taken after each oxide growth, and four point probe measurements following the diffusion steps. These tests were performed on control wafers used throughout the process. A gate oxide of 850 angstroms was desired, with the growth taking place in a dry oxygen ambient. Metallization was
the final step, with the layer being put down in an evacuation chamber. Testing after the completion of fabrication utilized the Hewlett-Packard 4145B Semiconductor Parameter Analyzer, which allows for the measurement of anything from resistance to transistor characteristics to individual gate performance.

RESULTS

Originally, six wafers were to be used in the process, three for control and three for device wafers. One control wafer was broken before any processing took place. This left a control wafer to monitor the NMOS diffusions (this included the pwell also) and PMOS diffusion. Misalignment for the second level took place due to the improper generation of the alignment marks on the mask. This was only a problem on one of the device wafers. However, prior to alignment at the fifth photolithography level, the two device wafers which had proper alignment were shattered, thus already decreasing the yield to 33% before processing was even completed.

Resistivity values from four point probe results after each predeposition step (for a complete summary of results, see Appendix D) showed that the pwell and PMOS drain and source were similarly doped, while the NMOS drain and source was heavily doped. This was not originally desired, but the pwell resistivity yields a doping concentration of $3 \times 10^{14}$, which is not a problem. The PMOS drain and source region were thus more lightly doped than desired, but again this should not have been a problem. The oxide growths all took place as desired, with the final field oxide only having a thickness of around 2000 angstroms. The reason for the thinner oxide at this level was to reduce the drive-in time for the NMOS drain and source, so as not to drive it through the previously diffused pwell. The gate oxide grown was approximately the 850 angstroms desired, thus allowing a comparison with the SPICE and SUPREM models. SUPREM showed a gate oxide of approximately 900 angstroms for the gate oxide growth conditions, while this thickness was used in all SPICE simulations for the MOS models.

The same could not be said for the junction depth values in comparing the results to the SUPREM simulations. The junction depths obtained by the groove-and-stain technique did not match up with those found using SUPREM. This has long been a problem at R.I.T., with the values found in SUPREM not matching up with actual data. In the case of the n-type spin-on dopant, however, the one used is a combination of phosphorous and arsenic, while only one element can be modeled using SPICE. The sheet resistances determined by the measured resistor values do not make sense in themselves, or when compared to SUPREM. However, in comparing resistor values for the same size resistors for each diffusion level, the pwell is the most highly resistive and the NMOS is the least resistive. This leads one to believe that the NMOS drain and source were the most highly doped region and the pwell the most lightly doped. The problems in determining the
sheet resistances and resistivities of each diffusion can be attributed to the spin-on glasses used as dopants. The coverage and uniformity over the entire wafer is not good, thus leading to inconsistency across the wafer.

Though the modeling of device parameters did not yield positive results, the device performance should still have been good. However, this was not the case. As was stated previously, before fabrication was even completed, the device yield was already down to 33%. With the misalignment which also took place, the yield on the lone device wafer was down to about thirty chips. The diffused resistors yielded the proper characteristics in both values and linearity. However, no MOSFET devices could be found anywhere on the wafer. When trying to obtain the characteristic curves of the transistors, a short between the drain and source of both transistor types was observed. This lead to an investigation of the gate oxide. Inquiries into other gate oxides, grown in the same tube, around the same time, indicate that the quality of the gate oxide was extremely inadequate. This, combined with the fact that the metallization step required three separate runs during processing due to a shutter design problem which did not shield the wafers prior to aluminum evaporation, led to the conclusion that working MOS devices were highly unlikely.

CONCLUSION

CMOS device fabrication at R.I.T. is feasible. The poor results obtained can be attributed to low quality oxides and metallization problems, which are both correctable. Secondly, ion implantation is a necessity for both threshold voltage correction (see Appendix a) and the actual doping of the drain and source regions. This will allow for more controllable and repeatable junction depths and sheet resistances. Until this is realized at R.I.T., planar diffusion sources should be used to get a more uniform and constant doping profile. With the above improvements and slightly better simulation packages, CMOS at R.I.T. will be a reality.

REFERENCE LIST


APPENDIX D

SUMMARY OF RESULTS

Summary of Oxide Growths

<table>
<thead>
<tr>
<th>Lithography Level</th>
<th>Oxide Thickness</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>4089 A</td>
</tr>
<tr>
<td>2</td>
<td>4321 A</td>
</tr>
<tr>
<td>3</td>
<td>4500 A</td>
</tr>
<tr>
<td>4</td>
<td>2000 A</td>
</tr>
<tr>
<td></td>
<td>850 A</td>
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</table>

Four Point Probe Summary

<table>
<thead>
<tr>
<th>V/I</th>
<th>Psh</th>
<th>CONC</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwell</td>
<td>48.55</td>
<td>220</td>
</tr>
<tr>
<td>PMOS</td>
<td>54.3</td>
<td>246</td>
</tr>
<tr>
<td>NMOS</td>
<td>---</td>
<td>---</td>
</tr>
</tbody>
</table>

No data for predep.

Resistor Values for Constant Size (47 squares)

<table>
<thead>
<tr>
<th>Resistance (ohms)</th>
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</thead>
<tbody>
<tr>
<td>pwell</td>
</tr>
<tr>
<td>PMOS</td>
</tr>
<tr>
<td>NMOS</td>
</tr>
</tbody>
</table>

Groove and Stain Results

<table>
<thead>
<tr>
<th>Junction Depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>pwell</td>
</tr>
<tr>
<td>PMOS</td>
</tr>
<tr>
<td>NMOS</td>
</tr>
</tbody>
</table>

Threshold Adjust Implant

- assuming a Beam Current of 10 uA
- Boron must be implanted for both NMOS and PMOS Vt correction

<table>
<thead>
<tr>
<th>Vt Adjust (volts)</th>
<th>DOSE (atoms/cm^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+1</td>
<td>2.69E11</td>
</tr>
<tr>
<td>+2</td>
<td>5.38E11</td>
</tr>
<tr>
<td>+3</td>
<td>8.06E11</td>
</tr>
<tr>
<td>+4</td>
<td>1.08E12</td>
</tr>
<tr>
<td>+5</td>
<td>1.34E12</td>
</tr>
</tbody>
</table>
CHARACTERIZATION OF THE PERKIN-ELMER MODEL 140 PROJECTION ALIGNER EXPOSURE SOURCE AND MODELING OF RESIST PROFILES

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ABSTRACT

A correlation between scan speed and exposure dose, was obtained for the Perkin-Elmer Model 140 Projection Aligner to facilitate accurate resist profile modeling. A photovoltaic cell collector with filtering was mounted on a modified wafer chuck to acquire exposure data. The relationship between scan speed and exposure was found to be linear when plotted on log-log scale and predictable to within 5%. Lines of 1.4 um in Shipley 1400-27 resist and 1.6 um in KTI 820 resist were successfully imaged. Modeling of the scanner's output aerial image via PROSIM (Perkin-Elmer resist profile model) was performed with fair results.

INTRODUCTION

The Perkin-Elmer 140 Projection Aligner uses a scanning slit exposure system and 1:1 projection optics to create a uniform exposure capable of high resolution over the entire wafer surface. Figure 1-A shows the unfolded projection optics, and one should note that the image and object planes are conjugate planes located at a radius $r$. The optical system shown in Figure 1-B consists of a spherical concave primary mirror, a concentric spherical convex secondary mirror, and an array of three flat folding mirrors. The radii of the primary and secondary mirrors are adjusted to create an annular region of nearly perfect optical imagery for the object/image plane. The array of three flat folding mirrors is included so that the mask and the wafer may be locked together in a single assembly for a single direction scan.[1]

The projection optics used have several inherent advantages. The geometry promotes telecentricity evidenced by the parallelism of the principal rays to the system axis at each focal plane. This allows the mask plane to depart from the nominal object plane and system focus can be preserved as long as the wafer plane is displaced by the same distance from the nominal image plane. This is exactly the case as the mask and the wafer are locked on a single assembly. The all-reflective optics mean there are no color aberrations and the entire spectrum of the illumination source may be utilized. Narrow band filters are not needed thereby avoiding the substantial light loss and interference effects caused by the filters.
The High Performance Condenser system HPC pictured in Figure 2 supplies uniform, intense ultraviolet and visible illumination to the projection optics. A high pressure mercury lamp is imaged on a slit that controls the width of the field of the projection optics. The lamp energy passes through an aspheric corrector, which is a lens with a reflective coating on half of the back surface and is reimaged by the reflective portion of the aspheric lens onto the primary mirror. The aspheric lens acts as a secondary mirror and superimposes a 7.5x magnified image of the mercury lamp onto a 1.0 mm slit.
The energy then passes through the slit to a torroid mirror that acts as a very strong field lens and via one flat fold mirror images the energy onto an aperture. The aperture permits simultaneous variation of energy throughput and cone angle of illumination. There exists the inherent trade-off between better resolution (cone angle) and exposure dose (energy throughput). After the stop, the energy is imaged onto the mask plane via a fold and a relay mirror. The HPC assembly also contains an actinic filter used to block the UV radiation when viewing the wafer for alignment, and a light-sensitive diode for monitoring the mercury lamp intensity and internally adjusting the carriage speed to maintain a given exposure.

Although the carriage speed controls the exposure dose, it is desirable to know the actual exposure dose in units of mJ/cm², a fairly standard unit in any literature research or data collection. Since the exposure is a scanning slit mechanism, the irradiance had to be collected and integrated along the slit and the wafer surface. The detector is a photovoltaic cell that converts input photons to electric pulses. These pulses are then sent to the integrating radiometer which has a built-in sensitivity of 2.36E-3 amp*cm/watt. The radiometer sums the pulses, and thus the input photons over a small time constant, and the result is a measure of amp*secs. The amp*secs are then divided by the sensitivity factor to arrive at the irradiance in watts/cm². The total exposure is equal to the integration of the output current and can be found by dividing the radiometer output current amp*secs by the sensitivity factor amp*cm²/watt.

The collected data will be used as input for PROSIM, a Perkin-Elmer resist profile simulation. The calculation by PROSIM requires three steps: Image, Rate, and Develop. Image requires exposure device characteristics in order to generate an aerial image output. Rate requires the input of remaining resist thickness vs. time in the developer (Perkin-Elmer DREAMS software) to produce the dissolution rate vs. depth for each incident exposure. The thickness vs. time data is generated via DREAMS which uses interferometry measurements during development to record signal strength during development time. Develop needs the Image and Rate outputs to arrive at the final simulated resist profiles.

The goal of this research work was to develop an in-line method of measuring the total exposure dose in milli-joules per square centimeter, and then to use this data to successfully model profiles in the resist exposed with the Perkin-Elmer Model 140 scanners.

**EXPERIMENT**

A wafer vacuum chuck for the Perkin-Elmer 140 Projection Aligner was modified to hold a radiometer detector head, as depicted in Figure 3. An International Light model XR140A collector with an additional neutral density of 2.0 was used in conjunction with an IL700A integrating radiometer to measure the exposure dose for scan speeds ranging from 10 to 999. The addition of the neutral density filter was necessary to avoid
saturation of the integrating radiometer and to prevent
photo-multiplication in the collector. A relationship between
the scan speed and the exposure dose was established. This data
was used in the subsequent processing and modeling of Shipley
1400-27 and KTI 820 resist films on four inch silicon wafers.

Ten four inch wafers were cleaned using the RCA process.
The wafers were then primed with HMDS spun on at 4000 rpm for 20
secs and coated with either Shipley 1400-27 or KTI 820 resists
dynamically dispensed at 500 rpm for 5 secs and then ramped up to
a final spin speed of 5000 rpm for 20 secs. The resultant 1 um
resist films were then prebaked in a convection oven at 95 C for
20 mins. These wafers were processed through the Perkin-Elmer
Model 140 Projection Aligner and then developed in a beaker. The
Shipley resist was developed in diluted Microposit 351 and the
KTI resist was developed in diluted KTI 934, both of varying
concentrations. The process was then optimized for each resist
using image critical dimension measurements of line/space pairs
and SEM analysis. The Perkin-Elmer scanner was operated in the
manual mode and one is referred to the operation manual for the
actual procedure.

The PROSIM model was performed to set up the aerial image
using the scanner device parameters which were a numerical
aperture of 0.17, a partial coherency factor of 0.6, a
illumination wavelength of 436 nm, and a defocus distance of 2.0
um.

![Figure 3: Modified Wafer Chuck and Integrating Radiometer](image)

RESULTS

The relationship between the scan speed and the exposure
dose was found to be non-linear with doses ranging from 530mW/cm
down to 5.2mW/cm. The data is shown in Figure 4. The
correlation is repeatable and exposure doses can be predicted to
within 5% of actual using the linear relationship obtained on a
log plot, shown in figure 5. The resolution capabilities using the scanner were found to be 1.4μm for the Shipley 1400-27, and 1.6μm for the KTI 820. Both resists were capable of resolving finer geometries but without any linewidth control, as evidenced in Figure 6. Optimum Processing for the Shipley resist included exposure at a scan speed of 50 and development in 351 developer diluted 4:1 (DI:dev) for 25 seconds. The KTI 820 was exposed at a scan speed of 65 and developed in KTI 934 developer diluted 4:3 (DI:dev) for 25 seconds. The PROSIM image profile, shown in Figure 7 was set up and can be used for resist profile simulation.

![Figure 4: Exposure Dose vs Scan Speed](image)

![Figure 5: Log Exposure Dose vs. Log Scan Speed](image)

![Figure 6: SEM of Resist Profile](image)

![Figure 7: Scanner Aerial Image](image)
CONCLUSIONS

Three goals were achieved with this work. The scan speed was correlated to exposure dose with 5% accuracy for the Perkin-Elmer Model 140 Projection Aligner. The process parameters were set up for both the Shipley 1400-27 and the KTI 820 resists. Thirdly, the scanner aerial image was successfully modeled via PROSIM.

ACKNOWLEDGEMENTS

Scott Blondell for his invaluable work on the detector mount and his help with getting the projection aligner up and running.

REFERENCES


DESIGN OF A 4-BIT PMOS PARALLEL COMPARATOR A/D CONVERTER

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ABSTRACT

This project dealt with the design of a 4-bit PMOS parallel comparator analog-to-digital converter. Using a predesigned comparator circuit, the rest of the logic was completed. Circuit analysis was performed using SPICE simulation. Circuit layout was done using Integrated Circuit Editor (ICE). The PMOS process consists of four masking levels: diffusion, thin oxide, contact cuts, and metal.

INTRODUCTION

There are various circuits to accomplish A/D conversion, some of which are parallel-comparator, successive-approximation, digital ramp, and integrating A/D converters. The parallel or flash converter was chosen for this project since it is the simplest and fastest of all of the other types. The disadvantage of this type of converter is the complexity of the hardware. Since the number of comparators needed is $2^N - 1$, where $N$ is the desired number of bits, the number of comparators doubles for each added bit.[1]

Figure 1 shows the basic architecture of a 4-bit parallel A/D converter. The number of comparators and reference levels needed is 15 and 16, respectively. The analog signal voltage, $V_a$, is fed one input of each of the comparators simultaneously. The other input is connected to a reference voltage, $V_{ref}$. The voltage reference is tiered down into equal steps through the resistor ladder. The output of the voltage comparators will be low for all those whose $V_{ref}$ is greater than $V_a$, and high for those which is smaller than $V_a$.[2] Figure 2 shows the output states of the voltage comparator.

The segment detection logic circuit, refer to Figure 1, is used to simplify the design of the encoder. It consists of fourteen 2-input NOR gates where one input is the output of one of the comparators, and the other is the inverted output of the comparator below it. The logic symbol, Boolean expression, truth table, and circuit design are shown in Figure 3.
Figure 1. Basic Architecture of a 4-Bit A/D Converter
THE advantage of the segment detection logic is that only one segment output will be high at a time since the output of the NOR gate is high only when both inputs are low. This in turn will make the design of the encoder easier.[1]

The encoder design consists of eight NOR gates where four of them have four inputs and the rest have three inputs. The outputs of each two adjacent 4-input and 3-input NORs are fed into another NOR gate whose output correspond to a certain bit. The digital output generated by the encoder corresponds to a certain bit. The input of each of the eight NOR gates is taken in the following manner: A binary code is assigned to the output of the segment detection logic from (0001 - 1110) where the left most number corresponds to MSB and the right most to LSB. If LSB is equal to 0, then the output is fed to the first and second NOR gates of the encoder, while if the MSB is equal to 0 then the output is fed to the seventh and eighth NOR gates.

\[
\begin{array}{c|c|c}
A & B & Q \\
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 0 \\
\end{array}
\]

Figure 3. Logic symbol, Boolean expression, and Truth table of a NOR gate

EXPERIMENT

SPICE simulation was used to analyze the subcomponents of the A/D converter circuit. These include the comparator circuit and the NOR gates. The transistor model used in these simulations is the following:

- Substrate doping = 1.2e15 /CC
- Oxide thickness = 700 Angstroms
- Channel Length Modulation = 0.02 /V
- Surface Mobility = 200 sq-cm/V-S
- Junction Depth = 2 Microns
- Surface State Density = 8E11 /sq-cm
- Source and Drain Resistance = 100 OHMS
- Gate to Source Capacitance = 3.45 nF
- Gate to Drain Capacitance = 3.45 nF
- Gate to Substrate Capacitance = 1.38 nF
- Junction Capacitance = 98.6 uF
The circuit layout was performed using the Integrated Circuit Editor (ICE).

RESULTS/DISCUSSION

The PMOS circuit used in the comparator is basically a differential amplifier with the inverting input tied to the analog input. The differential amplifier is designed to use two inverters with the source of their drivers coupled and driven by a current source, as shown in Figure 4. The ratio of the pull-up to pull-down of the inverters is 400:1 for optimum gain. The current source was designed to supply 9.06 microamps and has an output impedance of 86 Kohms. SPICE simulation shows that the comparator circuit works for reference voltages from 0 to -10 volts and will convert an analog signal into a digital output with a resolution of 0.16 volts. The simulation of the NOR gates shows that the gates have a rise time of 24 nanoseconds. The ratio of the pull-up to the pull-down of the NOR used was 16:1. Figure 5 shows the schematic of a NOR gate with one inverted input.

The final chip design covers an area of 4700x3200 microns and the circuit uses 225 transistors.

CONCLUSION

A PMOS A/D converter was designed and laid out using 10 microns design rules. This design is fully compatible with RIT's present maskmaking and fabrication capabilities.
REFERENCES:


FABRICATION OF A SINGLE LEVEL METAL CCD SHIFT REGISTER

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ABSTRACT

Using a "shadow mask" technique, a single level metal 3-phase CCD shift register was fabricated with electrode separations of 2 microns. Testing is pending at this time.

INTRODUCTION

A Charge-Coupled Device, or CCD, is essentially a linear array of closely spaced MOS capacitors. A three phase CCD shift register is realized by terminating such an array with a diode at each end (to inject and detect minority carriers), and connecting every third gate to a common conductor. A cross section of a three phase CCD shift register is shown in Figure 1.

Figure 1: Cross section of a three phase CCD shift register.[1]

Consider such a device fabricated on a P-type substrate. When a large positive voltage is present on the first electrode in the array, a depletion region is formed in the underlying silicon, temporarily creating a potential well for electrons, as shown in Figure 2a. Electrons injected from the input diode accumulate in the potential well formed under the electrode. If a positive voltage is simultaneously applied to an adjacent electrode, the potential wells overlap and any charge stored under the first electrode is now shared between the two, as shown in Figure 2b (hence the term "charge-coupled"). It follows that when the bias is removed from the first electrode, the charge is transferred completely under the second, as shown in Figures 2c and 2d. A similar transfer moves the packet of charge under the third electrode. When the electrodes are pulsed with overlapping clock pulses, as shown in Figure 2e, a moving array of potential wells is established. In this fashion, packets of electrons supplied from the input diode are shifted sequentially through the device, to be detected at the output diode.
The potential wells do not last indefinitely, and eventually, thermally generated electrons fill the well completely. Thus the CCD is a dynamic device, in which charge may be stored for times shorter than the thermal relaxation time of the capacitors. This time varies from one second to several minutes, depending on the processing.

Critical to the operation of the device is spacing the electrodes close enough so that their depletion regions overlap. If they do not overlap no charge-coupling takes place and the device fails. For transfer efficiencies compatible with today's technology, this spacing must be less than three microns[2], which presented a problem. Silver halide masks are currently employed at RIT and as a result the current minimum feature size restriction is ten microns. This restriction was overcome by employing a "shadow-mask" technique developed by Browne and Perkins.[3,4] The technique involves defining every other electrode in the array with photoresist on a thick layer of aluminum. The metal is then etched to clear, and carefully overetched, producing an overhang structure. A second thinner layer of metal is deposited over the entire wafer. By virtue of the overhang, solvent access to the photoresist is guaranteed and the unwanted metal over the resist is lifted off in an ultrasonic acetone soak. The remaining device features are defined in a subsequent photoresist application. The result is a linear array of electrodes, with the separations between them determined by the degree of overetch. Using this technique it is possible to fabricate single level metal structures with spacings as close as one half of a micron. This lower limit is imposed to allow for possible lateral surface migration of aluminum during the second metal deposition, which could short the device. An outline of this technique is shown in Figure 3.
The device fabricated was an 8-bit three phase CCD, and therefore has 24 transfer electrodes, plus 4 electrodes for the input/output. The transfer electrodes are 250 by 40 microns and are contacted through diffused buses. A P-type substrate was chosen for two reasons. First, in a P-type substrate the minority carriers are electrons, which have higher mobility than holes and should therefore result in higher transfer efficiencies. Second, for a silicon dioxide insulator on P-type substrate the fixed charge held near the surface is positive and the silicon at the interface is held in depletion even at zero volts bias, again improving the efficiency of the device. The transfer channel was surrounded by a P-type channel-stop diffusion. The resulting high majority carrier density prevents the formation of a depletion region of any significant width, creating a surface potential wall around the transfer channel. This serves to laterally confine the direction of charge transfer, and electrically isolate the device.

**EXPERIMENT**

Fabrication commenced with the growth 5000 angstrom masking oxide on a P<100> 14-22 -cm substrate at 1100C in wet O2 for one hour. Windows were opened in the oxide and boron was diffused using Allied B150 spin-on dopant source to define the P-type channel-stop. The masking oxide was removed and again regrown to 5000 angstroms and windows opened to define the input/output diodes, as well as the phase one, two and three clock buses. Phosphorous was diffused into these regions using Emulsitone N-250 spin-on dopant source. The oxide was again stripped and a 700 angstrom gate oxide was grown at 1100C in dry O2 for 25 minutes, through which contact cuts were opened. The wafer was coated with a thick layer of aluminum, and using the shadow mask technique, the electrode structure was fabricated. Figure 4 displays the five mask levels.
LEVEL 1: P-type channel stop.  LEVEL 2: Diode and clock bus.

LEVEL 3: Contact Cuts.  LEVEL 4: Every other electrode.

LEVEL 5: Remaining device features.  An overlay of all levels.

Figure 4: Masking levels for single level metal CCD.

RESULTS/DISCUSSION

Figure 5a shows a micrograph of the completed device, 5b a closer view using darkfield illumination, and 5c displays a close-up of the electrode structure, also using dark field. Using the "shadow-mask" technique, electrode separations of approximately two microns were obtained for a three and half minute time to clear and a one minute overetch. Yield was very high for this process step. Subsequent attempts may obtain closer spacing using a shorter overetch time.
Electrodes are 40 microns wide, separation 2 microns.

Figure 5a: A close-up of the electrode structure.

Figure 5b: A closer view using darkfield illumination.

Figure 5c: The completed device.
CONCLUSIONS

An 8-bit three phase single level CCD shift register with 2 micron separation between electrodes was successfully fabricated using the "shadow-mask" technique.

ACKNOWLEDGEMENTS

Scott Blondell for assistance with equipment difficulties, Dr. Lynn Fuller and Carl Conrad for after hour access to lab, Dr. Mike Jackson for obtaining supplies.

REFERENCES


SOFTWARE ANALYSIS OF CAPACITANCE–VOLTAGE MEASUREMENTS

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ABSTRACT

A computer program called CVPLOT, used at RIT to aid in the analysis of metal–oxide–semiconductor (MOS) capacitors, was recoded from REGIS graphics into the VAX Graphical Kernel System (GKS) allowing the user to obtain hardcopy plots of high and low frequency capacitance voltage curves from an HP–Plotter, LNO3 Laser Printer, and LA100 Line Printer. The revised program also allows changes to be made in the values of the ‘non–ideal’ (a nonzero flatband shift) parameters while subsequently observing the shift in the curve as a result of these changes. Curves for three different values of either substrate doping, gate oxide thickness, or temperature may also be superimposed on the same graph.

INTRODUCTION

The capacitance–voltage (C–V) measurement is one of the most important techniques utilized in the analysis of the metal–oxide–semiconductor (MOS) structure. Information such as the threshold voltage, flatband voltage, oxide capacitance, oxide thickness, substrate doping, mobile ion concentration, distribution of surface states, and minority carrier lifetimes may be obtained to characterize both materials and the processing sequence.

A menu–driven in–house computer program called CVPLOT models capacitance voltage measurements for MOS capacitors based upon input entered from the terminal. Theoretical high and low frequency ‘ideal’ and ‘non–ideal’ (a nonzero flatband voltage shift) capacitance voltage curves can be displayed on the computer screen as well as superimposing experimental curves on the same graph. These theoretical curves are generated from the exact charge analysis theory for the MOS capacitor located in Reference 1. The program was limited in that the only method of obtaining a hardcopy output was through a screen dump to a graphics line printer.

The purpose of this project was to revise the existing CVPLOT program by expanding its capabilities in the following ways: to give the user the ability to direct the output to any of the following devices: computer screen, HP–Plotter, LA100 Line Printer, or the LNO3 Laser Printer; to permit defaults of commonly used RIT values for gate oxide thickness, gate area, temperature,
and substrate doping to be easily input during the execution of the program; and to allow for changes in Phims (nonzero metal/semiconductor workfunction difference), Qf (fixed oxide charge), and Qm (mobile oxide charge) during the running of the program while subsequently observing the shift in the 'non-ideal' curve on the screen as a result of these new values. Another goal was to superimpose 'ideal' C-V curves for three different values of either gate oxide thickness, substrate doping or temperature. The ultimate purpose was to improve the software tool available to the student for the analysis of capacitance voltage measurements.

PROGRAMMING

The graphic routines of the CVPLLOT program were recoded from REGIS[2] graphics into the GKS[2,3] graphics format (see Appendix A for the programs). Figure 1 is a block diagram of the original CVPLLOT program containing a description for each subroutine.

To implement the above changes, revisions were made to: the calling program, CVPLLOT.FOR, and subroutines PLOTSUB.FOR, and CVSUB.FOR. In addition, two subroutines were added to the program, COPYSUB.FOR and HP TRUNCATE.PAS. COPYSUB.FOR creates the output data files used for obtaining hardcopies of the results seen on the screen based upon the variables sent to it from CVPLLOT.FOR. Problems developed in obtaining output on the HP-Plotter from the HP.DAT file created in COPYSUB.FOR. When this file was created, each line exceeded 80 characters resulting in arbitrary carriage returns and form feeds being injected into the file. To correct this, a subroutine called HP TRUNCATE.PAS was written in Pascal which takes the HP-Plotter Tile (HP.DAT) and reformats the strings to 80 characters per line so that they may be successfully plotted.

![Figure 1: Block diagram for the original CVPLLOT program.](image-url)
One aspect of the recoding is that all of the output had to be transformed into graphics mode. This means that real numbers needed to be converted into character strings that could be handled by the graphics package. This was accomplished using a VAX Run-Time Library Routine called OTS$CNVOUT[4] which converted real numbers into character text in exponential notation. The data sheet for OTS$CNVOUT is included in Appendix B.

The revised CVPLOT program, which retains the original name, may be accessed from the following run command for VAX/VMS:

$RUN USER:[MICROLIB.TOOLS.CV]CVPLOT

where MICROLIB is the computer account in the microelectronic engineering department where the program resides. The user may desire to place the following command line in a LOGIN.COM file to eliminate having to repeatedly type the previous run command:

$CVPLOT:==RUN USER:[MICROLIB.TOOLS.CV]CVPLOT

By typing just CVPLOT at the dollar ($) prompt the program will be executed. Once in the program, the user chooses from the main menu the option to create 'ideal,' multivariable, or 'non-ideal' C-V curves. If the 'ideal' or multivariable route is chosen, then data is input in response to prompts at the computer terminal and the output is displayed on the screen. Next, the user has the option to create a hardcopy output file or return to the main menu.

If the 'non-ideal' path is chosen, values are again input and the graph is displayed. Next, the user has the option to change the 'non-ideal' parameters, i.e. Phims, Qf, or Qm. These changes may be executed as many times as desired, but if a hardcopy output is finally chosen then the last input values will be used to create the output plot. An 'ideal' curve may be created through the 'non-ideal' path by entering zeros for the non-idealities, and then changes may be made to the 'non-ideal' parameters. In this way, the user can observe the shifting of the 'ideal' curve in response to the effect of the non-idealities. When a hardcopy output is chosen, a file is placed in the users directory containing the appropriate data for that particular chosen output device. Table 1 gives the filename.extension that is placed in the users directory,

<table>
<thead>
<tr>
<th>Chosen Output Device</th>
<th>Filename</th>
</tr>
</thead>
<tbody>
<tr>
<td>HP-PLOTTER</td>
<td>HP.DAT</td>
</tr>
<tr>
<td>LN03 LASER PRINTER</td>
<td>LASER.DAT</td>
</tr>
<tr>
<td>LA100 LINE PRINTER</td>
<td>LA100.DAT</td>
</tr>
</tbody>
</table>

Table 1: Listing of filename.ext placed in users directory from the CVPLOT program.
RESULTS

Figure 2 outlines the block diagram of the revised CVPLOT program with the two previously mentioned subroutines. Figure 3 is an example of a normalized 'ideal' curve output to the LN03 Laser Printer. Figure 4 illustrates an 'ideal' graph output on the HP-Plotter for three different values of substrate doping. Figure 5 demonstrates the combination of a 'non-ideal' shifted curve with experimental data (dashed curve) plotted on the LA100 Line Printer. Notice that when an 'ideal' low frequency curve is plotted, the threshold voltage is also extracted for either the high or low frequency experimental data curve. This plot only uses the experimental data for demonstration purposes and no relationship between the two curves is intended.

CONCLUSION

The revised CVPLOT Program is fully operational at this time. Hardcopy output can be obtained from the HP-Plotter, LN03 Laser Printer and the LA100 Line Printer. Suggestions for further work include modifying the COPYSUB.FOR routine to allow plotting of 'ideal' and 'non-ideal' curves on the same graph. This is only available now through the screen dump. The effects of sintering on the curves along with calculations for the interface trap density are future enhancements that would be of great benefit.
Figure 3: Ideal low frequency C-V curve from an LNO3 Laser Printer.

Figure 4: Ideal high frequency curves for three values of substrate doping output from an HP-Plotter.
Figure 5: Non-ideal low frequency curve with experimental data curve output from an LA100 Line Printer.

ACKNOWLEDGMENTS

The author would like to acknowledge the help of Steve Wilkins of the RIT User Computer Center for his assistance with GKS graphics, Mike Young, computer lab assistant with the UCC for his HP-TRUNCATE.PAS subroutine, Robert Pearson for help on deciphering his original CVPLOT program, and Mike Jackson for continued support.

REFERENCES


[2] Copyright Digital Equipment Corporation


THICKNESS MEASUREMENTS USING PRISM COUPLING

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ABSTRACT

A HeNe laser and a 45-90 degree prism with an index of refraction of 1.51 were used to study the prism coupling method of determining the thickness and index of refraction of thin films. This project involved the design and construction of a set-up that allowed for simple adjustment of the incident angle of the light. Based on the available prism, SiO2 films were testable.

INTRODUCTION

It is possible to very accurately determine the thickness and index of refraction of a thin film by using a prism coupler. A typical system is shown in Figure 1. This is accomplished by placing a prism in close proximity to the thin film that is to be measured. A monochromatic beam is incident on one face of the prism. Normally there is almost total internal reflection at the interface between the bottom of the prism and the air gap that exists between the prism and thin film. However, a small field will exist at the interface and reach outside of the prism. This field is called an evanescent field and it decays exponentially to zero within a few wavelengths. If the air gap is made small enough, (on the order of one half to one wavelength of the light) the evanescent field will extend into the thin film. If the horizontal component of the evanescent field (i.e. the component
parallel to the interface) is equal to one of the modes of the thin film waveguide, light will couple into the film. Furthermore, if this condition is met, the light propagating in the film will combine constructively with light entering the film further away. This will cause more of the incoming light to be coupled into the film. The net result will be a significant amount of light traversing the air gap and propagating horizontally inside the thin film.

It is possible to adjust the horizontal component of the evanescent field by adjusting the incident angle of the laser. If the intensity of the light coming out of prism is measured, there will be a drop in intensity at the angles of theta where this coupling occurs. These angles are called mode angles, and are characteristic of the film’s index of refraction and thickness. If the intensity of the reflected beam is plotted as a function of the angle of incidence, a plot similar to the one shown in Figure 2 would be expected. If two or more of these mode angles are obtained, the index and thickness of the film can be calculated using the following equations:

\[ k \omega (n^2 - Nm^2) = m\pi + \phi_0(n,Nm) + \phi_2(n,Nm) \]  \hspace{1cm} (1)

where \( \phi_n(n,Nm) = \arctan \left( \frac{n^{2l}}{(Nm^2 - nj^2)} \right) \)  \hspace{1cm} (2)

Figure 2. Intensity (I) of Reflected Light VS. Angle of Incidence (\( \theta \)) [1]
where the subscript \( j \) is 0 for substrate parameters
\( j \) is 2 for air gap parameters

\( W \) is film thickness
\( n \) is index of refraction of the film
\( m \) is mode number
\( k \) is propagation constant in free space of the light used \( (k = \frac{\omega}{c}) \)
\( \omega \) is angular frequency of the light
\( c \) is speed of light
\( N_m \) is propagation constant of mode \( m \) in the film \( (N_m = n_p \sin \theta_m) \)
\( n_p \) is index of refraction of the prism
\( \theta_m \) is mode angle for mode \( m \)
\( \gamma \) is the polarization of the mode: \( \gamma = 0 \) for TE polarization
\( \gamma = 1 \) for TM polarization

This project involved the design and construction of a preliminary test apparatus to investigate this phenomena for silicon dioxide films.

**EXPERIMENTAL**

A Helium-Neon laser with wavelength of 6328 angstroms was used as an incident light source. A right angle prism with index of refraction of 1.51 provided the necessary coupling medium. The set-up, shown in Figure 3, was constructed. The laser is stationary, the thin film/prism apparatus pivots so that it is possible to adjust the angle of incidence, and the photodetector must be moved to collect the reflected wave. The wafer slides into the slot and is held in place by the vacuum (not shown). The shelf supports the prism. The clamp can be adjusted to vary the pressure (and thus the air gap distance) between the prism and thin film. The intensity of the reflected light was recorded by hand and plotted as a function of the incident angle.

![Figure 3. Prism Coupler Test Set-up](image-url)
RESULTS/DISCUSSION

A plot of the intensity of reflected light versus the angle of incidence can be seen in Figure 4. This data was obtained from a wafer that had 5000 angstroms of oxide and an index of refraction of 1.46. Clearly, this plot lacks the mode angles that are so prevalent in Figure 2. The angle of incidence is limited to +6 and -20 degrees due to the physical make-up of the apparatus. If we increase the angle past +6 degrees, the light enters the prism and strikes the prism/air gap interface at an angle that does not exceed the critical angle needed for total internal reflection. The light will enter the thin film regardless of its thickness and index of refraction. If we increase the angle past -20 degrees, it becomes impossible to collect the reflected light due to the size of the detector.

Figure 4. Results for a Silicon Dioxide Film

The reason that no mode angles were observed could be the result of several factors. The small difference in the index of refraction between the film and prism makes it crucial to have the correct air gap spacing. This however is impossible to measure and it is necessary to rely on trial and error. Several different pressures between the prism and film were tried with similar results. Another possible reason why no mode angles were observed is decoupling of the light back into the prism. Once the coupled light propagates past the incident laser beam it may decouple back into the prism if the prism and film remain in close proximity. It may be necessary to separate the prism and film after the point where the laser strikes the interface. Finally, it may be possible that the silicon dioxide film that was tested was too thin to support more than one mode angle. If the only mode angle that was supported falls outside the limitations of the apparatus, no mode angles would be observed.
CONCLUSIONS

The set-up that was designed and constructed allowed for easy and accurate measurements of the reflected intensity versus incident angle. Some limitations on the measurable angles of incidence were observed due to the size and location of the detector. The use of an equilateral prism will increase the total range of incident angles that can be measured. Mode angles were not observed due to decoupling of the coupled light, the prism had too low of an index of refraction, or the film was too thin. This technique would be better suited for measuring the thickness of photoresist. This would be possible if an equilateral prism with a sufficiently high index of refraction were used.

ACKNOWLEDGEMENTS

Mr. Lechner of the Optics Department for helping me measure the index of refraction of numerous prisms, Joe Hahn for helping me construct the set-up, Scott Blondell for helping me modify the set-up, and M. Jackson for making several valuable design suggestions.

REFERENCES


IMPLEMENTATION OF A CONTROLLABLE PROCESS FOR THE RIE ETCHING OF SiO2 AT RIT

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ABSTRACT

An Electrotech Plasmafab 425 reactor was brought on line to perform reactive ion etching (RIE). Samples of SiO2 over Si were etched. Results show 400 angstroms/minute using a combination of freon 23 and oxygen as the etchant with good visual uniformity. A selectivity of 6:1 for SiO2:Si was achieved.

INTRODUCTION

The reactive ion etching of SiO2 maintains an important position in the microelectronics industry. As device features shrink in size it becomes increasingly important to perform etching with a high degree of anisotropy. Anisotropy is defined as preferential etching in the vertical rather than the horizontal direction and can be calculated as:

\[ A = \frac{2D}{(L-W)} \]

Where \( A \) is the degree of anisotropy, \( d \) is the thickness of the film in nanometers, \( L \) is the width of the top etched image in nanometers and \( W \) is the width of the original photoresist image. [1] During wet processing a high degree of lateral undercutting is seen. RIE processing, however, yields a greater degree of anisotropy enabling the fabrication of smaller geometry devices. Table 1 shows a comparison of the bias achieved through wet and dry etching. Bias refers to the amount of lateral loss of sidewall material beyond the edge of the resist.

Table 1: Etch Bias During Pattern Transfer [2]

<table>
<thead>
<tr>
<th>Thickness of Material</th>
<th>Wet Bias</th>
<th>Dry Bias</th>
</tr>
</thead>
<tbody>
<tr>
<td>5000A</td>
<td>.4um</td>
<td>.1um</td>
</tr>
<tr>
<td>10000A</td>
<td>1.0um</td>
<td>.3um</td>
</tr>
<tr>
<td>17000A</td>
<td>5.0um</td>
<td>.4um</td>
</tr>
</tbody>
</table>

As can be seen, a dry etch process provides some very desirable results. In addition to this anisotropy, a dry process, with its small amount of gas disposal, provides a secondary advantage in that large quantities of dangerous acids and solvents do not have to disposed of.
When implementing a plasma etching process there are some very important parameters that need consideration, not the least of which is selectivity. This refers to the preferential etching of one film with respect to another and can be expressed as:

$$S = \frac{R_a}{R_b}$$

Where $S$ is the selectivity, $R_a$ is the etch rate of film 1 and $R_b$ is the etch rate of film 2. Maintaining a selectivity greater than 10 is usually desired to minimize damage to the underlying material.

A related parameter is the degree of resist mask erosion. The mask material most commonly used being photoresist, it is essential that the resist mask be extremely impervious to the effects of the etch. To insure that the resist mask maintains its integrity throughout the process the following steps can be taken:

a) increase resist thickness
b) optimize postbake time and temperature
c) use a plasma pretreatment process such as that in PRIST (Plasma Resist Image STabilization).

If the resist experiences severe degradation unwanted resist etching or liftoff can occur causing unreliable pattern transfer and failed devices.

For a process to be effective the etch rates of S102 must be uniform across the entire wafer surface as well as from wafer to wafer. Uniformity refers to variations in the etch rate and can be quantified as follows:

$$U = \frac{(R_{max} - R_{min})}{(2Rav)}$$

Where $U$ is the uniformity and $R$ is the etch rate measured at 5 equally spaced points across the wafer. [1]

When processing with a plasma a problem results from radiation damage. Deep level traps can be induced which can cause degradation of minority carrier generation time thus increasing junction leakage currents and decreasing capacitor charge retention times. Threshold voltage shifts can be caused by the increase in interfacial sites and also a degradation in transconductance occurs for MOS devices. The generation of ions by the plasma can form an additional trapping layer on the surface of the wafer. Reducing these effects is very important to device performance. With the use of CHF3 as the etchant a polymer layer is formed during the etch which acts as a protective layer on the chamber walls and minimizes sputtered contamination yielding a lower concentration of interface states. Hydrogen in the discharge also ties up Si dangling bonds and reduces the number of defects. A 600°C anneal in forming gas can serve to reduce the threshold shifts and an HF dip after processing is useful in repairing the damaged wafer surface. [3]
The term plasma is used to describe a partially ionized gas containing electrons, both positive and negative ions, and various neutral species. A glow discharge is a self-sustaining plasma in the pressure range from 7.5 mtorr to 5.6 torr. For RIE etching, the pressure is usually maintained under 100 mtorr. The electron density in a plasma used for etching is generally between $10^{8}$ and $10^{12}$ cm$^{-3}$. Under a constant electric field, the electrons present between the electrodes are accelerated toward the positive electrode (anode). During their travel, these electrons can transfer energy to the various neutral species present through collisions. Depending upon the magnitude of the energy transferred, the collision can either fully ionize the neutral species or just excite an electron to a higher energy state from which it subsequently relaxes giving the characteristic glow of the glow discharge. When full ionization occurs, the products of the collision include another electron which can then be accelerated toward the anode with the possibility of gaining enough energy from the electric field to perform more energy transfer and a positive ion which is accelerated toward the negative electrode (cathode). This positive ion, upon impact with the cathode, can cause secondary electron emission which is required for the successful sustaining of the plasma. Secondary electrons generated in this manner can initiate a cascade effect thus helping to create a stable plasma where generation of electrons and ions is balanced by the loss to the electrodes and the diffusion out of the plasma. A major drawback of a DC system is the inability to etch insulators such as SiO$_2$. The need for conducting electrodes negates the possibility of etching an insulator since the plasma cannot be sustained. As the secondary electrons are emitted from the insulator, there can be no current flow through the insulator to replace the lost electrons so a positive charge builds up and the discharge is extinguished. A solution to this problem is to use an RF alternating field in place of the DC system.

With the change to alternating fields, there is little difference in the plasma provided the frequency of the field remains low enough that the ions can be swept out of the discharge in a single cycle of the applied voltage. If this ion cutoff frequency (50KHz to 2MHz) is exceeded then the secondary ion emission is not the primary source of electrons anymore. The electrons are now generated by the ionizing collisions. For normal plasma operation, an electron in the plasma oscillates with the field and undergoes collisions with the larger particles present. These collisions result in a random motion and the electric field does work on the electron in trying to restore it to ordered motion thus giving it a higher energy and a higher probability of undergoing ionizing collisions. The ions do not gain a high amount of energy due to their great mass and lower mobility. Therefore RF discharges require lower field strengths and they do not require conducting electrodes making the etching of insulators possible. To perform etching a gas is introduced.
into the chamber and ionized to form reaction products which upon interaction with the film form volatile products which can be desorbed and swept out of the chamber. [4] [5]

EXPERIMENTAL

In order to begin process testing it was necessary to commission an Electrotech Plasmafab 425 reactor. After this was completed the etch tests were begun. A 4000 angstrom film of SiO2 was grown in wet O2 @ 1000 C for 80 min. An ellipsometer was used for thickness measurements. For a test of pattern transfer an RIT capacitor mask was used to pattern different size squares into 1.2 microns of Kodak 820 positive photoresist. This was postbaked at 140 C for 2 minutes. An Alpha Step surface profilometer was employed to determine etched step heights and, in conjunction with the ellipsometer data, etch rates and selectivity were calculated. An argon preclean was employed to degas the chamber and condition the resist. CHF3 was used as the etch gas in conjunction with O2 in a 16:1 ratio. An argon postclean was also utilized to clean the wafer and to remove any residual adsorbed halogens from the wafer surface. After much experimentation with flow rates and power the following process was arrived at.

<table>
<thead>
<tr>
<th>Step</th>
<th>Gas</th>
<th>Flow Rate (sccm)</th>
<th>RF Power*</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Argon</td>
<td>24</td>
<td>2A</td>
<td>2 min</td>
</tr>
<tr>
<td>2</td>
<td>CHF3</td>
<td>80 (16:1)</td>
<td>2A</td>
<td>var</td>
</tr>
<tr>
<td></td>
<td>O2</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Argon</td>
<td>24</td>
<td>2A</td>
<td>2 min</td>
</tr>
</tbody>
</table>

* RF power was measured in amps, not watts, on the Plasmafab

RESULTS/DISCUSSION

The etch rate of SiO2 was determined to be approximately 400 angstroms/minute with a selectivity of greater than 6:1 for SiO2:Si. Uniformity across the wafer was not measured but it was dramatically increased when the wafer table was stationary as opposed to rotating.

The reactions that are believed to occur with CHF3 are as follows:

\[
\text{CHF}_3 + \text{e}^- \rightarrow \text{CHF}_3 + \text{H} + \text{e}^- \quad \text{(most probable reaction)}
\]

\[
\rightarrow \text{CF}_3^+ + \text{H} + 2\text{e}^-
\]

\[
\rightarrow \text{CF}_2 + \text{HF} + \text{e}^-
\]

\[
\rightarrow \text{CF}_2^+ + \text{HF} + 2\text{e}^-
\]

\[
\text{CHF}_3 + \text{e}^- \rightarrow \text{CHF}_2 + \text{F} + \text{e}^- \quad \text{(not probable due to higher heat of reaction)}
\]
CHF3 plasmas produce CF3 and CF2 ions for etching but virtually no free fluorine due to the scavenging effect of the free fluorine producing HF which does not contribute to the etch. The positive ion bombardment causes lattice damage creating active sites at which reactions can proceed at an accelerated rate. When SiO2 is etched in the presence of hydrogen the hydrogen promotes formation of a polymer layer which reduces the Si etch rate and thereby increases the selectivity. Polymer formation occurs both on the walls of the etched profile and the bottom. The impinging ions continually erode the layer at the bottom leaving sites open for etching. The sides however, are not subject to the ion bombardment and the polymer layer inhibits the etch.

CONCLUSION

The major thrust of the project was to bring the reactor up and to develop a process for utilizing RIE of SiO2 at RIT. This was accomplished in a very rudimentary manner due to time constraints. There can be much more experimentation done to further qualify the process and to develop processes for the etching of other films such as polysilicon, nitrides, and aluminum now that the reactor has been brought on line.

ACKNOWLEDGEMENTS

I would like to thank Scott Blondell for his invaluable help with recommissioning the reactor.

REFERENCES


ADVANCED MASK MAKING AT RIT

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ABSTRACT

This project involved the definition of the steps necessary to generate a mask or reticle for any of the three exposure tools (i.e. GCA 10X G-line Stepper, Perkin Elmer Scanning Aligners, and Kasper Contact Aligners) used at RIT. Next a working process for creating chrome masks for the Perkin Elmer Scanners was developed. Using the process outlined in this paper 5 micron line widths can be repeatedly obtained.

INTRODUCTION

A method for creating accurate, high quality masks is needed to reduce minimum dimensions of devices made at RIT to below 10 microns. This can be accomplished by going to masks made of chrome instead of emulsion. Though emulsion masks have the advantage of the ease of processing and relative low cost, they unfortunately suffer from poor linewidth control and lack of durability. Emulsion films are made of small grains and its these grains that limit your resolution to approximately 10 microns. For the 10x reticles used in steppers these limits are acceptable. But for contact printing and the Perkin Elmer scanners, a one to one mask is needed with dimensions approaching three (3) microns. For this the emulsion is inadequate, therefore the need for chrome masks is obvious.

With chrome masks the resolution needs of 3 microns at RIT can be met. Chrome masks have better resolution because of its different method of imaging it. Photoresist is used to transfer the image into the chrome as compared to directly imaging the emulsion masks. A chrome system starts with a quartz plate which can be of varied size and thickness. The plates for the Perkin Elmer Model 240 Scanners are 5"x5" and 90 mils thick. Chrome is then deposited on the plate by either sputtering or evaporation techniques. Normally the thickness of the chrome is less than 2000 angstroms but not so thin as to have pinholes. The chrome is then coated with some type of photoresist. This resist is spun on very thin (between 0.3 - 0.5 microns) so as to obtain the best possible resolution. Chrome is very reflective and can degrade your image because of reflections off the surface. These problems can be minimized by using low reflective chrome or using an anti-reflective coating in combination with the photoresist. This system is then exposed with the desired pattern and developed accordingly for the resist type used. The pattern is then transferred by etching the chrome, usually with a Ceric Ammonium Nitrate solution. The resist is then stripped and the
mask carefully inspected for any pinholes or other defects.

In the VLSI industry, chrome masks and reticles are the standard. Because of the increased demand for high precision and low defect density masks, optical methods for creating these masks has become inadequate. The use of electron beam lithography is now industry wide. Although the electron beam tools have excellent precision and very high resolution (on the order of 0.2 microns), there are some drawbacks. Electron beam exposure tools are very costly, usually in the millions of dollars. This expensive tool also needs strictly controlled environmental and physical conditions maintained. The housing to achieve these controls can also cost millions of dollars. Aside from the large capital cost, the electron beam imaging system is very slow. It could take many hours to expose just a single mask. These drawbacks are accepted in order to obtain the high quality masks and reticles needed in today's semiconductor industry.

This project included two parts which were as follows:

(1) First a flowchart which follows through every step of mask making for the three different exposure tools at RIT, (i.e. GCA 10x Stepper, Perkin Elmer Scanning Aligners, and the Kasper Contact Aligners) was generated for both emulsion and chrome.

(2) A process was devised to create chrome masks and then used to create masks for the Perkin Elmer Scanner.

EXPERIMENT

The basic assumption is that all masks start with MANN 3000 files created with ICE[*] layout software. These files will be used by a Mann 3000 pattern generator to create a 10X reticle. Referring to Figure [1]. Processing beyond this point depends on the end result desired. This is as far as the reticles for the GCA stepper need to go because it is a 10X reduction tool. Now the image is in emulsion and it needs to be reversed because emulsion is a negative tone imaging system. (i.e. it becomes opaque when light strikes it.) The photoresist is positive tone so the mask itself must be positive tone. This can be done with a simple chemical reversal process after exposure. A chrome reticle could then be created by contact printing from emulsion to the photoresist on the chrome plate.

The next alternative is to reduce the image to 1X. This is accomplished on the photorepeater. The photorepeater will step and repeat the image of the circuit across the entire photosensitive plate. This is called a mask.

[*] ICE - Integrated Circuit Editor is a CAD tool available to students at RIT through the Microelectronics Department
FIGURE 1. MASK MAKING FLOW CHART
To create an emulsion mask take the reticle created on the pattern generator and use it directly on the photorepeater. The negative tone of the reticle will be reversed again because of the emulsion film. After the development and fixing of the emulsion film the mask is ready to use. This process works for both the Perkin Elmer and Kasper aligners NOTE: The Kaspers use 4" plates while the Perkin Elmers use 5" plates.

Making chrome masks is slightly different. The 10X reticle is created on the pattern generator as before, but instead of normal processing the image must be reversed. This is because the photoresist on the chrome plates is positive and therefore the image must be 'turned around' before using the photorepeater. The photoresist is sensitive to UV light so the chrome masks must be exposed on Photorepeater #2 which is in Mask Making #2. This photorepeater is equipped with a mercury vapor lamp which gives UV illumination. Expose as you would an emulsion mask.

The path that was chosen to demonstrate the chrome mask process was that for creating chrome masks for the Perkin Elmer 120 Scanning Aligner. The plates that were used were from Electronic Materials Corporation.

The plates were quartz 5"x5"x0.09"
12% reflective chrome 0.1 microns
Microposit 1450-017 0.5 microns
positive photoresist

Turn on lamp in photorepeater #2 (needs at least 20 minutes to warm up and stabilize). Next the intensity of the lamp needs to be measured. Place the plate holder (without the plate in it) on the platen of the photorepeater and slide out the cover shield. Move the platen so that it is underneath the lens. Place the sensor of the IL440 radiometer on the holder underneath the lens. Be sure to use the washer with the small hole on the sensor to achieve the best possible accuracy. The ratio of the areas of the sensor and the washer is 4.86. (i.e. take the reading with the washer in place and multiply that reading by 4.86 to get the true measurement.) Open shutter manually to take the reading. Check the focus and make sure it is set for the particular holder being used. (The chart for focus and holders is in Mask Making #1 on the controller for the photorepeater). The settings for the 4" plates is well documented in a logbook for photorepeaters. The settings for the 5" plates were as follows:

<table>
<thead>
<tr>
<th>Setting</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exposure spacing</td>
<td>0.200</td>
</tr>
<tr>
<td>Row spacing</td>
<td>0.200</td>
</tr>
<tr>
<td>Number of Rows</td>
<td>18</td>
</tr>
<tr>
<td>Exposures/Row</td>
<td>18</td>
</tr>
<tr>
<td>X-starting point</td>
<td>5</td>
</tr>
<tr>
<td>Y-starting point</td>
<td>5</td>
</tr>
</tbody>
</table>

NOTE: The controller used for the mercury lamp shutter is on top of the console.
Mount the plate in the holder. (Note: These plates are white light sensitive so all work must be done in red light.) The shutter must be timed and set by hand. The markings on the timer are meaningless. Adjust the time of exposure accordingly. After the exposure is complete, remove the plate from the platen and secure it in a light tight box. Transfer it into the wet chemical across from Photolithography area #2 in the clean room. The rest of the processing will be accomplished here.

RESULTS/DISCUSSION

The following process was found to yield linewidths of 5 microns repeatedly.

Exposure desired 35 - 40 mJ/cm²

Develop the plate in Microposit 351 positive resist developer.

Diluted (2:1) (water:developer)
Room temperature (20°C)
Time - 90 seconds
Rinse and inspect

Post bake the resist prior to etching

Bake Temperature - 90°C
Bake Time - 30 minutes

Etch the chrome plate (Ceric Ammonium Nitrate solution)

Chrome Etchant Type 1020
Etch Time - 60 seconds
Room Temperature - (20°C)
Rinse and Blow dry
Inspect

Strip the photoresist

acetone soak - 10 minute
Inspect for scumming

CONCLUSIONS/SUMMARY

A process for generating 5 micron lines on chrome has been developed. With some refinement of this problem linewidths of 3 microns could be attained.

ACKNOWLEDGMENTS

My thanks go out to Scott Blondell for making the machines work. And thanks to Mike Jackson for the instruction, and thanks to Shaun Francomacaro for giving me the drive to 'get the job done.'
This project developed a test chip designed to standardize the testing requirements and characterize bipolar, PMOS and CMOS processes at Rochester Institute of Technology. The common process monitors were designed to test resistivity, opens and shorts, contact resistance and capacitance. The photolithographic monitors were designed to test image resolution and alignment. Process specific discrete devices were designed to test parametrics and leakage currents. The test chip dies were primarily designed to be inserted onto the mask to eliminate the need for process monitors on each die and secondly, to periodically monitor the performance of a student run integrated circuit factory.

INTRODUCTION

A student run integrated circuit factory processes a significant quantity of wafers each quarter. The wafers are predominately manufactured using either bipolar or PMOS processes. Presently, the wafers are tested and characterized based on the student's individually designed test structures. Statistical data would then be collected from the wafers by testing each die. A test die that would standardize some common process monitors could be implemented and integrated into student's projects for extraction of process data. In addition, the test die could be used exclusively on a wafer as a monitor of the health of the factory.

The design of the test die should include monitors for the bipolar and PMOS processes. With the advent of a polysilicon gate CMOS process, additional process monitors will be required. Each process will have a dedicated test die mask set. The test dies will occupy a 4000 m x 4000 m area and the process monitors will be built on common 2x6 probe pads. The test dies will allow for additions of new test devices.

The test dies will include a variety of photolithographic monitors, process monitors and electrical tests, each of which will be implemented onto the three dies for the parameters that require monitoring. The photolithographic parameters of interest include image alignment and image resolution. Process parameters that require monitoring include capacitance, opens and shorts,
resistivity, linewidth variations, minimum resolvable contacts, contact resistance and contact chain yield. Electrical structures will be used to monitor parameterics and leakage currents.

**TEST DIE LAYOUT**

The test dies were generated in ICE (Integrated Circuit Editor) which is an in house CAD package used for the layout of the test monitors. The common (*) monitors to all three of the test dies are:

* Alignment marks
* Alignment verniers
* Resolution targets
* Serps/Combs
* Contact holes
* Contact chain
* Van der Pauws
* Linewidths
* Resistors

The specific monitors for each process are:

### Bipolar Test Die
- Big contact vertical NPN
- Normal vertical NPN
- Lateral PNP
- Diode
- I2L structure

### PMOS Test Die
- Capacitors
- 1/3 gate
- NOR gate
- NAND gate

### CMOS Test Die
- Capacitors

The structures and their intended purpose follow:

- **Alignment marks**...to aid aligning to previous mask.
- **Alignment verniers**...to check alignment to previous mask down to 1 m.
- **Resolution targets**...to determine minimum resolvable lines and spaces.
- **Serps/Combs**...to determine opens/shorts in metal.
- **Contact holes**...to determine the minimum resolvable contact hole.
- **Contact chain**...to determine yield on contacts between 1st metal and diffusion.
- **Van der Pauws**...to determine sheet resistance of diffusions or implants.
- **Linewidths**...use with van der Pauws to determine linewidth variation in diffusions.
- **Resistors**...to measure direct resistance.
- **Big contact vertical NPN**...to determine hfe before metal.
- **Normal vertical NPN**...to determine transistor parameters.
- **Lateral PNP**...to determine the effects of lateral junctions.
- **Diode**...to determine diode parameters.
- **I2L structure**...RS flip flop and D flip flop to determine functionality.
- **1/3 gate**...to determine MOS parameters with a L/W ratio of 1/3.
- **NOR gate**...to determine MOS functionality.
- **NAND gate**...to determine MOS functionality.
Table 1 is a summary of the actual layout and a brief description of the monitor.

Figure 1
GCA MANN Stepper and Kasper/Perkin Elmer alignment targets

Figure 2
Alignment verniers

Figure 3
Resolution targets [4]
2, 4, 6, 8, 10um lines/spaces

Figure 4
Capacitors MOS devices
800, 600, 400, 200um square

Figure 5
Serp/Comb structure
5, 10, 15um lines/spaces [4]
Table 1 (cont.)

Figure 6
12L structure - RS Flip Flop and D Flip Flop

Figure 7
3, 5, 7, 10, 12, 15μm contact hole test structure [4] with 20x20μm contact resistance structure [4]

Figure 8
Contact chain [2] with Diode, Large NPN, Normal NPN and Lateral PNP
Table 1 (cont.)

Figure 9
P-diffusion
100x100um and 60x60um
Van der Pauws [3] and
Linewidth structure [4]

Figure 10
N-diffusion
100x100um and 60x60um
Van der Pauws [3] and
Linewidth structure [4]

Figure 11
Metal Linewidth structure [4]
with P-diffusion resistors and
L/W of 1/3 PMOS transistor

Figure 12
PMOS NOR and NAND gates
with L/W of 1/3 for the
driver transistors
RESULTS/DISCUSSION

The focus of this project was to put together the most used process monitors onto one test die per process. The details on the theory of process monitor design can be found in the references. The CMOS process was defined by senior William J. Brocklehurst and was chosen to be used in the test mask design for the CMOS test die. The Bipolar and PMOS processes are the standard processes defined as of May 1988. While I attempted to include as many monitors on each die as possible, some had to be left out because of space limitations. Re-evaluation of the test dies should be made periodically to discard unused monitors and to implement new ones. As a recommendation, the serp/comb structure should be reduced in size on the CMOS test die to allow room for some of the other monitors.

CONCLUSION

The Bipolar, PMOS and CMOS test die designs are complete. They are ready to be made into MANN files and mask reticles. Each of the monitors specified above are in a separate symbol file with a descriptive filename.

REFERENCES


A DESIGN TOOL SOFTWARE INTERFACE

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ABSTRACT

Currently, the Integrated Circuit Editor (ICE), a CAD I.C. design tool used for layouts at RIT, lacks any design rule checking simulation capabilities. This project involved writing a program that would translate the output file from ICE in the CalTech Intermediate Format (CIF) into a format that would be readable by other software tools, such as design rule checking and circuit node extraction programs.

INTRODUCTION

The Integrated Circuit Editor (ICE) is an in-house CAD package used to layout I.C. designs at RIT. ICE stores the designs in the CalTech Intermediate Format (CIF) file structure. This file structure is set up to define the process layers and the individual components within each layer. The components are defined as grouped sequences of boxes along with scaling factors and positional information. [1] A sample CIF file is shown in Figure 1.

```
Comment ICE cif version 1.0;
DS 4 100/1;
   L OXIDE;
   Box 950 950 280,280;
DF;
DS 2 100/1;
   L CC;
   Box 950 950 220,220;
DF;
```

Figure 1: Sample CIF file.

The "rasterizer" program transposes the component symbols into a two-dimensional array that represents the original design when it was laid out in ICE. [2] The preliminary version of the program will work strictly for 1900 um² designs. Since the design rule for the RIT PMOS process is ten microns minimum geometry, then the design will be divided by ten to get 10 um² pixels. The user will be required to layout the design on ten micron boundaries.

Each cell or pixel in the array holds eight bits (one byte) of information and represents ten square microns. The individual
layers are encoded into the byte by designating each bit as one of the PMOS process layers. Since there are only four layers used in the current RIT PMOS process (diffusion, oxide, contact cuts and metal) then there are four unused bits in each pixel. Figure 2 shows the bits set for the four process steps and the bits left for future expansion.

```
msb         lsb
7 6 5 4 3 2 1 0
```

![Figure 2: Process layer bit mapping.](image)

The program will prompt the user for the CIF file to be converted and will translate the CIF commands in the following manner. If a LAYER command is found, a variable within the program will be set to the value to say three, which indicates that the current layer is OXIDE. If a BOX command is found, the size and position of the box is stored and the box is then placed into an array that will contain the overall design. This array is dimensioned as 190 X 190 bytes with each byte representing 10 um². This process is shown in Figure 3.

```
--------
--------
LAYER OXIDE --> layer = 3 (oxide)
--------
bit 3 will be set for
--------
each pixel set
--------
Box 950 950 200,200 -->
```

![Figure 3: Interpreting the CIF file lines.](image)
PROGRAM DESCRIPTION

The program is laid out to accept a CIF file name from the user and then opens the file for input. The CIF file is then scanned line by line for commands. When a command line is intercepted, it is interpreted to determine which command the line represents (i.e. LAYER or BOX command). If the line is a BOX command, then the position and size of the box is used to place the box into an array at the appropriate process layer. Once all the lines have been scanned and the end of file is detected, the array is written out to a second file named "RASTER.OUT". If any errors are encountered, they will be reported and the program will terminate.

RESULTS/DISCUSSION

The program name is RASTER.EXE and is executed on the VAX system by typing "RUN RASTER.EXE". The program prompts the user for a CIF file name and scans the file for CIF commands. The individual components in the original design are a series of boxes and are written into an array. Once all the boxes have been put into the array, it is written out to a file called "RASTER.OUT" in hexadecimal format. This file can then be read by design rule checking and node extractor programs to further check the I.C. design. Any errors detected will be reported to the user and the program will terminate. A sample output representing several process layers within the design is shown in Figure 5.
CONCLUSION

A program was written to aid the design process at RIT. The interface will fill a void between the ICE package and current design rule checking software. This will help designers check their I.C. designs for layout errors and also facilitate the use of future software packages. The design process has been enhanced with powerful error checking software as well as providing the designer with confidence that the designs are electrically correct. The problem of having to remake masks after errors are discovered during the processing stages has been eliminated.

ACKNOWLEDGMENTS

I would like to thank Rob Pearson for suggesting this project and helping me layout the groundwork for the preliminary designs. Mike Jackson was great at providing a layman's look at software design and helped a lot in the revisions of this paper. Carl Conrad worked with me in the standardization of the output file format and the definition of understanding the term "lessons in futility on the RIT VAX".

REFERENCES


AN INTEGRATED APPROACH TO POSITIVE RESIST DEVELOPMENT CHARACTERIZATION

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ABSTRACT

This paper investigates Neureuther and co-workers development model of positive novolak-type photoresist systems in aqueous alkaline developers. A measurement system for determining the exposure and development model parameters is described. The dissolution rates for two developer solutions have been examined and the impact of the developer differences on resist profiles is illustrated. The dissolution rate of resist in metal ion free developer at various temperatures is investigated.

INTRODUCTION

Simulation is a well-established and essential tool in the design of integrated circuits. In the case of photolithography, accurate models and sets of parameters are required for various resists, developers, and processing conditions. Dill, et al. proposed the first models for exposure and development of positive photoresist [1].

The state of positive photoresist during exposure is described in terms of the normalized concentration of the inhibitor $M(x,t)$, which is the fraction of inhibitor remaining (at any depth in resist, $x$, and exposure time, $t$) as compared to the inhibitor concentration before exposure. The function $M(x,t)$ depends on the optical resist parameters $A$, difference in absorption between bleached and unbleached resist; $B$, absorption of fully bleached resist; and $C$, the rate of change of the resist absorption. Since there is little scattering in most photoresist film, the absorption constant, $\alpha$, can be expressed using Lambert-Beer Law.

$$\alpha = A M(x,t) + B$$ (1)

The total absorption of the photoresist film reduces as exposure converts the inhibitor to reaction products. For a positive photoresist:

$$\frac{dI(x,t)}{dx} = -I(x,t)\alpha$$ (2)

where $I(x,t)$ is light intensity at any depth ($x$) and time ($t$) in the resist.
The rate of destruction of the inhibitor is dependent on the local optical intensity \( I(x,t) \), the local inhibitor concentration, and \( C \), as given by:

\[
\frac{dM}{dt} = -I(x,t)M(x,t)C
\]  

Equations 2, and 3 are subject to the following initial conditions:

\[
M(x,0) = 1 \\
I(x,0) = I_0 \exp[-(A+B)x]
\]

and boundary conditions:

\[
I(0,t) = I_0 \text{ (constant lamp intensity)} \\
M(0,t) = \exp(-I_0Ct)
\]

One should note that equations 2 and 3 are coupled differential equations, and in order to determine \( I(x,t) \) and \( M(x,t) \), these equations must be solved by numerical integration techniques, once the values for \( A, B, C, \) and \( I_0 \) are known.

The values of \( A, B, \) and \( C \) are dependent on exposure wavelength. Techniques for measurement of these parameters have been described in detail by several authors [1-2]. The internal transmittance, \( T \), of a photoresist film on a matched substrate is expressed as:

\[
T(t) = \exp[-\int_0^d \alpha(x) \, dx]
\]  

where \( d \) is the thickness of the resist film. Equation 4 may be used to derive relationships between the optical resist parameters and the optical transmittance of a resist film. These relationships are:

\[
A = \frac{1}{d} \ln\frac{T(\infty)}{T(0)} \]  

\[
B = -\left(\frac{1}{d}\right) \ln T(\infty) \]  

\[
C = \frac{(A+B)/A}{1/T(0)[1/T(0)\frac{dT(0)/dt}]} \]  

Figure 1 represents a typical apparatus for measuring transmittance of a resist film. A glass substrate with the same index of refraction as the photoresist is utilized. This minimizes the reflection from the resist-glass interface. The other end of the glass substrate is coated with anti-reflection coating (MgF2) to minimize the reflection from glass-air interface.

In the resist development model of Dill, et al., development of positive photoresist is considered as a surface-rate limited etching reaction. The parameters that control this rate are resist and developer chemistry. Dill, et al. defined the development behavior as a log-polynomial function of inhibitor concentration with parameters \( E_1, E_2, \) and \( E_3 \) describing the polynomial:

\[
\text{Rate}(M) = \exp \left( E_1 + E_2 M(x) + E_3 M(x)^2 \right)
\]
However, this polynomial fails at high exposure dose. Also, with a significant surface induction effect (the retardation of dissolution rate near the surface compared to the dissolution rate in the bulk), it is necessary to include the depth dependence of development rate in the model.

A model proposed by Neureuther and co-workers includes the retardation of the development rate near the surface, and this is used as a multiplier $f(x,M)$ to the bulk development rate $R_b(M)$ [2].

$$\text{Rate}(x,M) = f(x,M)R_b(M)$$

(6)

In this product formulation, the depth dependence is independent of $M$, thus, $f(x,M)$ can be separated into individual functions of $x$ and $M$.

The bulk development may be viewed as the dissolution of base resin modified by the presence of photoactive compound, inhibitor, (PAC; $M$), and the dissolution of base resin modified by presence of reacted photoactive compound (carboxylic acid; 1-$M$). In order to combine these two dissolution process, Neureuther derived the following form for the rate function $R$

$$1/R = F_1(M)/R_1 + F_2(M)/R_2$$

(7)

The parameters $R_1$, and $R_2$ are the limiting rates for fully exposed and unexposed resist, respectively. In Equation 7, the first term is associated with resin-carboxylic acid, and the second with resin-PAC dissolutions. The suitable forms for $F_1(M)$
and $F_2(M)$ are given by

$$F_1(M) = 1 - \exp(-R_3(1-M))$$
$$F_2(M) = -\exp(-R_3(1-M))$$

$R_3$ is a sensitivity parameter which is a measure of how fast the development rate increases as the exposure increases. The combination of Equations 7, 8, and 9 gives

$$R = 1 / R_1(1-\exp(-R_3(1-M))) + R_2\exp(-R_3(1-M))$$

Equation 10 describes the bulk development rate over the full range of exposure from $M=0$ to $M=1$.

The development rate near the surface is described by the product of the bulk rate and a multiplier $F(x,M)$. This function is depended on both exposure and depth, and may be written as

$$F(x,M) = 1 - (1-F(0,M)\exp(-x/R_4))$$

where $x$ is the depth into the resist, $R_4$ is the characteristic retardation depth, and $F(0,M)$ is the ratio of surface development rate to bulk development rate at any $M$ value. Neureuther modeled $F(0,M)$ as a simple linear function of $M$

$$F(0,M) = R_5 - (R_5-R_6)M$$

where $R_5$ is the ratio of surface rate to bulk rate at $M=0$ and $R_6$ the ratio at $M=1$.

This project was an attempt to obtain optical resist parameters for $M(x,t)$ determination, and positive resist dissolution rate, $R(x)$.

**EXPERIMENT**

The apparatus shown in Figure 1 was modified for measuring transmittance of photoresist film due to unavailability of glass substrate with index of refraction of 1.65 and anti-reflection coating. Instead, a glass slide with index of refraction of 1.50 was utilized as the substrate with no anti-reflection coating. The resist was spun at 4000 rpm for 30 seconds and prebaked at 70°C for 20 minutes in a convection oven. Monochromatic light (436nm) was used to expose the resist film, and the intensity transmitted through the resist film and the substrate was measured using a radiometer.

The Perkin-Elmer Development Rate Monitor (DRM), model 5900, was used to obtain the dissolution rate of the photoresist. The exposed samples were developed at 20°C, with constant agitation. During development, photoresist thickness as function of development time was monitored by the DRM.

Several numerical integration techniques were examined to solve equations 2 and 3 for $M(x,t)$ and $I(x,t)$. Due to the
complexity of these equations, no solution was found.

RESULTS/DISCUSSION

Table 1 shows both the experimental and literature values of A, B, and C for AZ1350J-SF and KT1820. Figure 2 shows a typical optical transmittance plot for AZ1350J-SF positive photoresist film. Equations 4A, 4B, and 4C have been used to determine A, B, and C values. Due to the absence of a glass substrate with index of refraction of 1.65 and the anti-reflection coating, the values obtained differ from the literature. In addition, problems have been encountered in solving the equations 2 and 3 to determine the inhibitor concentration. Thus, the development rate was not characterized as function of inhibitor concentration.

<table>
<thead>
<tr>
<th>TABLE 1 : A,B,C Exposure Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Prebake 80\degree C, 25min;Exposed for 436nm)</td>
</tr>
<tr>
<td>Photoresist</td>
</tr>
<tr>
<td>AZ 1350J-SF</td>
</tr>
<tr>
<td>(Reported Values)</td>
</tr>
</tbody>
</table>

| Photoresist | A \(\text{um}^{-1}\) | B \(\text{um}^{-1}\) | C \(\text{sec}^{-1}\) |
| KT1820 | 0.665 | 0.062 | 0.089 |
| (Reported Values) | 0.510 | 0.031 | 0.013mJ/cm\(^2\) |

Figure 2: Optical transmittance of a 1.3um film of AZ1350J-SF resist as a function of exposure time.
Figure 3 shows the dissolution rate as a function of depth for AZ1350J-SF, obtained from the DRM. The development rate retardation near the surface of photoresist, addressed in the Neureuther development model, is apparent.

Shipley 1400-27 positive photoresist has been characterized under various processing conditions. The simulated exposure condition uses a lens with NA=0.28, sigma=0.7, and wavelength of 436 nanometers. The dissolution rates for Shipley MF312, and MF319 developers are compared in Figure 4. MF312 developer showed superior contrast and sensitivity but at the expense of a higher unexposed development rate. The exposure doses were adjusted to yield a 1 micrometer linewidth. The effect of development temperature on resist profile is shown in Figure 5. The development of metal ion free developer unexpectedly decreases with increasing temperature.

Due to the complexity of solving equations 2 and 3, the development rate behavior was not characterized as a function of the inhibitor concentration.

Figure 3: Dissolution rate of AZ1350J-SF as a function of the thickness.
Figure 4: Simulation of resist profiles of Shipley 1400-27 resist for 2 different developers. Doses are indicated by ( ) in mj/cm².

*DOSES ARE INDICATED BY ( ) IN mj/cm².

Figure 5: Simulation of resist profiles of Shipley 1400-27 for several developer temperatures.

EXPOSURE : 135 mj/cm²
DEVELOPMENT TIME : 185 seconds
CONCLUSION

An accurate development model of positive novolak-type photoresist systems in aqueous alkaline developers was reviewed. The measurement system for determining the exposure and development model parameters was described. The dissolution rates for Shipley MF319 and MF312 developers had been examined and the impact of the developer differences on resist profiles was exhibited. The dissolution rate of resist in metal ion free developer (MF312) at various temperatures was investigated.

As mentioned earlier, due to the complexity of solving equations 2 and 3, the development rate was not characterized as a function of the inhibitor concentration. By solving the equations 2 and 3 in the future, a complete characterization of positive photoresist development can be accomplished. Understanding the behavior of resist dissolution is very essential for improving a photolithographic process.

ACKNOWLEDGMENTS

I would like to thank Mr. Mike Jackson, Dr. Robert Clark, and Mr. Paul Whalen for their support of the project.

REFERENCES


TIME DEPENDENCE OF HOT ELECTRON INDUCED SURFACE STATES

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ABSTRACT

Hot electron injection was investigated using the HP 4145B SPA to induce Fowler- Nordheim tunneling. High frequency and quasi-static capacitance-voltage (C-V) measurements were taken on p-substrate MOS capacitors in order to generate the distribution of surface states throughout the band gap. The results proved inconclusive with no deformation of the low frequency C-V technique being observed.

INTRODUCTION

The density of interfacial traps (also called surface states or interface states) throughout the band gap of a metal/Si02/Si (MOS) capacitor can be modulated by hot electron injection through the thin gate oxide. It has been shown [1] that the distribution of surface states, created in the above manner, will vary as a function of the time elapsed since the injection.

Ideally in metal/oxide/semiconductor (MOS) structures the conductance of the Silicon Dioxide (SiO2) is considered to be negligible until the voltage across the oxide is greater than its dielectric strength. In this circumstance the conductance dramatically increases and the oxide loses its insulating property. In real MOS structure, however, current flow is possible before breakdown under conditions of heightened electric field or temperature. This is possible due to quantum theory which allows for a finite probability of finding a particle outside of the classically forbidden potential well. This probability increases monotonically with increased energy. When the probability is high, i.e. when a particle has enough energy, it is possible for it to travel between potential wells in the lattice, as is shown in Figure 1. This process is called tunneling. [3]
In a metal gate MOS capacitor the induced tunneling involves electrons moving through the potential barrier between the metal fermi energy and the insulator conducting band. This process, as stated above, requires the electrons to be at energies quite larger than thermal equilibrium hence the term "Hot" electrons. The high energy electrons passing through the oxide have been shown [4],[5],[6] to effect the density of surface states at the oxide-semiconductor interface. Surface states are defined as allowed energy states in which electrons are localized (trapped) in the vicinity of a materials surface. These states introduce energy levels throughout the forbidden band gap, as shown in Figure 2. The interaction of a state with an electron results in the state becoming charged and so affecting the charge distribution in the device and, thereby, device performance. The effect upon the charge distribution is a function of the gate bias.

Surface states are, to a first approximation, filled when located below the fermi energy and the empty when above it. The gate bias serves to modulate the position of the fermi energy throughout the band gap and hence also the status of the surface states. This is illustrated in Figure 3. A further complication is that the interfacial states have different charge properties depending upon their location in the band gap. Traps with energies above mid gap are acceptor like - negatively charge when filled, neutral when empty. Traps with energies below midgap are donor like - neutral when filled, positively charge when empty.

![Figure 2: Interfacial Traps in the Band Gap. From Ref.[3]](image)

The dependence of device performance on the internal charge distribution and its dependence, in turn, on the density and location in the band gap of surface states, makes an accurate determination of the surface distribution throughout the band gap extremely important. The required determination, fully described in ref [2], involves using values obtained from high frequency C-V measurements and measured quantities such as oxide thickness to determine Cox,Cdep,etc. The distribution of surface states is obtained by integrating the quasi-static C-V curve.

Figure 4 shows expected low frequency C-V curves prior to, immediately after, and 32 hours after hot electron injection. The change in surface state distribution after injection manifests itself as a deformation of the quasi-static C-V curve.
As shown, the distribution of surface states changes as a function of time after injection.

![Figure 3 Trap Filling As a Function of Bias](image)

a) Inversion b) Depletion c) Accumulation

From Ref. [3]

![Figure 4 Expected Results. From Ref. [1]](image)

This project was an initial attempt to observe the effects of Hot Electron injection to the surface state distribution of P-substrate MOS capacitors. The Hot carriers will be forced using a constant current source and the effects determined via the high and low frequency capacitance-voltage technique.

**EXPERIMENTAL**

The MOS capacitors used in this experiment were p-type with an acceptor doping of 6.2E14 cm3, and oxide thickness of 900A, and an area of 10.3E-3 cm2. Fowler-Nordheim tunnel injection was produced using an HP4154B Semiconductor parameter analyzer in constant current mode. The current densities forced ranged from 6.0 E-6 A/cm2 to 1.7E-4 A/cm2. A positive gate bias was used. Since the injection mechanism occurs from the substrate to oxide, the device was illuminated to insure a sufficient supply of the minority electrons. Both high frequency and quasi-static C-V measurements were made immediately prior to and after injection, as well as, at appropriate intervals thereafter.
RESULTS/DISCUSSION

The high frequency and quasistatic CV measurements taken just prior to injection are presented in Figure 5 and 6 respectively. Note the similarity between Cmin and Cmax values for the high and low frequency curves. This would suggest the low frequency measurement is an accurate one. The results after injection, however, do not conform to what was expected. No change in the low frequency curves was noted for any of the input current densities, except for the highest densities which produced breakdown of the gate oxide.

The lack of results for this experiment, in light of the published results, is not immediately obvious. The first step in attempting to evaluate this problem would be to investigate the low frequency C-V technique used. According to reference 2, in order to obtain the true low frequency curve, it is necessary that during the measurement the structure, remain in thermal equilibrium. When this is the case, the measured capacitance contains the total response of the interface states, i.e. the system is sensitive enough to detect change in surface density. The method proposed to determine the relative sensitivity of the low frequency technique involve, first, theoretically determining and plotting the time constants of electron exchange between surface states and the valence and conduction bands as a function of surface potential. These curves are then compared to a plot of the rate of change of the surface potential with respect to time as a function of surface potential. The criterion which the relationship between these three curves has to satisfy to result in a "true" low frequency curve is discussed in detail in the reference.

CONCLUSION

Hot electron injection of P type MOS capacitors produced no measurable change in surface state distribution. This was not as expected or predicted by references [1],[4],[5], and [6]. It is recommended that the low frequency C-V technique used to determine the surface state distribution be investigated to determine its relative sensitivity to changes in surface state density.
ACKNOWLEDGEMENTS

My thanks to Rob Pearson for assisting me with the low frequency C-V measurements and to Mike Jackson for his help and guidance.

REFERENCES


HIAC/ROYCO PARTICLE COUNTER INSTALLATION

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ABSTRACT

A HIAC/ROYCO particle monitoring system is being installed to monitor aerosols in the RIT clean room. The system is controlled by a VAX mainframe computer using a Fortran program to read the data from the counter process it and write it to an output file. This file is used to generate control charts monitoring the particle levels at several locations in the cleanroom workspace.

INTRODUCTION

HIAC/ROYCO particle counting systems are capable of sampling either a liquid or gaseous medium. The pump in the model 1100 aerosol sensor draws the gas from the location being sampled through the model 160/161 ten port scanner into the sensing unit. The gas flow rate is approximately 1.0 $\pm$ 0.5 cubic feet per minute. The sensing unit contains an optical sensor which is used to detect particles in the gas stream. The unit is capable of detecting up to 300,000 particles per cubic foot with the sizes ranging upward from .5 micrometers.

The sensing unit creates a data signal which the model 4150A system control unit uses to produce count data. The count data can be broken down into six particle size ranges called channels. These channels have an associated size threshold that is preset at the factory and which varies from unit to unit. A typical distribution of the channel threshold levels is shown in Table 1. When in cumulative mode, each channel counts all particles larger than the threshold. In differential mode each channel counts particles between the two adjacent thresholds. It is capable of manual, timed or volume controlled sample modes. The system control unit has an RS232 interface allowing external computer control.

<table>
<thead>
<tr>
<th>CHANNEL</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>THRESHOLD</td>
<td>.5um</td>
<td>1.5um</td>
<td>3.0um</td>
<td>5.0um</td>
<td>10.0um</td>
<td>15.0um</td>
</tr>
</tbody>
</table>
This project involved setting up the system as shown in Figure 1 and writing a Fortran program so that the number of particles in the RIT clean room air could be monitored by this system automatically. The results from each count are written to a data file which is used to update a statistical control chart.

HIAC/ROYCO

PARTICLE COUNTING SYSTEM

Figure 1
EXPERIMENTAL

A Fortran program was written on the VAX to set up the necessary particle counter parameters. The more significant values include the upper and lower count levels, the air flow stabilization time, and the sample time. It then initiates a count, and receives the count data. The program converts the data from character to integer format and calculates the number of particles per cubic foot of air from the gas flow rate, gas flow time, and the number of particles counted in the sample. The date and time the sample was taken is written along with the count to a data file unique to each port location.

Figure 2 is a block diagram of the program with a full flow chart given in Appendix A. Commands are issued so that data is passed from the particle counter to the VAX and from the VAX to the particle counter in the communications set up block. There are eleven parameters used to set up the particle counter in the parameter setup block. The Fortran program converts the data, after a sample is taken, from character format to number format in the sample block. The data is written to an output file that is unique to each location in the cleanroom. After the communications are reset the alarms are written to the computer terminal.
RESULTS/DISCUSSION

The Fortran program sets up the particle counter, initiates a count, processes the data, and writes it to a separate data file for each different location in the cleanroom. It takes samples from each port every half hour until 6:00 in the evening.

RIT has six of these individual particle monitoring systems. A multicom munications port has been received that can be used control all of the six of these systems. One of improvements that can be made to the program is to implement control of all six systems using the new communications port.

Another improvement that could be made is to write the alarms that are written out at the end of the program into a file so that they can be retrieved for later review.

ACKNOWLEDGEMENTS

First I would like to thank Fairchild Corporation for donating the system to RIT. I would like to thank Rob Pearson for his help in configuring the system and Carl Conrad for his expert programing advice.
REDESIGN OF AN EIGHT-BIT, ECL DAC TO FACILITATE
SPEED AND FUNCTIONALITY TESTING OF A BI-CMOS PROCESS

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ABSTRACT

The redesign and layout of a clocked eight-bit digital to analog converter using emitter coupled logic is examined based on testing of the original circuit, simulation of ground node resistance and pinout compatibility to a produced part. The completed layout is subjectively compared to the original circuit design. Production and evaluation is pending at this time.

INTRODUCTION

ECL is an acronym for Emitter Coupled Logic, a high performance bipolar logic family. ECL is used for maximum speed without regard for power consumption. The layout is area consuming and not conducive to operating with large logic arrays because a typical gate requires seven to nine transistors and five to six resistors whereas the same gate in CMOS can be accomplished with two transistors. As the main virtue of ECL is performance and speed, it is typically biased at the maximum limits of the process, since performance increases with power consumption. ECL is capable of much greater performance than CMOS, however CMOS has a great advantage in density and power consumption on average. Even though the per stage power consumption of CMOS is increasing, taken as a whole there is a significant amount of time where gates remain static for several clock cycles where CMOS power consumption is nearly zero.

Bi-CMOS is a developmental process scheme that combines both bipolar and CMOS onto a single integrated circuit. One such process being developed at National Semiconductor uses the modular approach where CMOS is the baseline. The Bipolar transistor module was initially developed with a test pattern that in addition to parameter monitoring structures and Delay line circuits, incorporated a functional circuit designed in ECL, the DAC.

ECL itself is a current switching logic that is complementary in nature, where performance is maintained by running the maximum current per stage without saturating the differential pair. What this implies is that a large current is always flowing in two of the three branches of the typical logic gate. This is true because when one side of the circuit is off the remaining side has the current flowing.
Using the gate shown above in Figure 1 for discussion, the branch current Is is set by Dv where:

$$I_s = \frac{Dv - Vbe}{R_c}.$$  \hspace{1cm} (1)

This is both the controlling current that is switched and the level selecting current in the output stages. Vx, an internal node to the circuit, has its voltage controlled by which branch the current flow is in. The low logic level, VxL is the voltage at node x when the current is flowing:

$$VxL = (Vcc - I_s \times R_l).$$  \hspace{1cm} (2)

The other case is when the current is not flowing and the high logic level, VxH, exists:

$$VxH = (Vcc - 0.0 \times Vg) = 0.0$$  \hspace{1cm} (3)

These give the two logic levels at node x for either input conditions. The output stages then shift these levels down by a base emitter junction drop, Vbe to make them compatible with the input logic levels. Saturation becomes a danger when the highest input level, Aih, becomes greater than IsRl. In normal operation the stages are cascaded with the input of the stage being considered (Aih) being set by the output of the previous stage (Aoh). Aoh itself is set by (VxH-Vbe) or -Vbe. In this condition the voltage on the collector of the input transistor is

$$V_c = -(I_s \times R_l)$$

and the voltage on the base is Vb=-Vbe for any Is,Rl combination. Because the output of the previous stage was set by Aoh the onset of saturation occurs in the case where Vc starts approaching Vb. Therefore with a known Rl, Is is calculated to be as near as possible to saturation but still keeping a safety margin. The maximum Is is:

$$I_s = \frac{+Vbe}{R_l}. \hspace{1cm} (5)$$

This gives a maximum Dv of:

$$Dv = (I_s \times R_c) + Vbe = (Vbe \times R_c / R_l) + Vbe$$  \hspace{1cm} (6)
In this way the logic centering and logic swing of the family is set. Many different logic families are possible by choosing Rc and Rl values that are compatible with the voltage and current capabilities of the process being used.

The DAC itself was originally designed around this logic block diagram.

**FIGURE 2** ORIGIONAL CIRCUIT BLOCK DIAGRAM

HOB CURRENT SOURCES  
R 2R LADDER LOB CURRENT DIVIDER  
3 TO 7 DECODE STAGE  
LOB LEVEL SHIFTER  
HOB LEVEL SHIFTER

The balance of accuracy to area was addressed in the number of bits directly decoded as compared to the number of bits that were decreased in significance by current division on the R-2R ladder. For the original circuit, bits D0 D1 and D2 were decoded from three binary bits to seven current sources. These are labelled the HOB or higher order bits. The HOB are decoded 2 to 7 by this truth table;

**FIGURE 3** HOB TRUTH TABLE AND LOGIC EQUATIONS

<table>
<thead>
<tr>
<th>INPUT CODE</th>
<th>A B C</th>
<th>SEVEN CURRENT STAGES</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>ON</td>
<td>ON : ON : ON : ON : ON : ON : ON</td>
</tr>
<tr>
<td>0 0 1</td>
<td>ON</td>
<td>ON : OFF : ON : OFF : OFF : OFF : OFF</td>
</tr>
<tr>
<td>0 1 0</td>
<td>ON</td>
<td>OFF : OFF : ON : OFF : OFF : OFF : OFF</td>
</tr>
<tr>
<td>0 1 1</td>
<td>ON</td>
<td>ON : ON : ON : ON : ON : ON : ON</td>
</tr>
<tr>
<td>1 0 0</td>
<td>ON</td>
<td>ON : ON : ON : ON : ON : ON : ON</td>
</tr>
<tr>
<td>1 0 1</td>
<td>ON</td>
<td>ON : ON : ON : ON : ON : ON : ON</td>
</tr>
<tr>
<td>1 1 0</td>
<td>ON</td>
<td>ON : ON : ON : ON : ON : ON : ON</td>
</tr>
<tr>
<td>1 1 1</td>
<td>ON</td>
<td>ON : ON : ON : ON : ON : ON : ON</td>
</tr>
</tbody>
</table>

**CURRENT SOURCE LOGIC EQUATIONS**

\[ I_1 = A + B + C \]  
\[ I_2 = A + B \]  
\[ I_3 = A + (B \cdot C) \]  
\[ I_4 = A \]  
\[ I_5 = A \cdot (B + C) \]  
\[ I_6 = A \cdot B \]  
\[ I_7 = A \cdot B \cdot C \]
This has the effect of portioning the input code into seven regions. When the first three bits A, B and C are in any combination the decoder stage turns the appropriate number of output current sources on to reflect the significance level of those three inputs. This portioning helps reduce the level of current that needs to be switched during operation as compared to using a pure R-2R ladder.

The remaining five bits D3 to D7 are on the resistor ladder and are labeled the LOB or lower order bits. A schematic of one half of the R-2R ladder is shown here:

FIGURE 4  R-2R LADDER

This ladder performs the function of decreasing the significance of a true signal in progression from D3 to D7. Each resistor is either R or R/2 in value and is configured to divide the current in half once for each of the five stages. The LOB output drivers are of the same value as the HOB output drivers which is 32*Ilsb. This value arises from the fact that the significance of the sixth bit is two to the fifth power which is 32. Bit D3 is divided once for a value of 16*Ilsb, and bit D7 is divided five times to give just Ilsb. The input resistance looking into the ladder is 75 ohms, which corresponds to video cable and video amplifier applications.

For clarity of discussions the DAC is separated into two portions, the digital and the analog. Each voltage node is prefixed by an A or a D to indicate the separation. Separate biasing is included so that if a saturation or latchup problem does occur then the general area can be discovered. Additionally the separation allows for the determination of the actual output current per stage during operation.
The remaining two blocks in the original diagram are for the setting of the logic levels and directing of the logic flow. They do not directly contribute to the functioning of the circuit.

EXPERIMENTAL

The first step in the procedure was to determine the best method of redesign through testing of the original circuit. This testing was facilitated by building several test jigs and then driving a sampling scope as the load. The first form of error found was a zero code offset, that is to say that a zero input gave a significant output. This was simulated on SNAP, a version of SPICE and determined to stem from the resistance of the ground node. The following plot is the output error as a function of ground node resistance Rrx.

FIGURE 5 GROUND NODE RESISTANCE ERROR
Since the \( I_{\text{out}}(\not) \) line is drawing full scale current when a zero is given as the input a resistance of only one ohm in the physical ground line will give an error of seven millivolts as shown in the figure. Since the fullscale swing is supposed to be a 1-volt peak signal through 75 ohms, 13.3 milliamps is a fullscale deflection. When fullscale is divided into 256 even divisions, the LSB or single increment value is 52 microamps and 3.9 millivolts. This gives a 2 LSB offset for a one ohm ground node resistance. Ground Node grouping and layout about the R-2R ladder is a prime consideration factoring into the control of resistance. Another problem observed was the glitches or timing mismatches that were consistently observed at the counting division between the LOB and HOB. The errors were consistent and nearly even for each of the seven transitions. These glitches were observed to have a pulse width of nearly one stage delay for the ECL gate type in use. Examination of the original circuit shows a disparity in the number of stages seen by the HOB and the LOB. The HOB had another logic stage to contend with, and hence an added delay. The addition of an even stage is therefore a consideration. Several other smaller changes to the global design were:

- A balancing of the HOB logic bus through readjustment of the decoder.

- A minimization of process gradients in current source resistors by placement changes.

- A latched and clocked buffer stage to remove the on and off chip delay from the bits due to very uneven line lengths.

- An input stage to generate the complement immediately after coming on chip, to limit pinout and increase gain for the latch.

These changes were implemented to match the pinout of a standard production part to aid in comparison of performance. The final change made was to alter the basic gate function and family type. The new circuit differs only in the center push down resistor \( R_p \) shown here.

Testing of other circuits following the original test chip layout had shown that by decreasing the amount of voltage the parasitic input capacitators had to change during an input transient the performance could be increased. The original logic swing was \( V_{\text{be}} \), the new one is cut in half by the center push down resistor to \( V_{\text{be}}/2 \). The original core of the circuit remained intact with the 3 to 7 decode and R-2R ladder portions of the circuit being integral to operation.
RESULTS/DISCUSSION

The first step in the layout was the creation of the single transistor and the differential pair. The single transistor was given a double base and collector configuration to enhance performance. Since layout size was not a constraint each transistor was also given a substrate connection. Shown below is the basic differential pair and a 1-x transistor as layed out.

FIGURE 7 LAYOUT OF 1-X AND DIFFERENTIAL TRANSISTORS
The double contacts and substrate connections may be redundant in a well controlled process but this design is for inclusion into a test pattern. As such information from imperfect runs in terms of process parameters is still desired. The layout of each cell is similar and differs only in the functionality. For ease of discussion and representation the schematics will be shown. There are three level shifter types used in the circuit; HOB, LOB, and 3-7 decode bus driver. Each performs the function of altering the logic levels so that the following stage is matched. There are several levels available that relate to the number of $V_{be}$ or diode drops in the output stage. They are labeled A1, A2, and A3 where A would be the logical variable and 1, 2, or 3 is the number of diode drops for that level. All the internal standard logic is at A1, and all the analog output drivers are at A2. The decoder stage in the HOB section requires all three levels for each of D0, D1, and D2.

The final layout is approximately 3 mil square, and is shown here in block diagram form.

FIGURE 8

The new design will be included on the next generation of test chip masks to be produced at National. Further estimation of the improvement of the circuit design will not be possible until the devices are fabricated.

ACKNOWLEDGEMENTS

Thanks to National Semiconductor, specifically Dick Merill for the use of National’s test, layout and simulation equipment. The initial work was all done there while on Co-op.
ABSTRACT

Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) measurements were performed to characterize field induced charges in thin (300Å) oxides subjected to a RF generated oxygen plasma used to remove photoresist. Results based on C-V curves indicate a -4.6 V threshold voltage shift for capacitors exposed to the RF plasma as compared to capacitors without plasma processing. Results based on tunnel current measurements were inconclusive.

INTRODUCTION

Recent industry trends calling for the fabrication of high density MOS devices have concurrently resulted in the use of thinner gate oxides. These thinner oxides are more susceptible to damage due to the high electric field stressing that may occur in subsequent plasma processing steps.[1-4]

Oxide traps are present in the SiO2 bulk as well as the Si-SiO2 interface, and are generally associated with defects in the film such as impurities and broken bonds.[4,5] Though usually uncharged, they may become charged if exposed to a large electric field, as is the case with a plasma. These traps are thought to be generation-recombination sites, and positive charge generation at the site of these traps has been attributed to impact ionization that occurs during high field stressing. Charge trapping in SiO2 is one of the principal causes of device degradation and instability in MOSFET's.

The conduction mechanism in thermally grown SiO2 has been found to take place via a Fowler-Nordheim (F-N) tunnelling mechanism.[6,7] The energy difference between the Fermi level and the conduction band in the oxide presents a barrier for electrons that enter the oxide from the metal gate. When a sufficient bias is applied to the gate, electrons tunnel through this barrier, thus a current flow is evident. Figure 1 illustrates this phenomenon.

Trapped positive charges in the oxide are thought to reduce the tunneling barrier thereby increasing the F-N current flow.[7] The mechanism here is thought to be due to the enhancement of the electric field from the positive charges.[8] Figure 2 shows the effect that positively charged traps in the oxide have on the barrier described in Figure 1.
Figure 1: F-N tunnel mechanism through SiO2 insulator

Negative Applied Gate Voltage

\[ V_g < 0 \]

Figure 2: The effect of trapped charges on oxide barrier height.
Fowler-Nordheim current may be represented by Equation 1 for the ideal case.

\[
J = \left( \frac{q^3 E^2}{\pi \hbar \phi_b} \right) \exp\left(-4(2m)^{1/2} \frac{q^3 \phi_b}{3 \hbar q E} \right)
\]

where \( J \) is the current density in A/cm\(^2\), \( q \) is the electronic charge in Coulombs, \( h \) is Planck's constant, \( E \) is the electric field, \( \phi_b \) is the barrier height, and \( m \) is the free electron mass. This shows the dependence of the current on the electric field present.

This experiment will attempt to identify and quantify field induced charges in thin oxides subjected to a RF generated oxygen plasma using two methods. First, the widely used Capacitance-Voltage (C-V) measurement techniques will be employed, and compared to a second method measuring enhanced Fowler-Nordheim tunneling currents as a function of plasma damage. C-V analysis will be done on stressed devices and compared to that of non-stressed devices. For these same conditions, the current will be measured, also using the C-V test apparatus, but in the conductance mode.

Equation 2 shows the flatband voltage of a MOS capacitor is a function of the non-idealities seen in the oxide.

\[
V_{fb} = -Q_f/C_{ox} - fQ_m - fQ_t + \frac{ms}{q}
\]

where \( Q_f, Q_m, Q_t \) are positive charges in the oxide as a function of fixed, mobile, and trapped charges. If trapped charges are present, a negative shift in the flatband voltage would be experienced. Figure 3 shows representative curves which illustrate the flatband voltage shifts that might be expected due to the trapped charges in the oxide for a p-type device.

Figure 3: Representative C-V curves illustrating flatband shifts due to trapped oxide charges.
Figure 4 is a plot of current density vs. applied gate voltage, and shows the shift that may occur if positive charges are increased in the oxide.[9] It is expected that I-V curves for devices processed with and without plasma would resemble these curves.

Figure 4: Current density vs. applied gate voltage [9]

EXPERIMENT

P-type, 14-cm, 3" wafers were cleaned using standard RCA techniques. A thermal oxide was grown in a dry oxygen ambient at 1000°C, with a resultant thickness of 320 Angstroms. This was followed by a nitrogen anneal at the same temperature for 20 minutes. The anneal step was done to minimize the amount of fixed surface states in the oxide. The wafers were split; one half was coated with photoresist and ashed for 20 minutes in a Plasmaline RF generated (250W) oxygen plasma. The control group did not see a plasma at any time. All the wafers were brought together; wafers were again cleaned, and aluminum was evaporated on the front side and the capacitor contacts were patterned. Following the patterning, aluminum was evaporated on the backside to form an ohmic contact. A 450°C sinter in forming gas (H2N2) was done to anneal the aluminum.

Testing was done on a Micromanipulator Model 410 high frequency C-V apparatus to determine flatband voltage shifts due to plasma processing. Using the same C-V test equipment, conductance was measured as a function of applied gate voltage.
RESULTS/DISCUSSION

Figure 5 is a representative C-V plot for a device that was exposed to a plasma (curve A) and compared to one that did not see a plasma (curve B). As expected, significant flatband voltage shifts have occurred in the devices that saw a plasma. The more gradual slope of curve A indicates the presence of interface states as well. Curve B shows a region in Cox which may be indicative of a leaky oxide.

Table I summarizes Cox, Cmin and Vt data for seven capacitors that were tested. From these values, an average flatband voltage shift of -4.6 Volts due to plasma was calculated.

**TABLE I: Summary of Results**

<table>
<thead>
<tr>
<th>Cox (pF)</th>
<th>Cmin (pF)</th>
<th>Vt (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plasma</td>
<td>No Plasma</td>
<td>Plasma</td>
</tr>
<tr>
<td>485</td>
<td>475</td>
<td>75</td>
</tr>
<tr>
<td>555</td>
<td>494</td>
<td>100</td>
</tr>
<tr>
<td>640</td>
<td>425</td>
<td>100</td>
</tr>
<tr>
<td>585</td>
<td>505</td>
<td>85</td>
</tr>
<tr>
<td>610</td>
<td>450</td>
<td>80</td>
</tr>
<tr>
<td>510</td>
<td>450</td>
<td>80</td>
</tr>
<tr>
<td>515</td>
<td>475</td>
<td>45</td>
</tr>
<tr>
<td>557</td>
<td>468</td>
<td>81</td>
</tr>
<tr>
<td>57.2</td>
<td>28</td>
<td>18.7</td>
</tr>
</tbody>
</table>

Mean 0.53 0.08 Std. Deviation

The theoretical threshold voltage as generated on the RIT CVPLOT program is approximately -0.3 Volts for a metal-semiconductor work function difference of -0.9 Volts, and $Q_f = 7.0 \times 10^9$. It should be noted that the threshold voltage for the control devices that did not see a plasma was much closer to the theoretical value than those that did see a plasma. This has been unprecedented at RIT for p-type MOS capacitors.

Cox and Cmin were both higher in the plasma group than the no plasma group. Different oxide thicknesses might cause this phenomenon but the difference in the two wafers was only 10 Angstroms and would not account for the large difference.

The variation across the wafer was also worse for the plasma group for Cox, Cmin and Vt.

Figures 6 is a plot of current versus applied gate voltage. The magnitude of the current is much larger than was expected, and the curve is linear as well. This supports the hypothesis that the oxide is leaky, thus we are simply measuring a resistance.
Figure 5: Capacitance Voltage Curves with and without Plasma

Figure 6: Current vs. Applied Gate Voltage

NEGATIVE APPLIED GATE VOLTAGE
CONCLUSIONS

This experiment provides preliminary evidence that plasma processing alters the C-V characteristics of MOS devices. Significant negative shifts in threshold voltage were evident in devices that experienced a plasma processing step, with an average of -4.6 Volts. A large leakage current has been demonstrated, and it is felt that 300 Angstroms is too thin for devices fabricated at RIT. Due to the implications of this experiment, a repeat is certainly warranted, and should include thicker oxides to eliminate the leakage effects. If this is done, the tunneling current phenomena may be experienced.

REFERENCES:

1. Singer, Peter, Evaluating plasma damage in thin gate oxides, Semiconductor International, August 1987


WEDAX STUDIES ON THE HITACHI S.E.M.

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ABSTRACT

The WEDAX (Wavelength Dispersive Analysis of X-rays) system incorporated into the Hitachi S.E.M. is a method of performing chemical microanalysis of a material. The primary objective of this project was to bring up the system to full operating status and calibrate the WEDAX utilizing known samples of aluminum, copper, and silicon. As of May 1988, the S.E.M. resolution is at 2K and the WEDAX is still inoperable.

INTRODUCTION

Wavelength Dispersive Analysis of X-rays (WEDAX) is a method of performing chemical microanalysis of a wafer surface. This technique is based on the theory that as the specimen is irradiated with an electron beam, x-rays are emitted with energies and wavelengths characteristic of the specimen's elemental composition. As the impinging electron beam strikes the surface atoms, electrons are inelastically scattered causing x-rays to be formed by two distinctly different processes. The incident electrons decelerate upon encountering the Coulombic field of the atomic core, which consists of the nucleus and tightly bound electrons, leading to the formation of a continuous spectrum of x-rays. This continuous spectrum of x-rays varies from an energy of zero up to the value of the incident electron energy [1]. The above process is referred to as 'bremsstrahlung', or "braking radiation." The continuum x-rays detected will show up as a form of background noise on the graph. The x-rays that we are primarily concerned with are those called characteristic x-rays produced by a sufficiently energetic beam electron causing an inner-shell electron, K, L, or M, to be ejected, leaving the atom in an ionized, or excited state. It takes the atom approximately ten picoseconds [2] to relax to its original ground state after ionization. In the process of relaxation, transitions of electrons from a higher shell to the vacancy, for example, from the L to K shell, results in the excess energy being released in the form of a photon of electromagnetic radiation. This x-ray emission process is summarized in Figure 1.
Various possible x-ray producing transitions are shown in Figure 2.

A transition of one shell is denoted by the subscript and that of two shells by a subscript. The energy of the photon is equal to the difference in energy between the shells involved in the transition, and for inner-shell transitions, the energy is such that the photon lies in the x-ray range of the electromagnetic spectrum.
These photons, according to the Duality Principle, have an associated wavelength which is related to the photon energy by:

\[ \lambda = \frac{hc}{qE} \]

where \( h \) is Planck's constant, \( c \) is the speed of light, \( q \) is the electron charge in coulombs, \( E \) is the energy in keV, and \( \lambda \) is given in nanometers. Due to the discreet energy levels between shells, we can fingerprint an element by its characteristic x-rays which are well known and tabulated.

Detection of the x-rays is a straightforward matter employing Bragg's formula. A small portion of the x-rays generated from the sample pass through a port in the specimen chamber and enter the WEDAX housing. The x-rays impinge on the analyzing crystal, are diffracted and enter the detector, as depicted in Figure 3. If Bragg's law is satisfied:

\[ n \lambda = 2d \sin \theta \]

where \( n \) is an integer, \( \lambda \) is the x-ray wavelength, \( d \) is the lattice spacing of the analyzing crystal, and \( \theta \) is the incident angle of the x-ray on the crystal, constructive interference will occur, providing a maximum at the detector. The distance \( l_\circ \) from the sample to the analyzing crystal in the x-ray spectrometer can be expressed by:

\[ l_\circ = 2r \sin \theta \]

where \( r \) is simply the Rowland circle radius of the spectrometer. Combining the two equations, we see that \( l_\circ \) is proportional to the wavelength by the equation:

\[ \lambda = \frac{(d/r) l_\circ}{2} \]

Thus, with known crystal lattice spacings and a fixed Rowland circle radius, determining the wavelength is a simple matter of reading \( l_\circ \) from the dial of the spectrometer and performing a simple conversion.
FIGURE 3. Schematic Diagram of Hitachi and WEDAX System. [3]
Upon entering the detector, the x-rays ionize the counting gas, a mixture of 90% argon and 10% methane, causing current to flow. This signal, proportional to the amount of x-rays detected is fed through a series of amplifiers, a pulse height analyzer, count rate meter and finally plotted on a chart recorder. The graph is a plot of the number of x-rays counted as a function of t₀, with the maximum peak corresponding to the major element contained in the sample. Figure 4 shows an example of a Kα transition for a sample containing copper, where t₀ is expected at 127.58 mm.

![Chart Recorder Graph](image)

**FIGURE 4. Chart Recorder Graph**

**EXPERIMENT**

The project was concerned with bringing up the S.E.M. and the WEDAX system. After connecting the utilities the system was ready to be powered up. Once running, the electrical and mechanical alignments were performed on the S.E.M. in accordance with the Hitachi User’s Manual. Facilities for the WEDAX consisted of 110VAC and P-10 gas for the detector. P-10 gas is a mixture of 90% argon and 10% CH₄ and enters the system at a flow rate of 1 bubble per second as measured by an auxiliary tube from the gas manifold and placed in a beaker of isopropyl alcohol. A sample of copper was then affixed to a specimen holder and irradiated by the S.E.M. in the spot mode at an accelerating voltage of 30KeV. The x-ray detector signal was routed from the pulse height analyzer through the count rate meter on the EDAX system and into a 10K resistor network. At the resistor network the signal was converted from a voltage to a current enabling it to be fed into the chart recorder and displayed as a function of time.

With the chart recorder running, the crystal drive was started with an initial t₀ reading of 60mm and ran to 223mm. The crystal used was RAP (rubidium acid phthalate) with a crystal
lattice spacing, \( d \), of 13.06Å. The \( I_0 \) reading associated with the highest peak was then compared to the expected table value. If a discrepancy occurred, the crystal would be placed at the position of maximum signal occurrence and the indicator assembly adjusted to reflect the expected value. This entire process would be repeated for samples of aluminum and silicon, with the final positioning of the indicator being a 'best fit' setting for all three samples.

RESULTS

Many hours were spent troubleshooting the electrical components of the S.E.M. due to the corrosion within the main console. The column was pulled-down, cleaned, reassembled, and by shining a light down the column, a rough mechanical alignment was performed. Upon troubleshooting the main console, a loose connection was found, reconnected and the system became operational. An electrical alignment was performed according to the Hitachi User's manual and a fluctuating beam current warranted replacement of the emission current potentiometer resulting in a repeatable resolution of 2K.

Inspection of the WEDAX system revealed worn crystal drive gears. It was determined that they would last through preliminary tests and replacement was to be made when the system is turned over for full-time use. With all portions of the system connected according to the manual, x-rays have yet to be detected.

SUMMARY

Further restoration of the Hitachi S.E.M. and WEDAX maybe questionable due to the excessive corrosion of all PC boards within the main console. If and when the WEDAX becomes operational, the replacement of the crystal drive gears is warranted. The S.E.M. is functional.

ACKNOWLEDGEMENTS

Drs. Lynn Fuller and Mike Jackson for their guidance and assistance in troubleshooting the system. Scott Blondell for his patience and technical expertise.

REFERENCES

EVALUATION OF INTEGRATED INJECTION LOGIC DEVICES AT RIT

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ABSTRACT

IL logic gates were fabricated using a two diffusion, four mask process. The functioning of NOR and OR gates were evaluated, and suggestions for improving the process are given.

INTRODUCTION

ILL was invented back in 1972 by two different groups working independently of each other; one at IBM Laboratories in Germany, and the other at Philips Research Labs in the Netherlands. Both groups had the same goal which was to develop a bipolar logic that combined the high speed of a BJT with the high packing density of MOS. The result was Integrated Injection Logic.

The IIL design evolved by shrinking direct-coupled transistor logic (DCTL) shown in Figure 1a. The emitter-grounded output transistor pair was replaced by a single multi-collector vertical npn transistor. A lateral pnp transistor was used as the current injector source, and replaces the diffused resistor of the DCTL gate by also acting as an active load. As a result, no large space consuming resistors are required on the chip for either the source or load function. Thus the DCTL gate shown in Figure 1a has been reduced to a single IIL transistor pair as shown in Figure 1b.

![Figure 1: (a)DCTL inverter (b)IIL equivalent inverter](image)

The end result of these modifications was to reduce the size of the logic gate down so that it takes up less real estate on the chip. Furthermore, the base of the npn and the collector of the pnp share a "p" diffusion, and the base of
the pnp and the emitter of the npn share an "n" diffusion as shown in Figure 2. This sharing of common regions between two transistors is called "merging" and further enhances the conservation of silicon area on the chip. Consequently, this makes IIL desirable for MSI and LSI applications. Other advantages of using IIL are that only four masks are required (two diffusions, contact, and metal) and there is no need for isolation or ion implantation which simplifies the processing.

![Figure 2: Cross-section of IIL inverter.](image)

Although IIL has many advantages, there are a few tradeoffs. First of all, in order for the "merged" design to work the pnp vertical transistor must operate in the reverse or "up" mode. In other words, the collector acts as the emitter and the emitter acts as the collector. This concept is shown in Figures 3a and 3b. For normal operation, the current flow lines are downward as shown in Figure 3a, whereas the current flow lines are upward for reverse operation as shown in Figure 3b.

![Figure 3: (a)normal operation, (b)reverse operation](image)

Since the collector is the substrate for normal operation, then the collecting area is very large with respect to the base area and most of the current from the emitter gets collected and high gains are easy to achieve. In contrast, for the reverse mode the collector area is small, and the
emitter is the substrate, so a large portion of the substrate current recombines in the base and is not collected. Therefore the reverse gain is considerably reduced. Furthermore, the gain is also proportional to the ratio of the emitter doping (Ne) to the base doping (Nb), as shown in Equation 1.

\[
\frac{I_c}{I_b} = \frac{Ne}{Nb} \frac{Dnb Lpe Ac}{Dpe Wb Ab} \tag{1}
\]

Since we are using the substrate as the emitter, and it is lightly doped at about 2.0E+15 then the reverse gain is reduced even further. A reverse gain of at least one is needed in order for III to be used in LSI applications where a large number of gates will be chained together. If the gain is less than one, then the small signal gain of the chain will be degraded with each stage until it cannot be distinguished from the background noise.

This project involved the testing of the NOR/OR gate circuit shown in Figure 4.

Figure 4: NOR/OR gate schematic

With a high input signal on A and B (A,B>800mv), current is injected from Q1 and Q3 into the base of Q2 and Q4 which are consequently driven into saturation. The voltage at the output of Q2 and Q4 is VCE sat, which corresponds to a low signal of approximately 100mv. Thus the NOR function has been realized. This low input of VCE sat is then the input to the next gate, Q6. Therefore, Q6 is off and the output of Q6 is pulled up to the 5V supply via the 10K pullup resistor, and the OR function is demonstrated.
However, if the input signal for A and B is low, then Q2 and Q4 are off, and current is injected from Q5 into the base of Q6; saturating it. Now the output of Q2 and Q4 are at VBE sat of Q6. This corresponds to a high signal of 750mv for the NOR gate. Since Q6 is saturated then the output of Q6 is VCE sat or 100mv, which is the low logic level for the OR gate. Thus the internal logic swing of the circuit from high to low is 650mv.

EXPERIMENT

The simple IIL logic gates described above, were fabricated and tested for proper functioning using a probe card setup. The NOR/OR gate shown in Figure 5 was tested to verify the operation of a IIL circuit. The circuit was tested using a 1.5V pulse at a frequency of 5KHz applied to inputs A and B, Vinj=5V, Rinj=1K, Vp=1V, and Rp=10K. A Tektronix 2430A digital oscilloscope, and HC100 color plotter were used to obtain plots of the input and output waveforms. The forward and reverse beta's of the npn vertical transistor were also investigated using the HP 4145A Parameter Analyzer.

RESULTS/DISCUSSION

The NOR and OR logic functions are verified by the plots in Figures 6 and 7. In Figure 6, the input signal for A and B is shown and the output of the NOR gate is plotted below it. When the inputs are low the NOR gate is at a high logic level of 750mv, and when the inputs switch high the NOR gate drops to a low logic level of 150mv. Thus the NOR gate functions as predicted by theory. The logic swing for the NOR gate is 600mv which is comparable to the predicted swing of 650mv. The internal switching times for the NOR gate were about 120ns. Figure 7 shows the input and output waveforms for the OR gate. When the inputs are low the output is low, and when the inputs switch high, the OR gate is pulled up to the 1V supply, and the OR function is verified. Note that the rise time for the OR gate was 4us and is much greater than the fall time of 120ns. The rise time is longer, since the 10K resistor limits the speed at which charge can be removed from Q6, whereas the fall time is shorter due to the saturation of transistor Q6 which pulls the output down. In order to reduce the rise time, an active pullup could be used in place of the 10K resistor.

The forward and reverse gain of the npn transistor was obtained from the plots in figures 8 and 9. The forward gain was 34 and the reverse gain was only 0.07. For the process used, the predicted reverse gain was 0.046, using the values shown below.
Figure 6: NOR gate function

Figure 7: OR gate function

Figure 8: NPN forward beta

Figure 9: NPN reverse beta
Even though the gain was low, the circuit still functioned properly since we were dealing with simple logic gates.

Also, recommendations made by Mark Grabosky[4] have shown to be instrumental in obtaining working circuits. He suggested to use a large N+ emitter diffusion to surround the circuit, and make contact with the substrate. This helped to reduce the emitter resistance, and any lateral hole diffusion. As a result, the logic swings were not affected. This diffusion is the cross-hatched region shown in the layout of Figure 5.

CONCLUSIONS

The results show that functioning IIL circuits can be made at RIT. Although the circuits were simple logic gates, more complicated designs can be made if the reverse gain is increased. One way of doing this is to start with an N+ substrate and grow an N- epitaxial layer on top of it for fabricating the circuit, as shown in Figure 10. Note, wafers such as these can be purchased from companies like Spire or Eaton.

The N+ substrate will now act as the emitter, and its doping can be used in equation 1 to calculate the gain. Substituting a value of 5.0E18 for the emitter doping results in a reverse gain of 2.45 which is greater than one.
Other ways of increasing the reverse gain are to maximize the ratio of collector area to the base area, and to minimize the base width.

ACKNOWLEDGEMENTS

C.E. Conrad for setting up the probe card station which facilitated the testing of these circuits.

REFERENCES


[5] Taub and Schilling, Digital Integrated Electronics, Chapter 4,
ABSTRACT

An experiment to compare resistivity and carrier concentration results for p-type silicon using four point probe and Hall measurements is described. The effects of current magnitude and magnetic field magnitude on the results obtained using Hall measurements were also investigated. The Hall data and four point probe data was in close agreement for both carrier concentration and resistivity for specified ranges of current and magnetic field.

INTRODUCTION

Hall measurements and four point probing are techniques used to measure the material properties of resistivity, carrier concentration and carrier mobility in semiconductors. Both methods provide information about the electrically active impurity profiles. While four point probing is much easier to perform, its application to compensated samples is hampered by the fact that two of the properties must be measured directly. In this way Hall measurements can be applied as an alternative method of characterizing semiconductor samples.

Hall measurements make use of the Hall effect to directly determine both the resistivity and electrically active carrier concentration in the sample. From those values the carrier mobility can be evaluated. The Hall effect is demonstrated by referring to Figure 1. Consider a uniformly doped sample of thickness t, width W and length L, through which a current I flows. By applying a uniform magnetic field B perpendicular to the current, a magnetic force is exerted on the charge carriers in the y direction. For equilibrium, a net force of zero in the y direction must exist on the carriers. Hence, an electric field
\( \vec{E} \), is established which counters the magnetic force. This effect, known as the Lorentz force, is demonstrated in Equation 1,

\[
F = 0 = q \vec{E} + q(\vec{v} \times \vec{B}) .
\]

Since all vector values are applied perpendicularly, Equation 1 can be reduced to scalar values and yields,

\[
qE_H = qvB
\]

or

\[
E_H = \frac{vB}{d} .
\]

Equation 2 can be easily manipulated to provide a measurable quantity, the induced Hall voltage,

\[
V_H = E_H W = \frac{vB W}{d} .
\]

Since the drift velocity in a semiconductor is

\[
v_d = \frac{I}{nq(tW)} .
\]

where \( n \) is the carrier concentration, then Equation 4 can be substituted in Equation 3 to provide the Hall voltage in terms of the measurable quantities \( B, I \) and \( t \) and thus

\[
V = \frac{IB}{nqt} .
\]

The Hall voltage is measured using a high impedance voltmeter from which the carrier concentration \( n \) is evaluated in Equation 5.

Resistivity can be found by removing the magnetic field and reconnecting the leads so that the terminals, thru which the current is supplied and the voltage is measured, are adjacent as in Figure 2.

\[
p = \frac{(\pi d / \ln 2)}{I_{AB} / V_{AB}} .
\]

This result stems from the restriction that the sample be symmetrical and provide equal path lengths through which the
current and voltage flow. A small correction factor determined by Chang should also be included to account for the finite contact size relative to the sample size [2].

The third property of the sample, the Hall mobility $u_H$, can be found using the results already determined and is given by,

$$u_H = \frac{R_H}{\rho}$$

where $R_H$ is the Hall coefficient (1/nq). The value of $u_H$ only has real significance in single carrier systems where it can be easily related to the carrier mobility, $u$, by a known proportionality factor, $r$, for the given material [3].

The application of Hall measurements has proven useful in the field of microelectronics to fabricate some unconventional integrated circuits. Hall sensors react to magnetic fields which induce a detectable voltage. The absence or presence of this voltage can be used to note the position of the sensor. Due to this fact, Hall sensors have found widespread use in keyboard switch applications.

This project was a preliminary investigation to determine the capability of detecting the low voltage levels which Hall sensors use. Positive results should indicate the feasibility of manufacturing functional Hall sensors.

**EXPERIMENT**

The experiment involved the fabrication of two identical devices used to measure induced Hall voltages in p-type semiconductors. As seen in Figure 3, square geometries were chosen with corner contacts to ensure the current applied and voltage measured were perpendicular to each other. Table 1 contains information pertaining to the devices.

![Figure 3. Hall sample with aluminum contacts A,B,C,D.](image)

<table>
<thead>
<tr>
<th>Table 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>length</td>
</tr>
<tr>
<td>width</td>
</tr>
<tr>
<td>thickness</td>
</tr>
<tr>
<td>$\rho$</td>
</tr>
<tr>
<td>carrier</td>
</tr>
</tbody>
</table>

The square geometries were cut from the wafers using a Tempress Model 602 saw. Following a RCA clean, aluminum was
deposited on the corners using a CVC evaporator to form the equally sized triangular contacts and sintered at 450 °C. Finally the squares were mounted on perforated plastic board and wire leads were connected to the contacts using silver paint. The set-up for the measurement of the Hall voltage is shown in Figure 4. A Keithley 220 Programmable Current Source with a voltage limit of 10 volts was used. The carrier concentration as a function of the magnetic field and current supplied was deduced using equation 5. The resistivity was measured by simply turning off the magnet and reconnecting the leads as mentioned earlier. Both the resistivity and carrier concentration determined using Hall measurements were compared to results obtained using a four point probe.

RESULTS/DISCUSSION

The resistivity values obtained using four point probe and Van der Pauw measurements are shown in Figure 5. A consistent Van der Pauw resistivity was found for a current ranging between 0.05 mA and 10.0 mA. Below 0.05 mA the sensitivity of the equipment was not high enough to supply an accurate voltage measurement. Above 10.0 mA the current supply was limited by a maximum voltage so the sample in fact did not see currents above 10.0 mA. This explains the drop in resistivity in Figure 5 and that data should be disregarded. Table 2 supplies the measured resistivity values and exemplifies the close correlation between the two measurement techniques.

<table>
<thead>
<tr>
<th>Table 2: Resistivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Four Point Probe</td>
</tr>
<tr>
<td>Hall (Van der Pauw)</td>
</tr>
</tbody>
</table>

The measured carrier concentration as a function of current is shown in Figure 6. For a magnetic field of 4000 Gauss, the carrier concentration was relatively constant for a current supply between 0.05 mA and 10.0 mA. The carrier concentration
Figure 5
RESISTIVITY USING HALL MEASUREMENTS
Resistivity vs. Current

![Graph showing resistivity vs. current](image)

Figure 6
CARRIER CONC. USING HALL VOLTAGE MEASUREMENTS
Carrier Concentration vs. Current (B=4000 gauss)

![Graph showing carrier concentration vs. current](image)

Figure 7
CARRIER CONC. USING HALL MEASUREMENTS
Carrier Concentration vs. Magnetic Field (1 - 1.0 mA)

![Graph showing carrier concentration vs. magnetic field](image)
outside this range varied due to the same reasons the resistivity varied. Table 3 supplies the measured carrier concentrations and again a close correlation existed between the two measurement techniques. The graph in Figure 6, for a magnetic field of 4000 Gauss, typified curves for other magnetic fields.

Table 3:
Electrically Active Carrier Concentration
(B = 4000 Gauss)

<table>
<thead>
<tr>
<th>Method</th>
<th>Concentration (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Four Point Probe</td>
<td>2.0 x 10¹⁴</td>
</tr>
<tr>
<td>Hall</td>
<td>4.1 x 10¹⁴</td>
</tr>
</tbody>
</table>

Figure 7 demonstrates the carrier concentration as a function of magnetic field for a current supply of 1.0 mA. As the magnetic field increased the carrier concentration increased in a non-linear yet non-logarithmic fashion. The reason for this remains unresolved at this point. Similar results occurred for other constant current supplies.

Overall, the resistivity and carrier concentration values obtained using Hall measurements matched closely to those values obtained using a four point probe. Given the existing equipment, Hall measurements can be used to provide a close estimate for the carrier concentration and resistivity in a semiconductor. The data suggests that the generated Hall voltages were in fact real with only slight inaccuracies that may have resulted from spurious emf’s, contact resistance, lack of perpendicularity of the magnetic field and current flow, and finite contact sizes. Magnetoresistance and scattering showed no evident effect on the material parameters for the p-type silicon. Based on these results the capability to fabricate and test diffused Hall sensors with the existing equipment may be possible. Only a more sensitive voltmeter (0.1 to 1.0 mV range) and modifications to the set-up are needed to accommodate the smaller sample. However, lattice scattering, finite contact size and magnetoresistance may introduce problems due to the conduction nature of the diffused n-type silicon needed in a Hall sensor.

CONCLUSIONS

An experiment set up to obtain resistivity and carrier concentration from Hall measurements has been described and shown to correlate well with four point probe measurements. Based on these results, the manufacture and testing of functional Hall sensors should be possible.
ACKNOWLEDGEMENTS

Thanks to Mike Jackson for his advice and help obtaining supplies and Dr. Peter Cardegna, in the Physics department, for his advice and cooperation.

REFERENCES


ABSTRACT

A basic test station, using a modified four point probe was designed and built for measuring resistivity over a temperature range. This test station can now be used to characterize the effects of any subsequent semiconductor processing on transition temperatures and performance of superconductive films.

INTRODUCTION

A short history of superconductors is provide to fully understand the background of this project [1-17]. Superconductors are materials that exhibit a complete loss of electrical resistance as they are cooled below a critical temperature. This phenomenon was discovered in 1911, when physicist Heike Kamerleigh Onnes was conducting experiments with mercury at low temperature. During one of his experiments he noticed that the resistance of a sample all but disappeared at four degrees Kelvin. Little work was done in the early parts of the century, and the work that was done, was limited to metals and metal alloys.

Then in 1973 niobium alloys were found to exhibit superconductivity at around 23 K. These materials found their first applications in medical imaging systems and in particle accelerators. Still, the temperatures needed to obtain superconductivity made most applications impossible. Then in 1983 metal oxides such as BaLaCuO showed transition temperatures of 35 K. This was a major jump from the previous temperature of 23 K, and was discovered by two of IBM’s research scientists, Karl Alexander Muller and Georg Bednorz. Early in 1986 another small jump up to 44 K was observed in niobium-germanium-aluminum and oxygen material developed by two Japanese scientists, Oguski and Osono. During the last few months of 1986 various researchers started working with ceramic material with transition temperatures around 70 K. Early in February of 1987 a Houston scientist discovered a ceramic material (yttrium, barium, copper, oxide) with a transition temperature of 95 K. This was probably the most significant development since the discovery of superconductors, because liquid nitrogen could now be used as a coolant instead of the conventional liquid helium coolant. The boiling point of nitrogen is 77 K while the boiling point of helium is 4.2 K. Nitrogen is much cheaper, easier to handle and obtain than liquid helium. Liquid helium has a current price of about four dollars a liter compared to forty cents per gallon for liquid nitrogen. Reports of superconductors with higher critical temperatures continue to come in almost weekly.
Electric claims to have developed a material made up of yttrium, copper and oxygen that shows superconductivity at room temperature, up to 27°C (1). Probably the most promising new development comes from Georgia Institute of Technology. Physicist Ahmet Erbil says that he has developed a material made of copper oxides with a critical temperature of 500 K (2). This report like many others remains unconfirmed, but if true, would revolutionize the superconductor field.

Before tackling the importance and limitations of superconductors in the Microelectronics field it is necessary to consider some background material. Two basic criteria for a material to be accepted as a true superconductor are zero resistance below a critical temperature and the material must show the Meissner effect. The Meissner effect is defined as the expulsion of a magnetic field from a material's interior (4). This phenomenon is easily shown in the floating magnet experiment. The zero resistance effect is shown in Figure 1. Superconductive materials have basically the same resistance versus temperature curve as most metals until the critical temperature is reached, at which point the resistance drops off dramatically.

Superconductors not only have critical temperature criteria but critical current and magnetic field specifications as well. Critical current is the maximum current density a sample may conduct before its resistance reappears. Critical magnetic field is much the same but not as much of a limitation as critical current. Current densities have been raised to 100,000 A/cm² in thin films, but is limited to 1,000 A/cm² in bulk material.

Other problems that plague thin films of the high Tc materials have to do with stability. Superconductors tend to lose oxygen when exposed to atmospheric pressures. The loss of oxygen has drastic effects on performance, since oxygen is a crucial factor in the structure of superconductors. Many of the superconductive materials available today are very sensitive to water, heat and air which degrade their delicate structure and composition.

![Figure 1: Typical response of resistance to temperature for YBaCuO](image-url)
The most obvious application of superconductors to microelectronics is their use as zero resistance interconnects. Low power dissipation, coupled with faster signal transfer makes this application very attractive. The most important application in VLSI technology has to be Josephson junction devices. Josephson junctions are comprised of a thin insulating material sandwiched between two superconductive plates. One of the superconducting layers acts as a gate, when a voltage is applied, a magnetic field changes the current in the other layer. These devices act as superfast, low power, switches. Their low power dissipation also allows for higher packing densities.

Little is known about the reaction of superconductive films to standard semiconductor processing steps. Steps such as lithography (how will prebake and post bake temperatures effect the thin films?), chemical etching, plasma etching, and a host of other processing steps still need to be characterized for superconductive thin films. Ultimately a complete analysis of semiconductor — superconductor hybrid circuits, and their fabrication, must be done before superconductors become an important part of VLSI technology.

This project involved a special set up to achieve the environmental conditions needed to perform resistivity measurements at low temperatures on thin films. The main concern of this station was to provide accurate and repeatable resistivity measurements without degrading the thin film. Attention was given to uniform cooling and heating of the system so as to obtain the most accurate temperature readings and a vacuum environment to minimize condensation on the film.

EXPERIMENTAL

Figure 2 shows the basic test setup consisting of the sample chamber and the supporting equipment. A roughing pump was used to evacuate the chamber of any water vapor that might degrade the film upon cooling. This was connected to the chamber through a threaded brass coupling. A nitrogen bath was placed below the chamber, and contained in an "Igloo" cooler.

The vacuum chamber is the main assembly of the test station. The chamber is made of copper to insure maximum heat flow. Contained within the chamber is a four point probe, heating element, thermocouple, and sample stage. The chamber itself consists of two end caps and a four inch section of four inch diameter tubing. The top end cap and midsection was soldered together and sealed. The bottom end cap is removable, to accommodate the placing and removing of samples. An O-ring between the bottom end cap and upper chamber insures proper sealing.

The sample stage rests on the bottom end cap and supports all of the internal equipment. The stage consists of two aluminum plate with an intervening heating element. The surface of the stage is a Boron Nitride disc, this material was used to
SUPERCONDUCTOR TEST STATION
RESISTIVITY - VS - TEMPERATURE
(THIN FILMS)

VACUUM CHAMBER ASSEMBLY

4-POINT PROBE
PROBE MOUNT
SAMPLE HOLDERS
BORCN NITRIDE DISC
THERMOCOUPLE
ALUMINUM PLATES
HEATING ELEMENT
END CAP (COPPER)
O-RING

FINES

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electrically insulate the sample from the other elements while still allowing excellent thermal conductivity. A four point probe is also contained within the chamber, the probe is a standard tool for measuring resistivity of thin films. The four point probe is mounted on a teflon probe holder. This holder allows for positioning of the probe, although very limited, and securely holds the probe with three set-screws. The holder is made of teflon to protect the probe from the extreme cold temperatures during the experiment (the probe tips will be directly on the sample). A thermocouple is clipped to the stage and is used to monitor the temperature upon heating. The thermocouple implemented was an Omega "Type-J" thermocouple, which can measure temperatures down to -210 °C. Eight wires connect the various components to outside equipment through an epoxy seal.

The thermocouple voltage was connected to a DMM in parallel with the x-axis of a chart recorder. The voltage from the four point probe was connected to a DMM in parallel with the y-axis of the same chart recorder.

Four point probe voltage as a function of temperature is plotted as the sample is heated. Readings from the thermocouple DMM must be taken at two points to accurately calculate temperature. The resulting graph can be converted to a resistivity versus temperature graph by using the thermocouple table (APPENDIX-A) in conjunction with the equation for resistivity as a function of probe voltage (V), current (I) and spacing (S), given by rho:

\[
\rho = 2\pi TS(V/I)
\]

RESULTS/DISCUSSION

The test station was calibrated by measuring the resistivity of a silicon sample at room temperature and comparing it to another standard four point probe setup.

Problems appeared when cooling started. The Thermocouple never reached the desired temperature, that is to say that the correct voltage was never generated. The temperature achieved was only -10 °C. A slight air pocket between the stage and bottom end cap, the insulated heating element between the two aluminum plates, coupled with the fact that a vacuum is present could account for this lack of heat flow, since a vacuum allows for little heat flux. Another problem that resulted upon cooling, was that the four point probe voltage became very erratic and actually went up. This may have been caused by contact problems that resulted from uneven heating. Compressive stress on portions of the stage and chamber could have caused the probes to lift off slightly.
Yet another problem was identified when the chamber was opened after the experiment. Proper vacuum was not achieved and water had condensed on the inner surface.

The solution to the first two problems is to allow for better thermal conduction. The first step is probably to eliminate the heating element and let the sample warm to room temperature without assistance thereby allowing for direct contact of the two plates. The next, and easiest step, is to make sure that the stage is in direct contact with the bottom end cap before placing it in the chamber.

Before a higher vacuum can be achieved a leak check should be done to find the source.

SUMMARY

The test station was designed for resistivity measurements as a function of temperature. The station works at room temperature but needs to be modified in the area of heat transfer and vacuum technology. A couple of suggestions for a second generation test station, if there is to be one, include; enclosing the nitrogen coolant and modifying the probe holder to allow for greater mobility.

ACKNOWLEDGEMENTS

I would like to thank Scott Blondell and Gary Runkle, for assisting me in building and testing, Jim Argana from CVC corp. for supplying samples and advice, Standard oil of Niagra Falls for supplying Boron Nitride discs, and Dr. Richard Lane, Dr. Bob Snyder, Rob Pearson, and Mike Jackson for advice and information.

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THE USE OF A CONTRAST ENHANCEMENT LAYER TO EXTEND THE
PRACTICAL resolution LIMITS OF OPTICAL LITHOGRAPHIC SYSTEMS

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Rochester Institute of Technology

ABSTRACT

Resolution capability of a GCA Mann 4800 DSW stepper was improved using a bilayer photoresist scheme consisting of CEM-420 applied on Shipley 1400-27 resist. Wall profile or contrast improvements were observed experimentally on a 1.4 micron line-space pattern by using the Scanning Electron Microscope. Perkin-Elmer Development Rate Monitor (DRM) simulations predicted the above improvements by the use of the PROSIM software applications program. The physical data and simulations were evaluated and demonstrated a contrast improvement on the order of four times for the wafer with the contrast enhancement material.

INTRODUCTION

Today in semiconductor fabrication, circuit dimensions are becoming smaller and smaller due to the demand for increased performance. This fact, along with the need for masking low selectivity plasma processes, has increased the aspect ratios needed in the resists. Consequently, this puts higher demands on the exposure systems being used. Currently, optical lithography is the predominant patterning technique, even though it doesn't demonstrate the resolution capabilities of such systems as e-beam, ion-beam, and x-ray. This is due to the higher throughput, versatility and process simplicity inherent with optical systems. Therefore, new resist processing procedures have to be utilized in order to overcome the optical limitations (Numerical Aperture, Wavelength, and Depth of Focus) associated with optical projection systems. One such technique is the use of a contrast enhancement layer (CEL) on top of the resist to increase the working resolution by producing resist patterns with very steep wall profiles.

In optical lithography an aerial image of the mask actually exposes the resist. An aerial image for optical systems is shown in Figure 1. For aerial images the discrimination between darker and lighter regions is a continuous one. Thus, the image obtained can be degraded due to the diffracting lower intensity light. A CEL helps to improve the ability of the resist to effect this discrimination and consequently raise the contrast level of the aerial image. In other words the CEL modifies the aerial image which the resist sees.
The CEL is a high concentration photobleachable dye in the film. Initially the film is opaque, but following a dose of radiation it becomes transparent. During exposure the regions of the bleachable layer that are exposed to the highest intensities bleach through first, while those parts of the layer that receive the lowest intensities bleach through at a later time. If the exposure of the underlying resist proceeds faster than that of the CEL then the resist beneath the high intensity regions will be completely exposed before the low intensity regions in the CEL have a chance to bleach through and the underlying resist will not be exposed. The dynamics of this bleaching process are shown in Figure 1.(1)

In essence, the CEL forms an in situ contact mask for the resist, thus taking advantage of contact printing without mask degredation. A comparison of contrast enhanced and non-contrast enhanced imaging is demonstrated in Figure 2.(4) All of this giving rise to a lower contrast threshold for projection systems. It must be noted that the exposure doses for resist covered with a CEL are typically twice as much as that of resist alone, due to the bleaching which must occur.

The contrast enhancement material used in this experiment was Altilith CEM-420, optimized for use with G-line (436nm) illumination systems. A graph of the optical transmission properties is shown in Figure 3.(5) This shows a high Initial absorption at the G-line, which is necessary for optimum contrast enhancement. Therfore, the GCA Mann 4800 DSW Stepper, which has optimum focus at the G-line, was used to expose the resist.
One problem with CEM is that it must be removed before development because it is not soluble in the developer. This is done by the use of an organic solvent mixture consisting of 85% toluene and 15% anisole. However, when positive photoresist is exposed to such a solvent an inhibition is observed at the surface of the resist. This effect may be due to the solvents involved and/or interlayer diffusion. What is known is that the inhibition is strongly dependent on the process and can be adjusted from experimental results obtained from various processing techniques. This inhibition effect is not yet fully understood, but the results show no negative drawbacks.

Development was carried out with a sodium hydroxide based developer. The reason for this is that metal ion free developers typically have more resist loss and lower contrast than the sodium based developers. Development rate data was obtained from the Perkin-Elmer DRM 5900. I refer the reader to the RIT DRM operation instructions document for information pertaining to theory, procedure and the application software Dreams and Prosim.

EXPERIMENT

Using 4-inch wafers an adhesion promoter (HMDS) was applied via static dispense and a 4000 rpm spin for 20 seconds utilizing a manual spin coater. Subsequently, Shipley 1400-27 resist was dynamically dispensed at 800 rpm with a manual ramp to 4000 rpm for a total time of 40 seconds. One of the most important factors in obtaining a desired resist thickness, in this case 1.2 microns, is the ramping. The wafers were pre-baked on the GCA Wafetrac 9000 hotplate for 100 seconds at 90 c. After the wafers had been coated and prebaked two wafers were coated with the Altolith CEM-420. To obtain the desired film thickness of 6000A-7000A the material was dispensed at 500 rpm and then ramped to 4000 rpm for 25 sec.
Exposure was performed on the 10:1 GCA Mann 4800 DSW Stepper. Since the Perkin-Elmer DRM 5900 was used it was necessary to first do step exposures with the DRM 5900 mask to obtain development rate data. This means that a 6x6 array was produced on the wafer with each row being a different exposure and each die representing the DRM 5900 mask. Table 1 shows the exposure dose that resulted for various times using 260 mw/cm² intensity for wafers with and without CEL.

**TABLE 1**

<table>
<thead>
<tr>
<th>NO CEL</th>
<th></th>
<th>CEL</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Dose(mJ/cm²)</td>
<td>Time(sec)</td>
<td>Dose(mJ/cm²)</td>
<td>Time(sec)</td>
</tr>
<tr>
<td>3</td>
<td>0.01</td>
<td>135</td>
<td>0.52</td>
</tr>
<tr>
<td>47</td>
<td>0.18</td>
<td>179</td>
<td>0.69</td>
</tr>
<tr>
<td>91</td>
<td>0.35</td>
<td>223</td>
<td>0.86</td>
</tr>
<tr>
<td>135</td>
<td>0.52</td>
<td>267</td>
<td>1.03</td>
</tr>
<tr>
<td>179</td>
<td>0.69</td>
<td>311</td>
<td>1.20</td>
</tr>
<tr>
<td>223</td>
<td>0.86</td>
<td>355</td>
<td>1.37</td>
</tr>
</tbody>
</table>

Prior to development, Altilith CEM Stripper A-15 was puddled on the wafer for 45 seconds then spun dry at 4000rpm for 30 seconds. Development was carried out with the DRM using Shipley AZ351 developer diluted 2:1. Each wafer was analyzed with the Dreams and Prosil software applications programs to determine thickness vs. time, dissolution rate vs. thickness, thickness vs. log exposure, and resist profile simulations for the two processes.

Two more wafers were processed, but with the use of the RIT ETM mask. The development times for the wafer with CEM and the one without were 270 and 290 seconds, respectively. The purpose for this is to evaluate the edge profiles and resolution limits of the two processes using the Cambridge SEM. However, before they could be viewed with the SEM a thin layer of aluminum had to be deposited in order to dissipate any charging which could disintegrate the resist.

**RESULTS**

One advantage of CEM-420 is that it allows you to obtain much steeper side wall angles without any significant resist loss. Figure 4 shows 1.4 micron features with and without a CEL and Figure 5 shows the same features at a higher magnification. An improvement in contrast is demonstrated. However, from the SEM pictures it is difficult to see the amount of resist loss predicted by the DRM. The resist loss predicted was on the order of 0.2 microns, which was obtained from the resist profile simulation.
The DRM plot of Thickness vs. time showed the inhibition effect related with the use of a CEM. Other plots such as dissolution rate vs. thickness showed how the CEM doesn't deal with the standing wave effect and the thickness vs. log exposure plot showed an increase of gamma on the order of four times.

All of these simulations helped represent the final plot of the resist profile, which showed the increase in contrast and no resist loss for the wafer with a CEL. The one without, predicted image degradation defined by resist sidewall angle and resist loss. This was verified in the SEM pictures talked about above.

There were problems of resist adhesion on the patterned wafers, which could have been attributed to the HMDS used or the application. However, this could be remedied by patterning the resist on oxide grown wafers.

CONCLUSION

This simple bi-layer process showed how resist profiles can be improved without much added complexity. Although the fundamental optical resolution limits cannot be exceeded, the working resolution can be greatly enhanced. Also the added advantages allow the resist to be coated on thick so that some topography problems can be dealt with. Further work could be done in this area by trying to image high aspect ratio lithography.

REFERENCES


ABSTRACT
This project was an evaluation of a PMOS op amp characteristics. Due to nonworking op amps, SPICE simulation and design layout were investigated. Results show that new design and fabrication are needed.

INTRODUCTION
The op amp, designed to operate with +/- 9 volts power supplies, has been fabricated at RIT for possible commercial applications. It consists of two gain stages with an overall gain of 2000. The first gain stage is a differential input stage with a gain of 50. One of its differential outputs is level shifted using a source follower. Its other output is used to establish a reference bias voltage for the source follower through a saturated load. The second gain stage has a gain of 40 with its output buffered by an output stage to enable the op-amp to drive low impedance loads. The op amp circuit is shown in Figure 1, and its layout is given in Appendix I.

FIGURE 1. PMOS Op Amp Schematic Diagram

The operational amplifier parameters to be evaluated were broken down into four categories: open-loop differential characteristics, output signal response, input error signals, and common-mode characteristics. In this section, these parameters will be defined. And in each case, practical test circuits for parameter measurement are presented and described.
The open loop gain of the op amp is measured by plotting the input voltage versus output voltage with a load resistance of 20K [1]. The input signal (sweep) has enough amplitude to drive the output into saturation in both the plus and minus directions. Gain is equal to any output voltage change divided by the input voltage change that causes it. The slope of the curve at any point depicts the small signal gain near that point.

Output resistance of an op amp is the effective output source resistance when operated open loop. Using the open-loop parameter test method above, the output resistance of an op amp is measured by observing the low frequency gain decrease produced by the load [2]. The gain decrease results from the output voltage division across the output resistance and the load resistance, and the loaded gain is

\[ A_0' = \left(\frac{R_{load}}{R_o + R_{load}}\right)R_{load} \]

Then the output resistance will be

\[ R_o = \left(\frac{A_o}{A_0'} - 1\right)R_{load} \]

Unity-gain bandwidth is the frequency range from direct current to that frequency at which the open loop gain crosses unity. Because of slewing rate limiting, only small-signal response is achieved at this frequency, and the output test signal should be observed to ensure that the amplifier is in linear operation. The unity gain bandwidth is measured in a closed-loop circuit as in Figure 2 to avoid being affected by the highly amplified noise common to the open-loop test circuits.

![Unity-gain Bandwidth Test Circuit](image)

\[ f_c = \text{frequency at which } V_o = -V_s \]

FIGURE 2. Unity-gain Bandwidth Test Circuit

Slewing rate is the maximum rate of change of output voltage. In general, slewing rate is measured in the unity-gain voltage follower circuit of Figure 3. The amplifier is driven by a high frequency square wave. The slew rate is found as the slope of the transition between the output extremes.

Offset voltage is an important parameter when an op-amp is used to amplify small direct voltages. This is the differential dc input voltage required to provide zero output voltage with no input signal or source resistance. The offset value is measured
at room temperature. To facilitate the measurement of the input offset voltage a high-gain test circuit is used to amplify the offset as indicated in Figure 4 [2].

\[
V_{os} = -(V_{o}/1001) \\
V_{o} = -((R_{1}+R_{2})/R_{1})V_{os}
\]

**FIGURE 4. Input Offset Voltage Test Circuit**

Input offset current is the DC biasing current required at either input to provide zero output voltage with no input signal or offset voltage. The input bias current is the gate leakage current of an input FET. The input bias currents are measured by forcing them to flow in large resistors, as in the test circuit of Figure 5, which are bypassed to reduced noise. The output voltage is essentially the product of one of the resistors and the associated current. It is typically necessary to null the input offset voltage [2].

Switches:

<table>
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<tr>
<th>Switches</th>
<th>Vo</th>
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<tbody>
<tr>
<td>open</td>
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<tr>
<td>S1</td>
<td>I_{bias} * R_{g}</td>
</tr>
<tr>
<td>S2</td>
<td>I_{bias} * R_{g}</td>
</tr>
<tr>
<td>S1, S2</td>
<td>I_{os} * R_{g}</td>
</tr>
</tbody>
</table>

For Vo much larger than Vos

**FIGURE 5. Measurement Circuit for Input Bias Currents and Input Offset Current**
Input offset current is the difference between two input bias currents. This difference current is measured as indicated in Figure 5. Since the measurement takes the difference between two currents which are of the same order of magnitude, it is necessary to match the two resistors to within about .1 percent.

Common mode rejection ratio is the ratio of the differential voltage gain to the common-mode voltage gain. The CMRR is a figure of merit comparing the gain received by differential signals with that received by common-mode signals. The common mode gain is often a nonlinear function of the common-mode voltage level, especially for FET input amplifiers. For this reason the full common-mode voltage swing must be used in measuring CMRR. This is achieved by using the difference amplifier circuit of Figure 6. For well-matched or balanced resistors as indicated, the signal at the two inputs is essentially a common-mode signal. However, the common-mode unbalance of the amplifier produces an output error voltage and an associated differential input voltage \( V_i = \frac{V_o}{A_d} \). Then the common-mode rejection ratio can be written [2]

\[
CMRR = \frac{A_d}{A_{cm}} = \frac{(V_o/V_i)}{(V_o/V_{cm})} = \frac{V_{cm}}{V_i}
\]

where \( A_d \) is the differential gain, \( A_{cm} \) is the common-mode gain, \( V_o \) is the output voltage, \( V_i \) is the differential input voltage, \( V_{cm} \) is the common-mode input voltage. This can be rewritten considering

\[
V_o = \frac{(R_1+R_2)}{R_1} V_i
\]

\( V_{cm} \sim V_s \) for \( R_2 \) very large compared to \( R_1 \)

The common-mode rejection ratio is then expressed simply in terms of the input and output signals by combining the last three relationships to get

\[
CMRR = \frac{(R_1+R_2)}{R_1} \frac{V_s}{V_o}
\]

where \( V_s \) is the input voltage

![Common Mode Rejection Ratio Measurement Circuit](image)
Power supply rejection ratio may also be plotted and measured with a curve tracer. PSRR shows the effects that a change in power supply voltage may have on the output of an op-amp. Either the positive or negative supply may be changed to show the effect. The output of the op-amp is held close to zero volts during these changes by applying the right amount of voltage between its inputs. Input voltage is plotted against power supply voltage [1].

EXPERIMENT

Prefabricated PMOS op amp were diced, mounted, and wired bonded for testing. The op amp were inoperable even at other values of VDD and VSS. Threshold voltage of discrete P-ch transistors were obtained (Appendix II) and compared to the designed value. Several on-wafer op amp were probe tested showing non working op amps. SPICE simulation using actual threshold voltage was done (Appendix II). Design layout was also checked.

RESULT/DISCUSSION

Table 1 is a summary of the testing and simulation results. The discrete P-ch transistor threshold voltage ranged from -4.5 to -5 compared to -3 volts as designed. Design layout checking revealed that transistor MB was improperly designed with ratio

<table>
<thead>
<tr>
<th>\ \POWER\NSS\SUPPLY</th>
<th>+/-9volts</th>
<th>+9/-5volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>B.28E11 (Vth=-3v)</td>
<td>W/L = 10/100</td>
<td>W/L = 100/10</td>
</tr>
<tr>
<td>GAIN = 73DB</td>
<td>OUTPUT CONSTANT</td>
<td>AT 5.43V</td>
</tr>
<tr>
<td>CURRENT SOURCE</td>
<td>SOURCE SOURCE</td>
<td>SOURCE</td>
</tr>
<tr>
<td>IS OFF IS OFF IS OFF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

W/L inverted. The SPICE simulation results, using +/-9 volts power supply, showed that for the designed W/L ratio of 10/100 and threshold voltage of -3 volts, the op amp functions as expected though with a higher gain than was designed (i.e. 73DB instead of 66DB). This is due to the non unity gain of the source follower and the output stage. SPICE simulation using the
W/L of 100/10, i.e. actual layout, with the same -3 volts threshold show a constant DC transfer curve of Vout constant at 5.43 volts for any value of Vin from -2 to 2. For NSS value of 1.55E12 which gives an equivalent threshold voltage of -4.6 volts. The current source MB is off. The op amp was also simulated at supply power of -9/+5 volts with threshold voltage of -4.6 volts. Again, the current source MB is off. In summary, SPICE simulation showed that, with the wrong W/L ratio for MB and actual Vth, non of the op amp would work.

CONCLUSION

Actual measurements of the op amp parameters were not possible due to the non working op amps. However, a revision of the layout with the change of W/L ratio for transistor MB from 100/10 to 10/100 together with a tighter controlled process to produced the wanted threshold voltage of -3 volts would fix the problem.

ACKNOWLEDGEMENTS

Dr. Fuller for his permission to use his previous results and Mike Jackson for all his inputs.

REFERENCES

SETUP AND PERFORMANCE TESTING OF AUTOSORT MARK II FLATNESS ANALYSIS SYSTEM

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Rochester Institute of Technology

ABSTRACT

An Autosort Mark II wafer flatness tester was installed and initial runs and performance testing accomplished. A guide for aiding in everyday use of the machine was written as well as a fortran program that performs a statistical analysis on performance data.

INTRODUCTION

In the age of ever smaller line widths there is an increasing importance on optimizing performance of optical exposure systems. Knowledge of the exposure surface flatness cannot be overlooked in this optimization. Information in regards to total vertical runout, deviations from a specified focal plane, and wafer percentage within depth of focus limitations are important criteria that may be used to enhance resolution and yield performance for various optical exposure tools. The effect of various processing steps, such as high temperature oxidations, may affect wafer flatness and hence optimum resolution.

The Autosort Mark II wafer flatness tester, made by Tropel and donated to RIT by Eastman Kodak, provides information in regards to the above tests and sorts a group of measured wafers based on one user selected criteria. Even though sorting is performed on one criteria, data for each criteria is obtained for each wafer measured.

Interferometry, the method of measuring wafer flatness, is based on the wave nature of light. When two (or more) light waves of the same wavelength are superimposed, interference results in one wave. Depending the phase difference of the waves (fractional part of a period in which the time variable of a wave has moved), the interference will be constructive, producing a light fringe, or destructive, producing a dark fringe. At the constructive extreme, the two light waves will have phases that are an integer number of wavelengths apart and the resultant wave will have an amplitude that is the sum of the individuals. At the destructive extreme, the two light waves will have phases that are 180 degrees (one half the wavelength) apart and the summed amplitude of the resultant wave will be zero. These interferences cause alternate dark and light fringes and the various phase relationships of the two light waves that fall between these extremes will produce shades of gray fringe patterns.
The optical path of a typical interferometer system is shown in Figure 1. The light is directed into a prism and split into two beams at the prism/air interface nearest the wafer under measurement. One beam is internally reflected while the other passes out of the prism, reflects off the wafer surface at a high angle of incidence, and again enters the prism to combine with the internally reflected signal(s). This is referred to as a grazing incidence interferometer. The resulting wave exiting the interferometer is picked up by a 32 X 32 array of pixels, integrated over space and time, and stored for computer use.

Figure 1: AUTOSORT'S OPTICAL PATH

![Autosort's Optical Path Diagram]

There are four different criteria for sorting wafers. One of them is Total Indicated Runout (TIR) and is shown in Figure 2. This is a measure of the vertical distance between the lowest and highest points on a wafer's surface. The information it supplies is relative to exposure system considerations in that the depth of focus must be varied to account for all areas on a wafer. Because of this, TIR is the most used flatness criteria in the semiconductor industry today [1].

Figure 2: TIR/FPD SORT CRITERION

![TIR/FPD Sort Criterion Diagram]
A second criteria, Focal Plane Deviation (FPD), is also shown in Figure 2. This measures the largest vertical distance on a wafer surface, being negative or positive, from a specified focal plane. The focal plane is defined by the three Perkin-Elmer Alignment pad locations (Micralign reference pads in Figure 2) on the wafer perimeter, spaced at the vertices of a triangle. A subsequently needed depth of focus could be determined from this criteria.

Percent of Wafer within Depth of Focus (PWI), a third criteria, is a measure of the percentage of wafer that will be within a user specified depth of focus. This is represented in Figure 3. In using projectors for exposure purposes, this criteria could determine the depth of focus limits that can be used with 100% of wafer in focus.

Figure 3: PWI SORT CRITERION

The fourth criteria is Direct Step on Wafer (DSW) test/sort process and simulates, as shown in Figure 4, the exposure of a GCA stepper. The stepper normally refocuses for each step to be exposed on the wafer. Therefore, the Autosort will return the number of steps on the wafer that upon exposure will be 100% within the user specified depth of focus after each stepper refocusing. The number of steps on the wafer is automatically determined prior to measurement based on user entered parameters such as minimum unexposed distance from wafer flat, step size, step centering method, and wafer edge exclusion.

Figure 4: DSW SORT CRITERION
The Autosort Mark II flatness analysis system, using a collimated Helium-Neon laser (633 nm wavelength) as its source, was brought on line. Performance testing was carried out using 15, 3", 10-20 ohm/cm² SEH wafers which were run through the machine 25 consecutive times. During these runs, wafers were sorted according to various degrees of TIR, FPD, PWI, and DSN, but data was collected for all 4 criteria. A program was written to input performance testing results from a number of runs and output the average, standard deviation, and high and low data points for each criteria on each wafer. Autosort plots were also taken.

RESULTS / DISCUSSION

Upon calibration at each new testing session, sensitivity was within the 7.0 +/- 0.2 specified value of a calibration disk. In performance testing, a depth of focus of 1.5 microns was used (determines PWI results). This is a typical value for the GCA stepper that is in operation at RIT. Runout results for the 25 runs showed a superior standard deviation range of 0.46 - 2.61 compared to that of the percentage of wafer in focus test which standard deviation ranged from 1.84 - 10.84. A results summary is shown in table 1.

<p>| TABLE 1: PROGRAM RESULTS FOR 25 CONSECUTIVE RUNS |
|-------------------|-----|-----|-----|</p>
<table>
<thead>
<tr>
<th>Wafer</th>
<th>TIR (um)</th>
<th>FPD (um)</th>
<th>PWI (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.61</td>
<td>4.43</td>
<td>4.55</td>
</tr>
<tr>
<td>2</td>
<td>0.81</td>
<td>0.42</td>
<td>1.84</td>
</tr>
<tr>
<td>3</td>
<td>0.80</td>
<td>2.05</td>
<td>4.11</td>
</tr>
<tr>
<td>4</td>
<td>0.93</td>
<td>3.05</td>
<td>6.35</td>
</tr>
<tr>
<td>5</td>
<td>1.96</td>
<td>4.94</td>
<td>7.44</td>
</tr>
<tr>
<td>6</td>
<td>0.50</td>
<td>4.78</td>
<td>5.56</td>
</tr>
<tr>
<td>7</td>
<td>1.10</td>
<td>3.40</td>
<td>4.12</td>
</tr>
<tr>
<td>8</td>
<td>1.54</td>
<td>6.06</td>
<td>2.76</td>
</tr>
<tr>
<td>9</td>
<td>1.01</td>
<td>5.69</td>
<td>4.27</td>
</tr>
<tr>
<td>10</td>
<td>0.86</td>
<td>3.76</td>
<td>8.25</td>
</tr>
<tr>
<td>11</td>
<td>0.46</td>
<td>3.16</td>
<td>10.8</td>
</tr>
<tr>
<td>12</td>
<td>2.36</td>
<td>5.04</td>
<td>4.54</td>
</tr>
<tr>
<td>13</td>
<td>1.33</td>
<td>1.96</td>
<td>5.60</td>
</tr>
<tr>
<td>14</td>
<td>1.20</td>
<td>4.65</td>
<td>6.32</td>
</tr>
<tr>
<td>15</td>
<td>3.12</td>
<td>5.95</td>
<td>3.77</td>
</tr>
</tbody>
</table>

| Mean  | 1.37    | 3.96    | 5.36   |

The Tektronix Storage Display used by the Autosort will give a three dimensional and two dimensional ('birdseye' view) plot of the wafer surface topography however no hard copy is currently available as the printer in use is not Tektronix compatible.
To assist a user who is unfamiliar with the machine, a guide to start procedures has been written. This is a cross between the user manual and the individual variations of RIT's machine. It will bring the user from the point of arriving at the machine through the testing of the wafers. For more technical information, he/she is referred to the published users manual [2].

Finally, some concern should be given to the actual test area. The blowers on the environmental hood, located over the machine, are in operation however water hookups need to be made for temperature control. The current temperature specifications of the room (mask making area) may prove to be adequate over time however precise temperature (and humidity) control is required for optimum accuracy and run to run conformity.

CONCLUSION

The Autosort Mark II system is now up and running and ready for further testing. Future use may include testing as to how well results of the of flatness testing can be applied toward exposure tool effectiveness. Also, the effects on wafer flatness of various processing steps such as high temperature oxidation can be examined. Eventually, the autosort CPU may be connected on line to the VAX/VMS computer system so that data does not need to be input by hand into appropriate data files for program analysis.

ACKNOWLEDGMENTS

Scott Blondell; for his support in facilities hook up

Charles Thomas; Tropel service representative who aided in the 'fine tuning' of the machine.

REFERENCES


DESIGN, CONSTRUCTION, AND QUALIFICATION OF A CHLORINATED OXIDE GROWTH PROCESS

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ABSTRACT

This project dealt with the design and installation of a TCA bubbler system. Considerations for safety and temperature control of the TCA were simplified by the use of a J.C. Schumacher Flow Temperature Control unit. Installation of the system is complete and chlorinated oxides have been grown.

INTRODUCTION

Wet and dry oxide growth techniques are widely used in semiconductor fabrication. However, there are times when it is desirable to reduce sodium ion contamination and enhance the electrical characteristics of the oxide. This is most commonly done when the oxide is being used as a gate oxide in MOS devices. For this reason, oxidation of silicon in a chlorine-containing ambient can be a very beneficial process step. It is possible to reduce the mobile charges in the oxide by two orders of magnitude, increase the minority carrier lifetime by two orders of magnitude and also grow an oxide with much better integrity thus greatly improving the electrical properties. These benefits are not without some drawbacks to the process. These include increased surface roughness of the oxide, the separation of the oxide from the silicon, the etching of the silicon at the Si/SiO2 interface and the increased radiation sensitivity of devices containing chlorine.[1]

Sodium passivation is the process of immobilizing sodium ions in the gate oxide. Sodium passivation can be achieved with the incorporation of chlorine into the oxidation process two ways. The first is a cleaning of the tube itself. There is a very large potential for sodium contamination in the furnace because at elevated temperatures, sodium can diffuse through the walls of the tube. To decrease the contribution of this, it is necessary to perform a cleaning of the furnace tube, boats, and paddle to remove sodium and other metal ion contaminants. A standard procedure is to clean for 45 minutes at a temperature approximately 100 degrees celsius over standard process temperature in a chlorine ambient. It is possible to decrease the contamination levels even more by increasing the cleaning time. The mobile sodium ions in the oxide are also reduced when chlorine is incorporated into the oxide growth process itself. High temperatures are required for passivation to occur. However, some passivation is seen at temperatures as low as 900
degrees Celsius. For a particular oxidation time and temperature, the amount of passivation is dependent upon the level of chlorine contained in the oxide. The sodium concentration decreases with increasing chlorine concentrations.[2]

The mechanism proposed for the removal of mobile ion contamination is as follows: particles are present on the silicon surface at the start of oxidation. As the oxide is grown, these particles interact causing defects and they are incorporated into the oxide layer. These particles are usually metallic in nature. If the particles are incorporated into the oxide they become sites for breakdown. During oxidation the chlorine combines with the metallic particles to form metal chlorides which are volatile and are desorbed into the gas stream. The sodium is neutralized by the chlorine through the formation of neutral species. Experiments have shown that 1% TCA is the optimum concentration for passivation and increased dielectric strength. At concentrations lower than 1%, not enough chlorine is present. As the concentration exceeds 1%, corrosion of the silicon surface begins to occur.[3]

Localized impurities in the oxide are also causes of low integrity oxides. These impurities are usually sodium. The mechanism of neutralization is not well understood. It is proposed that the mobile ions become trapped when they reach the vicinity of the chlorine, incorporated in a Si-O-Cl bond where chlorine is substitutional for oxygen. Therefore, the trapping and neutralization of sodium ions occurs only at the Si/SiO2 interface.

EXPERIMENTAL

The gathering of the bubbler and needed hardware was made relatively simple by J.C. Schumacher Company. Upon calling the company for technical assistance, they decided to donate a complete TCA bubbler system to R.I.T. This system contained all safety valves and mass flow controllers needed for installation. Included with the system was the microprocessor control unit which contains mass flow controllers for the oxygen and nitrogen, an oxygen sensor and solenoids in the nitrogen lines to shut the system down in case of a decrease in oxygen, and temperature sensors to control the temperature of the TCA. Also included in the system was the bubbler housing which holds a 500 ml bubbler and heats the TCA.

The design considerations were based on what the tube would be used for, who would be using it, and safety considerations. As a gate oxide furnace, it was decided that it should have the capability of growing chlorinated oxides, dry oxides, and it should also be equipped with a nitrogen purge for post-oxidation anneals. Since many students would be using the furnace, the system should also be fairly easy to operate. Lastly, since chlorine is a harmful gas and that TCA breaks down in the tube to
form HCL, a good exhaust system must be placed at the end of the tube.

RESULTS

The TCA bubbler system is installed and running. A schematic of the system is given in figure 1. The system works by bubbling nitrogen through the liquid TCA, which is regulated at 25 degrees celsius. Oxygen is mixed with the nitrogen/TCA at the tube. Flow rates of the gases are regulated by the Flow Temperature Controller (FTC). This unit also contains all oxygen sensors and solenoids to shut the system down in case of a lack of oxygen. A nitrogen purge can also be performed if the FTC is put into standby. To do this, a switch was installed which puts the unit in standby and allows the electric valve to be switched to nitrogen. With the FTC in run mode, the electric valve can only be placed in the oxygen position. The tube has been cleaned with the TCA and oxides grown with the system show an improvement in mobile ion contamination over those grown with dry oxygen only.

CONCLUSION

The TCA bubbler system has been installed and is working as it was designed to. Mobile ions in the oxides have shown improvement, which should make it possible to fabricate better devices here at R.I.T.

ACKNOWLEDGEMENTS

J.C. Schumacher - for their technical assistance and donation of the TCA bubbler system.
Gary Runkel - for help with the installation of the system.
Dave Fatke - for help with the setup.

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Figure 1. Schematic of TCA bubbler system