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Design and Analysis of High Frequency Power Converters for Envelope Tracking Applications

Trevor Chase Smith

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Design and Analysis of High Frequency
Power Converters for Envelope Tracking Applications

By
Trevor Chase Smith

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in
Partial Fulfillment
of the
Requirements for the Degree of
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in
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Abstract

In the field of power electronics, designers are constantly researching new methods to improve efficiency while optimizing dynamic performance. As communication technologies progress we are more often dealing with systems of increasing speed and complexity. For instance, from 1991 to 2013 we have observed the mobile broadband communication sector evolve from ~230 Kbits/s (2G) speeds to ~100 Mbits/s (4G LTE), a 430% increase in communication speed. In contrast, we have not observed the same evolutionary development in industrial power converters. Most switch-mode power supplies are still manufactured for 100 KHz to 800 KHz operating frequencies. The main reason for this is that most electrical devices only require steady-state DC power, so high speed conversion performance is largely unnecessary. But as size expectations for portable electronic devices continue to decrease, the only way to meet future demand is to realize power electronics that operate at much higher switching frequencies. Furthermore there is increasing demand to improve the transient response requirements in processor-based systems and achieve practical envelope tracking in RF communication systems. The most straightforward method of increasing the dynamic response for these systems is to increase the switching frequency of the power electronics in a sustainable and coherent manner.
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<td>Alternating Current</td>
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<tr>
<td>AM</td>
<td>Amplitude Modulation</td>
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<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
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<td>CAD</td>
<td>Computer Aided Design</td>
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<td>CCM</td>
<td>Continuous Conduction Mode</td>
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<td>Current Mode Control</td>
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<td>Maximum Impedance Frequency</td>
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<td>PA</td>
<td>Power Amplifier</td>
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<td>PCB</td>
<td>Printed Circuit Board</td>
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<td>PID</td>
<td>Proportional Integral Derivative</td>
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<td>Pulse Skip Modulation</td>
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Chapter 1: Introduction

1.1. High-Frequency Power Electronics

There are various electronic systems which can benefit from higher speed power designs. One in particular is in the communications industry: RF power amplification. Most RF communication systems use power amplifiers (PA) to convert low-power signals into larger power RF signals for driving the antenna of a specific transmitter. The majority of PA designs utilize switch-mode pulse-width-modulating (PWM) converters as the power source to operate RF amplifiers. Typically, the converter is set to a fixed peak power level, and consequently, waveforms with non-constant envelopes incur an increase in power dissipation during the valley regions of the modulation cycle. This process causes significant efficiency degradation for the overall system.

The solution to solve this problem is known as “envelope tracking.” Envelope tracking works by dynamically adjusting the input supply voltage of an RF PA. The PA is kept in compression over the entire modulation cycle as compared to the “peak compression” method of traditional designs shown in Figure 1.1. The RF signal for this application is typically an amplitude-modulated waveform transmitted at various frequencies dependent on the specific radio design.
To achieve successful envelope tracking, the power supply must be capable of switching at frequencies greater than 5 MHz, as most modern RF waveforms observe a bandwidth of ~1 to 5 MHz. This poses a troublesome problem for power engineers because at these frequencies, the switching loss of conventional “hard-switching” MOSFETs can be quite substantial. This has led designers to pursue “soft-switching” methods to compensate for the efficiency loss at high PWM frequencies. It has also lead to the popularity and industrial development of gallium nitride (GaN) power transistor technologies. These GaN based devices are known to have higher efficiencies, work at higher frequencies, and offer higher power densities as compared to silicon metal-oxide-semiconductor technology.

For conventional “hard-switching” designs, the total power loss can be calculated by determining two critical factors; conducted dissipation, and switching transition loss. Switching losses occur during the devices on-off transition periods. What happens is that the intrinsic capacitance dissipates
stored energy during each switching cycle, resulting in power loss. These losses are generally proportional to the PWM switching frequency of the design. To gain a more comprehensive understanding of the switching loss attained in a PWM converter, the actual design topology should be analyzed, as the mechanism for switching loss can vary by converter topology.

1.2. Thesis Organization

The structure of this thesis is as follows; Chapter 2 covers the basic principles of traditional DC/DC switch mode power supplies (SMPS). The fundamentals covered in this chapter are used to highlight the mechanisms of power loss encountered in traditional converter designs. It also serves as a review of the major topics encountered in power electronic design and implementation. In Chapter 3 the advanced topics of zero-voltage-switching (ZVS) and zero-current-switching (ZCS) are studied. Different gate driving techniques are discussed and a multi-phase ZVS converter architecture is proposed. In Chapter 4, results of modeling, simulations and experiments are presented. A final conclusion discussing the experimental results, simulations, and future work is documented in Chapter 4.
Chapter 2: Conventional DC/DC Converters

2.1. Switching Loss in a Traditional Switch-Mode Converter

For the switching loss analysis, the power loss in typical synchronous “step-up” and “step-down” power stages will be evaluated. These types of topologies consist of high-side and low-side switches that operate in a complementary fashion. When one device is off, the other device is on, and vice versa. The power stage and the associated drive circuitry are often referred to as being in a half-bridge configuration. For either topology, the devices must be prevented from turning on simultaneously. Therefore, a small amount of dead-time is necessary in most practical designs. Dead-time is the length of time that both switches are kept off during a switching cycle.

The analysis of total switching loss is performed by evaluating the turn on, and turn off losses of the high-side and low-side switching elements. Although this chapter focuses on the switching losses encountered in traditional MOSFET technologies, the same fundamental equations can be applied to GaN devices as well.
2.1.1 Turn-on Losses in the High-side Switch

The high side switch is the main power stage in a synchronous step-down converter. The synchronous term is used to describe a technique of replacing a diode stage with an active switching element. In a step-up converter, the high side switch operates as a synchronous rectifier. For both topologies, power losses can be attributed to conduction, switching, and gate charging.

Conduction loss can be described as

\[
P_{\text{cond}} = \frac{R_{\text{on}} \cdot I_{\text{out}}^2 \cdot V_{\text{out}}}{V_{\text{in}}},
\]

(1)

where \( R_{\text{on}} \) is the on-state conduction resistance; \( I_{\text{out}} \) is the RMS drain current; \( V_{\text{in}} \) is the input voltage; \( V_{\text{out}} \) is the output voltage.

The high side switching losses can be analyzed by observing the drain-source voltage and current waveforms during the turn-on and turn-off transitions. Figure 2.1 describes the switching loss waveforms for a traditional “hard-switched” design.

![Figure 2.1: Turn-On Switching Waveforms Observed in SMPS](image-url)
In general, the turn-on power loss can be described as

\[ P_{\text{Switchloss}} = \frac{(t_{\text{sl}} + t_{\text{sh}}) \cdot V_{\text{in}} \cdot F_{\text{sw}} \cdot I_{\text{out}}}{2}, \]

where \( V_{\text{in}} \) is the input voltage; \( F_{\text{sw}} \) is the PWM switching frequency; \( t_{\text{sl}} \) is the low to high transition time; \( t_{\text{sh}} \) is the high to low transition time; \( I_{\text{out}} \) is the RMS drain current.

The high-low and low-high transition times are dictated by the device's gate charge and driver currents defined as

\[ t_{\text{sh}} = \frac{Q_c}{I_{\text{GDH}}} \quad \text{and} \quad t_{\text{sl}} = \frac{Q_c}{I_{\text{GDL}}}, \]

where \( Q_c \) is the total gate charge needed to bring the gate-source voltage through the Miller turn-on region as discussed in Section 2.1.1.2; \( t_{\text{sh}} \) is the high-to-low transition time; \( t_{\text{sl}} \) is the low-to-high transition time; \( I_{\text{GD}} \) is the gate drive current. The total gate charge is normally specified by the manufacturer's datasheet. But the associated driver current must be calculated or measured.

The high side driver gate current, which is the result of the device gate-charge during turn-on and the average high-low transition time, is

\[ I_{\text{GDH}} = \frac{V_G - V_P}{R_{\text{DRV}}}, \]

\[ \text{Section 2.1.1.2} \]
where $V_g$ is the gate drive voltage; $V_p$ is the switch plateau voltage; and $R_{DRV}$ is the series driving resistance.

The power lost in the gate drive circuit is approximated as a function of the total gate charge of each device being driven, as well as the speed of the gate-drive switching frequency. Assuming that the high-side and low-side switches are chosen to be identical, the total gate drive loss is found as

$$P_{gate} = F_{sw} \cdot (Q_{HS} + Q_{LS}) \cdot V_{DR} = F_{sw} \cdot (2Q_C) \cdot V_{DR}.$$

(5)

The gate drive voltage is typically from 5 V to 12 V depending on the MOSFET technology. New designs utilize logic-level devices in order to improve efficiency.

2.1.1.1 Loss Due to Common Source Inductance

The following switching loss analysis extends upon section 2.1.1. It provides a more comprehensive account of the power loss due to common source inductance (CSI). CSI is a path of parasitic inductance that is shared between the high-side gate driver and the main current path. For practical designs, this is a more accurate calculation because CSI is most always a loss factor in PCB design. It is also useful when accounting for loss due to the underlying device geometry of the switching element. The CSI observed in a typical QFN MOSFET package can range from 400 nH to 1000 nH [2].
When power is first applied, the CSI reacts to an initial \( di/dt \) event that reduces the effective gate-source voltage. This voltage, due to CSI, may be represented as

\[
V_{SL} = L_{CS} \left( \frac{di}{dt} \right) = L_{CS} \left( \frac{I_{out} - I_{p-p}}{t_{sH}} \right). \tag{6}
\]

The driver gate current, which is the result of the device gate-charge during turn-on and the average high-low transition time, is calculated as

\[
I_{GDH} = \frac{V_G - V_{SL} - V_p}{R_{DRV}}. \tag{7}
\]

We substitute in the appropriate equation for the CSI, and the gate drive current becomes

\[
I_{GDH} = \frac{V_G - L_{CS} \left( \frac{I_{out} - I_{p-p}}{t_{sH}} \right) - V_p}{R_{DRV}}. \tag{8}
\]

From equation (3) we know the specified high-low transition time takes into account the gate current, so we combine like terms and rearrange to yield

\[
I_{GDH} L_{CS} \left( \frac{I_{out} - I_{p-p}}{2} \right) = I_{GDH} + \frac{V_G - V_p}{R_{DRV}}. \tag{9}
\]
The only difference here is that instead of using the total gate charge, we must use the high-side gate-source charge. Rearranging (9) and solving for $I_{GDH}$, one finds the final gate drive current as

$$I_{GDH} = \frac{V_G - V_p}{R_{DRV} + L_{CS}} \left( I_{out} - \frac{I_{p-p}}{2} \right).$$

(10)

Once the gate driver current is known, the associated switching power loss incurred during the time between device turn-on and the Miller Plateau is

$$P_{\text{Switchloss}} = \frac{V_{in} \cdot Q_{GS} \cdot F_{sw} \left( I_{out} - \frac{I_{p-p}}{2} \right)}{2 \cdot I_{GDH}}.$$

(11)

The switching loss is proportional to the gate charge of the MOSFET as well as the switching frequency of the application.

2.1.1.2 The Miller Gate Charge Effect

The “Miller Effect” is due to the existence of an effective capacitance between the gate and drain of a standard MOSFET. It occurs when the applied gate voltage crosses a device’s turn-on threshold boundary. When this happens, the gate-source capacitance gets charged until the drain current reaches steady state. At this point, a plateau region exists while the gate-drain capacitance is charging, providing a feedback path from the drain to the gate.
This increases the equivalent charge required during each switching cycle [1]. The appropriate gate charge equation depends on the position and operation of the MOSFET, and it is sometimes substituted for the gate-source charge or drain-gate charge in (3).

During the Miller Plateau region, the output capacitance of the low-side FET is charged. This generates a voltage across the parasitic common source inductance ($L_{CS}$) that was represented in (6).

Substituting the equation for high-low transition time from (3) and using the gate-drain charge yields

$$V_{SLP} = L_{CS} \left( \frac{di}{dt} \right) = L_{CS} \left( \frac{I_{GDHP} \cdot Q_{LS}}{Q_{GD}} \right). \quad (12)$$

In a similar manner to the derivation of (10), the gate current during the plateau region becomes

$$I_{GDHP} = \frac{V_G - L_{CS} \left( \frac{I_{GDHP} \cdot Q_{LS}}{Q_C} \right) - V_p}{R_{DRV}}. \quad (13)$$

The result of (13) is used to yield the switching power loss during turn-on of the Miller Plateau region. We have

$$P_{MPloss} = \frac{V_{in} \cdot Q_{GD} \cdot F_{sw} \cdot I_{out}}{2 \cdot I_{GDHP}}. \quad (14)$$
2.1.2 Turn-Off Losses in the High-side Switch

We can calculate the high side switching loss during the turn-OFF period. Figure 2.2 shows the typical waveforms for drain-source voltage (RED), drain current (ORG), and gate voltage (BLUE) during this turn-off period.

![Diagram showing Traditional Switching Loss](image)

**Figure 2.2**: Turn-Off Switching Waveforms Observed in SMPS

Throughout the time-period $t_1$, the gate current is based solely on the induced common-source inductance voltage and the plateau voltage which is equal to the applied gate-source voltage driving the device. One has

$$I_{GDLP} = \frac{V_P - V_{SL}}{R_{DRV}} = \frac{I_{out} - \frac{I_{p-p}}{2}}{R_{DRV}}. \quad (15)$$

We substitute the low-high transition time from (3) into (15). We obtain
Rearranging and combining like terms to separate the gate drive current yields

\[
I_{GDLP} + \frac{L_{CS}}{R_{DRV}} \left( \frac{I_{out} - I_{p-p}}{Q_C} \right) = \frac{V_p}{R_{DRV}}.
\]

Solving (17) for the final gate drive current and simplifying, we have

\[
I_{GDLP} = \frac{V_p}{R_{DRV} + L_{CS}} \left( \frac{I_{out} - I_{p-p}}{Q_C} \right).
\]

This calculation can now be used to estimate the power loss during the Miller Plateau region as

\[
P_{GDLP} = \frac{V_{in} \cdot Q_{GS} \cdot F_{sw} \left( I_{out} + \frac{I_{p-p}}{2} \right)}{2 \cdot I_{GDLP}}.
\]
current is linearly decreasing. We must determine the gate-drive current accounting for CSI, and use this to calculate the power dissipation. In particular,

\[ I_{GDT2} = \frac{-V_p - V_{SL}}{R_{DRV}}. \]  

(20)

The induced voltage due to CSI is identical to the turn-on case. This equation can be solved in the same manner to calculate the power loss for this time period. The losses due to the Miller effect are not encountered during the turn-off period of the switching element. One has

\[ P_{GDT2} = \frac{V_{in} \cdot Q_{GD} \cdot F_{sw} \cdot \left( I_{out} + \frac{I_{p-p}}{2} \right)}{2 \cdot I_{GDT2}}. \]  

(21)

2.1.3 Low-Side Switch Losses

The losses within the low side switch can be attributed to on-state conduction, diode conduction, and gate charge. The main difference, in comparison to the high side switch, is the loss due to the conduction period of the body diode. In a step-down converter, this occurs once the high side device shuts off and the body diode in the low-side starts to conduct, charging the inductor. This is the dead-time during which both devices are turned off and only the lower side body diode is conducting. We have

\[ P_{LS} = V_D \cdot I_{out} \cdot T_D \cdot F_{SW}, \]  

(22)
where $V_d$ is the forward voltage drop of the diode; and $T_d$ is the rising/falling dead-time.

Both the conduction loss and gate charge loss can be described by the same design equations as found in equations (1) and (5).

2.2. Diode Reverse Recovery Effect

Aside from dead-time loss, the switching elements body diode also experiences what is known as reverse-recovery loss. In a step-down topology, this loss occurs as negative current flows through the body diode during the initial turn-on period of the high-side switch.

In various PWM converters, diodes are utilized to rectify switching voltages and manipulate the flow of current by fly-wheeling and clamping. For silicon carbide (SiC) diodes, the junction capacitance causes a difference in charge distribution whenever the device transitions from a conducting to non-conducting state [13]. This charge difference is dictated by the size of the P-N junction area and it is the main cause of reverse recovery loss. Diodes with larger junction areas result in larger reverse recovery current and thus higher power dissipation during state transitions.

As a MOSFET switches states while the body diode is conducting, there is a forced commutation of the diode, causing a conductive to non-conductive transition. In order to avoid this transitional loss, the MOSFET
must remain in the same state when the diode makes the transition. Rectifier diodes are typically designed to minimize the time duration of this transition. This is usually referred to as the devices “reverse recovery time”. This reverse recovery time can be used to calculate the transitional losses incurred in a MOSFET by integrating the power across the device. We have

\[ P_{SW} = \int_{0}^{t_{rr}} (V_{in} - V_{sw}) \cdot F_{sw} \cdot I_{in} dt. \]  

(23)

The specific transitional power loss during the reverse recovery region can be calculated as

\[ P_{drr} = Q_{rr} \cdot F_{sw} \cdot V_{in}, \]  

(24)

where \( Q_{rr} \) is the reverse recovery charge; \( F_{sw} \) is the switching frequency; \( V_{in} \) is the input voltage.

Figure 2.3 shows the expected voltage and current response of a typical rectifier diode. As the diode begins the state transition from forward conduction, it overshoots and reverses direction until it reaches a peak reverse current. It is not until this peak reverse current is reached that the reverse blocking voltage across the rectifier appears and begins supporting reverse voltage [14]. Once the diode current goes negative, it begins acting as an energy source and it delivers energy to the output load.
High voltage boost converters require fast and ultrafast rectifiers to minimize the aforementioned reverse recovery losses. There are several methods designers can use to reduce the effect of reverse recovery time shown in Figure 2.3. One method is to minimize the dead-time for when the MOSFET is off and the body diode is forward conducting. A second method is to slow down the synchronous MOSFET turn-on time which decreases the $di/dt$ slope when the diode changes states. A third method, which is more widely implemented, is to place a high-speed Schottky rectifier diode in parallel with the synchronous MOSFET.

The GaN FETs offer a different mechanism of reverse conduction. Instead of a parasitic bipolar junction used in silicon MOSFET technologies, GaN devices have a completely lateral structure. So in the absence of gate-
source voltage, a positive gate bias is generated by electrons that are injected from under the gate relative to the lateral drift region [15]. Once the threshold voltage of the GaN device is crossed, a conductive channel is formed and the “body diode” conduction effect is established. In comparison to this process, silicon MOSFETs implement diode conduction using minority carriers. These minority carriers are holes that have been injected into the N-side region. When a diode gets reverse biased, it takes time for the minority carriers to be recombined or removed [16]. This process is the main mechanism of reverse recovery loss in silicon MOSFET technologies. Since the GaN process does not implement conduction via minority carriers, the reverse recovery charge is essentially zero. But one disadvantage is that the forward voltage drop of a GaN FET's “body diode” is higher than that of a comparable silicon technology and so it incurs higher diode conduction losses. However, this disadvantage is easily overcome by utilizing an ultrafast Schottky diode in parallel with the synchronous GaN device.

2.3. Control Law Design

The majority of practical DC/DC converter control techniques fall under the methods of current mode control (CMC) and voltage mode control (VMC). Traditional switching power supplies utilize the method of VMC which relies primarily on a simple voltage feedback path as shown in Figure 2.7.
The method of VMC generates a PWM gate drive voltage by comparing an error signal with an internally oscillating ramp waveform. In the simplest of implementations the PWM comparator drives the reset input of an RS latch. Whenever the ramp waveform exceeds the hysteretic limit of the error signal, the RS latch output goes high which turns on the gate of the power-stage MOSFET.

![Diagram of Voltage Mode Control Scheme](image)

**Figure 2.4:** Voltage Mode Control Scheme

The method of VMC is simpler in implementation than that of CMC schemes, but it has several disadvantages including:
1) Two-pole output filter design requires complicated compensation structure at the error amplifier;

2) Control loop gain will vary with input voltage, making it more difficult to ensure stability;

3) Slower dynamic response with regard to line-load disturbances will be experienced because voltage perturbations must be measured at the output before the control loop takes over.

The method of CMC is employed to overcome these disadvantages and it works by implementing the same voltage loop feedback as VMC, but it also includes an inner current loop that is dependent on the average inductor current. Currently there are the following versions of CMC:

1) **Average CMC** – Scaled inductor current is converted to a moving average which is used to track a set reference voltage;

2) **Peak CMC** – MOSFET switches off when the inductor current reaches peak level;

3) **Valley CMC** – Current is measured on the down slope flowing through low side MOSFET;

4) **Sample and Hold** – Can be Peak, Valley, or Average but in all cases the current is sampled with regards to the slope transition of the inductor current. This technique is used in most digital controllers.
In all CMC methods, the inductor current, or low-side switch current, is measured and fed back into a PWM logic comparator. The comparator is typically designed to trip an RS latch whenever the sensed inductor voltage exceeds the level. The specific trip level is dictated by the method of control (peak, valley, average, etc.). Figure 2.8 outlines a basic example of a CMC design.

![Figure 2.5: Current Mode Control Scheme](image-url)
Both VMC and CMC designs utilize the same compensator design techniques in the feedback error stage. Figure 2.6 shows the typical compensation designs found in most control loops.

![Feedback Error Control Stage Diagram]

**Figure 2.6: Voltage Mode Feedback Error Control Loop**

The compensation method traditionally employed in buck and boost converters is proportional-integral (PI) control. PI control can be implemented using analog or digital methods. The transfer function of an analog Type I PI control law is

$$H_I(s) = \frac{1+ sC_{C2}R_{C2}}{sC_{C2}R_{RF1}}.$$  \hspace{1cm} (25)

Modern designs use a parallel capacitor ($C_{HF}$) to add a high frequency pole to the system. The control loop for this method now contains two poles and one zero. This configuration is commonly referred to as a Type II system in reference to the number of poles. The Type II transfer function is
Designs that have widely dynamic input and output conditions may require higher loop bandwidths than can be obtained with Type II compensation. In order to achieve a higher crossover frequency necessary to ensure fast dynamics we must add another pole and zero to the Type II system which provides the additional phase boost necessary to ensure stability. Many SEPIC, Flyback, and buck-boost topologies usually require this type of control. The transfer function is

\[ H_{II}(s) = \frac{1}{s \cdot (C_{C2} + C_{HF}) \cdot R_{F1}} \cdot \frac{1 + s \cdot C_{C2} \cdot R_{C2}}{s \cdot \left( \frac{C_{C2} \cdot C_{HF}}{C_{C2} + C_{HF}} \right) \cdot R_{F1}}. \]  

(26)

\[ H_{III}(s) = \frac{1}{s \cdot (C_{C2} + C_{HF}) \cdot R_{F1}} \cdot \frac{1 + s \cdot C_{C2} \cdot R_{C2}}{s \cdot \left( \frac{C_{C2} \cdot C_{HF}}{C_{C2} + C_{HF}} \right) \cdot R_{F1}} \cdot \frac{1 + s \cdot C_{C1} \cdot (R_{C1} + R_{F1})}{1 + s \cdot C_{C1} \cdot R_{C1}}. \]  

(27)
Chapter 3: Zero-Voltage Switching and Zero-Current Switching Converters

3.1. Introduction

There are various resonant switching techniques designed to mitigate the aforementioned losses incurred in traditional “hard-switching” power designs. Two prominent soft-switching techniques are zero-current switching (ZCS) and zero-voltage switching (ZVS). In this thesis we will be focusing on the more prevalent method of ZVS.

The ZVS technique is achieved by designing the high-side turn-on transition such that the drain-source voltage is nearly zero when the gate-source threshold is crossed. This technique reduces switching losses due to the “Miller Plateau effect”. Figure 3.1 illustrates the waveform differences between traditional “hard-switching” and “soft-switching” ZVS designs during turn-on.
The goal of any ZVS power design is to operate the main power stage switch (or switches) when the drain-source voltage is zero. In practical designs, there is usually some loss encountered during turn-on transition, as the drain-source voltage may not reach zero. Figure 3.2 illustrates the ideal switching waveforms encountered during ZVS operation. $V_{G1}$ is the gate drive voltage for the high side synchronous switch, $V_{G2}$ is the gate drive voltage for the low side power switch, $V_{SW}$ is the switch node voltage, and $I_L$ is the
inductor current. This circuit behavior will be replicated in PSPICE and validated on an experimental prototype in Chapter 4. For multiphase designs, the waveform behavior remains consistent, but the waveforms for each phase will be offset by a certain percentage. In particular, the waveforms will be offset by 180° for two-phase, 120° for three-phase, 90° for four-phase, etc.

![Figure 3.2: ZVS Boost Switching Waveforms](image)

Aside from improving efficiency, resonant switching also reduces both conducted and radiated emissions that often plague traditional PWM
converter designs. This is due to the generation of sharp switch-node ringing edges encountered in “hard-switched” designs.

3.2. Resonant Gate Driving Techniques

Apart from designing a scheme to implement ZVS in the power stage, there are also techniques to recycle power in the gate-driving circuitry. Figure 3.3 shows a standard gate driving configuration for a synchronous step-down converter. This is the aforementioned “hard-switching” half-bridge design that is known to suffer from heavy losses at high switching frequencies.

![Diagram of conventional gate driving scheme for synchronous step-down converters]

Figure 3.3: Conventional Gate Driving Scheme for Synchronous Step-down Converters

The goal of resonant gate driving is to utilize reactive components in the driving stage to recover power during each gating cycle. This recycled
energy is recovered to drive the power stage on the next PWM transition. It is very effective at reducing the losses when operating at high switching frequencies. Most resonant gate drive designs utilize diodes, inductors and capacitors. These inductors and capacitors are the reactive devices used for power recovery. The idea of utilizing resonant gating is traced back to the 1980’s, and, has been the topic of various research papers in academia and industry.

The conventional gating scheme is typically modified by inserting a resonant LC filter at both the low-side and high-side gate locations. The component values are designed to recycle a portion of the power left after each drive cycle.

Figure 3.4: Resonant Gate Driving Scheme for Synchronous Step-down Converters
The theoretical switching loss in a MOSFET is found by quantifying the gate-drive current used to turn the device on and off. In analyzing the efficacy of a resonant gating scheme, we determine what the gate drive current is while implementing the reactive components as shown in Figure 3.4. The configuration of these components results in a set of second-order LC differential equations;

\[ v_{CR}(t) = V_{LOL} - L_R \frac{di_{gate}}{dt} - R_s \cdot i_{gate}, \quad (28) \]

\[ i_{gate} = C_R \frac{dv_{CR}}{dt}. \quad (29) \]

By differentiating (28), we have a second order linear homogeneous equation

\[ L_R \frac{d^2i_{gate}}{dt^2} + R_s \frac{di_{gate}}{dt} + \frac{i_{gate}}{C_R} = 0. \quad (30) \]

The solution of this differential equation will give us the damping coefficient, resonant frequency, and natural frequency of the gate drive circuit. One has

\[ i_{gate}(t) = e^{\alpha t} \left( A_1 \cos(\omega t) + A_2 \sin(\omega t) \right). \quad (31) \]

The damping coefficient \( \alpha \) is related to the equivalent series resistance and resonant inductance as

\[ \alpha = \frac{R_s}{2L_R}. \quad (32) \]
The resonant frequency is given by

$$\omega = \sqrt{\frac{1}{L_RC_R - \frac{R_s^2}{4L_R^2}}}.$$  \hspace{1cm} (33)

The $A_1$ and $A_2$ coefficients in (31) must satisfy the initial conditions of the system. Once the initial conditions are known, $A_1$ and $A_2$ can be found for by taking the first derivative of (31) and simultaneously solving that system with the original gate current at time $t = 0$. We have

$$\frac{di_{\text{gate}}}{dt} = e^{\omega t} \left[ (\omega A_2 + \alpha A_1) \cos(\omega t) - (\omega A_1 - \alpha A_2) \sin(\omega t) \right].$$  \hspace{1cm} (34)

We assume that the inductor stores an initial current, $I_{\text{INIT}}$, and the output capacitor stores an initial capacitor voltage, $V_{\text{INIT}}$. Solving (34) at $t = 0$ gives us the $A_1$ as

$$A_1 = I_{\text{INIT}}.$$  \hspace{1cm} (35)

Substituting expression (35) into (34) and solving for $A_2$ at $t = 0$ gives

$$\frac{di_{\text{gate}}}{dt} = \frac{V_{\text{LOL}} - V_{\text{INIT}} - R_s A_1}{L} = \left[ (\omega A_2 + \alpha I_{\text{INIT}}) \right],$$  \hspace{1cm} (36)

$$A_2 = \frac{V_{\text{LOL}} - V_{\text{INIT}} - (L \cdot \alpha + R_s) I_{\text{INIT}}}{L \cdot \omega},$$  \hspace{1cm} (37)

$$A_2 = \frac{V_{\text{LOL}}}{L_R} - \frac{V_{\text{INIT}}}{L_R} - \left( \frac{R_s}{2L_R} + \frac{R_s}{L_R} \right) I_{\text{INIT}},$$  \hspace{1cm} (38)

$$A_2 = \frac{1}{\sqrt{L_RC_R - \frac{R_s^2}{4L_R^2}}}. $$
\[ A_2 = \frac{V_{LOL} - V_{INIT}}{L_R} - \left( \frac{R_i}{2L_R} + \frac{R_s}{L_R} \right) I_{INIT} \]  
\[ = \frac{1}{2L_R} \sqrt{\frac{4L_R}{C_R} - R_s^2} \]  
\[ A_2 = \frac{2V_{LOL} - 2V_{INIT} - 3R_s \cdot I_{init}}{\sqrt{\frac{4L_R}{C_R} - R_s^2}} \]  

3.3. High Side Gate Driving

Synchronous boost, buck, and buck-boost converters utilize switching elements with floating source connections. The voltage at this source “reference” connection is dependent on the state of the switch, input voltage, output voltage, and output current conditions. This part of the power stage is referred as the “high-side” switch. Proper operation requires specialized gate drive circuitry to maintain appropriate turn-on bias as the source reference voltage varies during each switching cycle.

Most industrial methods for high-side gate driving rely on the use of bootstrap circuit designs. A bootstrap circuit utilizes a diode and capacitor to cycle energy at the precise time when the high side switch needs to be turned on. A typical bootstrap circuit for a boost converter application is shown in Figure 3.5. Although this implementation is for a boost converter, the same technique is used for buck and buck-boost topologies as well. The bootstrap capacitor gets charged when the switch-node is pulled to ground through a
bootstrap diode which is connected to an internal bias supply. Once the switch node is high, the bootstrap diode reverses bias and blocks the capacitor voltage. The capacitor then discharges through the high side driver and provides a floating boost supply. The capacitor must be designed to provide enough energy for the driver to fully turn-on the high side switch during this transition. The bootstrap capacitor is typically in the range of 0.047 μF to 0.22 μF.

![Diagram](image-url)

**Figure 3.5**: High Side Bootstrap Circuit in a Boost Converter Application

One limitation of the bootstrap method is that it requires the switching clock to implement a minimum switch off time in order to recharge the bootstrap capacitor. This burden limits the maximum possible duty cycle of the design, meaning limitations between input and output voltage range. But the advantage of this method is its simplicity, low cost, and small footprint.
area. The majority of industrial controllers implement this method internally and the designer selects an appropriate diode and capacitor for the end application.

Another simple implementation that achieves a floating gate supply is to use a transformer-coupled driver. Transformers offer noise immunity, isolation, high-speed operation, and enable higher duty cycles. Of the various coupled gate drive transformer designs, one of the more prominent solutions is shown in Figure 3.6. The gate drive design is implemented for a boost converter topology. The design uses coupling capacitors on both sides of the transformer to provide an isolated gate drive voltage that is proportional to the duty cycle of the high-side driving waveform.

![Figure 3.6: Transformer Coupled Gate Drive in a Boost Converter Application](image-url)
The voltage across the primary side coupling capacitor can be calculated as

\[ V_{C1} = V_D \cdot D, \quad (41) \]

where \( V_D \) is the high side gate driving voltage from the controller; and \( D \) is the duty cycle of the gate driving waveform.

The coupling capacitor provides a reset voltage for the magnetizing inductance of the primary winding. The purpose of this capacitor is to prevent the transformer from saturating [18]. On the secondary side of the transformer, a common DC restore circuit guarantees proper gate drive voltage of the high-side MOSFET. This circuit is composed of another coupling capacitor C2, and a clamping diode D1, which enable operation over duty cycles greater than 85%.

In designing a transformer-coupled gate drive, the coupling capacitors act as high-pass filters with corner frequencies that are dependent on the input impedance of the output load [18]. The transformer must be designed to achieve impedance matching and voltage isolation. Typically the gate drive transformer is designed as a pulse transformer with fast rise and fall times, minimum overshoot, low leakage inductance, and minimal winding capacitance.

The following analysis details the steps for designing a suitable gate drive transformer for a boost converter operating at 5 MHz. We first analyze
the load as seen by the secondary side of the transformer. This capacitive load can be modeled by the equivalent gate-source capacitance of the high side MOSFET as

\[ C_{\text{EQ}} = \frac{Q_G}{V_G}, \]  

where \( Q_G \) is the total gate charge of the MOSFET; and \( V_G \) is the required gate-source voltage to turn on the MOSFET.

Ideally the pulse from the high side driving waveform should maintain a rectangular shape as it transfers energy to the secondary side winding. In reality, there is a voltage “droop”. The desired allowable voltage “droop” is used to calculate the transformers magnetizing inductance. The larger the magnetizing inductance is, the lower the percentage of voltage droop as defined by

\[ PD_{\%} = \frac{R_s \cdot t_{\text{pw}} \cdot K}{L_{\text{MAG}}}, \]  

where \( K \) is the coupling coefficient; \( L_{\text{MAG}} \) is the magnetizing inductance; \( t_{\text{pw}} \) is the pulse width of the input voltage waveform; and \( R_s \) is the input source impedance to the primary winding.

The high permeability transformer’s core results in high magnetizing inductance while using fewer turns. Transformers with higher magnetizing inductance will encounter less voltage droop as inferred in (43). Ferrite is the
most common core choice in the majority of industrial designs. Once the transformer specifications are developed, and, a suitable device is chosen, we simulate the design in PSPICE to verify theoretical performance. Figure 3.7 shows the realized SPICE schematic used to validate our transformer gate drive specifications.

![High Side Gate Driving](image)

**Figure 3.7:** SPICE Schematic for Transformer Coupled Gate Driving

The simulation results confirm a 5 V gate-source driving voltage is achieved at the high-side MOSFET for a boost converter operating at 5 MHz. Figure 3.8 shows the waveform captures of a single PWM pulse. Here, \( V_D \) is the initial driving voltage from the controller (~5 V), \( V_{sw} \) is the switch-node voltage for a 10 V to 33 V boost operation, and, \( V_{GD} \) is the gate drive voltage measured at the high-side switch.
3.4. Proposed Digital Zero Voltage Switching Controller

The proposed controller is designed to achieve ZVS operation at all input and output load conditions. The goal is to operate the converter power stage such that it follows the discontinuous conduction mode (DCM) / continuous conduction mode (CCM) boundary. It has been shown that during this boundary mode operation, the converter operates much like a quasi-resonant converter without the requirement of adding an external resonant tank circuit. In order to maintain the ZVS operation, an adequate control scheme must be implemented. We use a digital controller that will allow for the implementation of an adaptable algorithm capable of controlling the timing
configuration required for all the power stage switching elements, as shown in Figure 3.9.

![Figure 3.9: Block Diagram of Proposed Digital ZVS Two-Phase Converter](image)

### 3.4.1 Envelope Detection of an Amplitude Modulation RF Signal

Amplitude modulation (AM) is a radio broadcast technique used to transmit information by combining a baseband message with a carrier waveform. The signal strength of the carrier waveform is typically varied in proportion to the baseband message, encoding the transmitted information.

To achieve successful envelope tracking, the envelope tracking modulator must be supplied with an accurate envelope of the AM RF signal. To minimize the effects of interference, impedance mismatch, and parasitic losses, the envelope detection circuit should reside in close proximity to the envelope tracking modulator.
Shown in Figure 3.10 is the input of an RF PA being routed to an envelope tracking assembly. The first stage of this assembly consists of an envelope detection circuit that demodulates the RF signal. This envelope is then used as an input variable to vary the duty cycle of the PWM drive signals within the envelope tracking power stage.

The bandwidth of an AM signal over a given period is calculated as two times the highest modulating frequency during that time. It is the amount of space within the frequency spectrum that is occupied by the AM signal. For instance, if a 100 MHz carrier is modulated by a 10 MHz message signal, this creates sideband frequencies to appear at 90 MHz and 110 MHz. These sideband frequencies span 20 MHz in the spectrum and thus the bandwidth of the signal is 20 MHz.

Using FIR compiler IP’s, most modern FPGA solutions can easily employ Hilbert transforms that can be used to extract the envelope waveform of an AM signal. But for the majority of applications simple low-pass filtering techniques are sufficient.
Various analog solutions also exist for extracting the envelope of an RF signal. One example is the ADL5511, which is a peak RMS detector capable of extracting RF envelopes with bandwidths up to 130 MHz, and can operate at input frequencies up to 6 GHz.

3.4.2 Bandwidth Reduction

If the ET modulator is not capable of tracking the bandwidth of the input envelope signal, it must be conditioned with a low-pass filter to reduce the bandwidth to an appropriate level. Careful consideration must be given when applying this technique because a relationship exists between the effective efficiency of the ET system and bandwidth reduction that can be realized. If the bandwidth of the envelope signal is reduced too far, there will be little overall system level efficiency improvement to warrant the complexity and
cost of implementing the proposed ET solution. Various bandwidth reduction techniques have been shown to introduce memory effect distortion into the RF output of the PA which must be compensated by using pre-distortion on the RF input signal [17].

Any bandwidth reduction technique must guarantee that the new output amplitude does not fall below the original envelope amplitude, or, clipping and distortion at the output of the PA will occur. Low pass filtering may not always satisfy this condition and so other methods may be needed. In [17] a method was introduced to achieve this by creating an envelope difference signal which is rectified and added back to the filtered envelope amplitude. This process is iterated to insure the new reduced bandwidth envelope is always greater in magnitude than the original input envelope. Figure 3.11 displays the SIMULINK model that was developed to extract the peak envelope signal of a single-tone AM modulated waveform.

![Figure 3.11: AM RF Signal Generation and Envelope Detection Simulink Model](image-url)
Figure 3.12 displays the extracted envelope for a single tone input AM signal consisting of a 5MHz carrier modified by a 1MHz message signal.

**Figure 3.12**: Output Scope Envelope Waveform and Original Single-Tone AM Signal
Chapter 4: Experimental Results and Simulations

4.1. Introduction

Various MATLAB and PSPICE simulations were performed to evaluate the performance enhancements of a ZVS boost converter. Experimental prototypes were developed to justify our results. The equivalence of simulation and experimental findings confirm the gate charge, gate driving, ZVS boost operation, closed loop control schemes and other major results.

4.2. Closed Loop Simulations

As a transient response comparison, an ideal boost converter was developed in SIMULINK with Type II and Type III control schemes. The block diagram is shown in Figure 4.1.
The simulation was performed to compare the start-up differences between the two control methods. It is shown that the transient response is much faster when employing an optimized Type III compensator. Figure 4.2 compares the difference between the start-up transient responses for Type II and III compensators.
Ideally, the converter output should be invariant during load transients. To evaluate the differences between the Type II and III compensators, the SIMULINK model was updated to apply a load step of 0.5 A to 1.5 A. Figure 4.3 shows the transient response of both compensators, where the Type III compensator is revealed to have much better dynamic performance.

**Figure 4.2: Start-up Transient Response of Type II and III Compensators**

**Figure 4.3: Load Step Transient Response of Type II and III Compensators**
4.2.1 Inductor Current Sensing

A method for sensing inductor current was developed in [21]. It uses a simple comparator circuit to sense the current across an inductor, and, can be used to provide an amplified voltage to the PWM logic circuit. This method is used in order to maximize system efficiency. Figure 4.4 illustrates the analog circuit used for sensing inductor current.

![Diagram of inductor current sensing circuit](image)

**Figure 4.4:** Technique for Sensing Inductor Current.

4.3. Simulation and Modeling of Half-Bridge Gate Drivers

Various EPC GaN devices are analyzed and evaluated. The goal is to compare the power savings in silicon MOSFET and GaN devices within “hard-switching” operations. PSPICE Orcad modeling software was used to observe $dv/dt$ and $di/dt$ switching intervals and slew rates at various switching frequencies. This analysis gives insight into the losses observed at various switching frequencies using different devices. Major manufacturers
typically provide PSPICE transient models for their components as reported in Table 4.1.

<table>
<thead>
<tr>
<th>Device</th>
<th>Rating</th>
<th>RDSon</th>
<th>Gate Charge</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPC2015</td>
<td>40V at 33A</td>
<td>3.2mOhm</td>
<td>10.5nC</td>
</tr>
<tr>
<td>EPC2020</td>
<td>60V at 60A</td>
<td>2mOhm</td>
<td>16nC</td>
</tr>
</tbody>
</table>

**Table 4.1:** EPC GaN Devices for Evaluation

For consistent comparison of GaN device, comparable MOSFETs were selected and tested. These devices were chosen from a leading industrial manufacturer using total gate charge as the selection criteria. The devices, documented in Table 4.2, were chosen in order to attain minimal switching losses.

<table>
<thead>
<tr>
<th>Device</th>
<th>Rating</th>
<th>RDSon</th>
<th>Gate Charge</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD87350</td>
<td>30V at 30A</td>
<td>2mOhm</td>
<td>20nC</td>
</tr>
<tr>
<td>CSD18537N</td>
<td>60V at 54A</td>
<td>11mOhm</td>
<td>14nC</td>
</tr>
</tbody>
</table>

**Table 4.2:** State-of-the-Art MOSFET Devices for Evaluation

The PSPICE simulations were performed using device models provided by Texas Instruments and Efficient Power Conversion (EPC). Coherent simulation co-design is a valuable tool for analyzing new switching topologies. By predicting device performances, time and effort can be saved before conducting experiments. Our studies of switching loss are widely affected by the intrinsic capacitance in each switching stage. An accurate capacitive model is essential. The capacitive PSPICE models for the
The schematic model shown in Figure 4.6 was developed to simulate, verify, and analyze the gate charge waveforms for the supplied vendor models.

**Figure 4.6:** Measuring Gate Charge Waveforms with Vendor Models
The drain-source and gate-source voltage waveforms were captured during the turn-on transition region in order to analyze and verify the existence of the “Miller” plateau. Figure 4.7 and 4.8 display the gate charge simulation results for the studied MOSFET and GaN FET respectively.

**Figure 4.7**: PSPICE Gate Charge Simulation for CSD18537N MOSFET 40V at 2A

**Figure 4.8**: PSPICE Gate Charge Simulation for EPC2020 GaN FET 40V at 2A
4.4. Experimental Verification of GaN Technology

For the GaN device experiments, two different evaluation platforms were tested: (1) The EPC9001 40 V half-bridge platform shown in Figure 4.9; (2) The EPC9033 60V half-bridge platform shown in Figure 4.10. With the EPC evaluation modules, the power stage still needs to be designed and integrated in order to create a synchronous step-down or step-up converter. The power stage was created as a separate module attachment with each one designed using vector board to achieve approximately 40% inductor ripple current and 50 mVpp output ripple voltage which are typical design specifications for most low voltage buck and boost converters. The power stage module includes input bulk capacitance, output bulk capacitance, and the main switching inductor.

Figure 4.9: EPC9001 Half-Bridge GaN Module in a Step-down Converter
To validate the manufacturer transient models, an experiment was performed to capture actual gate charge waveforms using a dc current source generator to drive the gate of each device under test. The test setup used to perform this experiment is illustrated in Figure 4.11. These waveforms confirm the simulation results observed in Figures 4.7 and 4.8.

The experimental gate charge waveforms shown in Figure 4.12 confirm the PSPICE simulation results from Section 4.3.
Figure 4.12: Experimental Gate Charge Waveforms: (a) GaN EPC2020; (b) MOSFET CSD18537N

The “hard-switching” efficiency degradation for GaN and MOSFET devices were measured at various switching frequencies as specified by the test setup in Figure 4.13. The results in Figure 4.14 show a linear relationship between system efficiency and switching frequency for a 24 W step-down converter. This data was gathered at a 40% PWM duty cycle with $V_{in} = 20 \text{ V}$, $V_{out} = 8 \text{ V}$ and $I_{out} = 3 \text{ A}$.

Figure 4.13: Test Setup for Efficiency Evaluation
As the MOSFET devices are not recommended to operate at high frequencies, the switching losses for these devices were tested up to 1800 KHz as indicated by the dashed line in Figure 4.14.

To observe the difference in losses between gate-drive and switching loss for the lowest (300 KHz) and highest (2 MHz) switching frequencies a thermal camera was used to measure the board temperature during the test. Figure 4.15 shows that the majority of loss is due to the high-side device as well as the gate drive charging circuitry. The thermal captures report temperature in Celsius of the raw board, the high-side GaN device, and the LM5113 gate driver. It is deduced that soft-switching the high-side element is more critical. At lower switching frequencies 1 MHz to 5 MHz, the low-side switch may not require a resonant soft-switching implementation.
The results displayed in Figure 4.14 show an efficiency improvement of GaN technology over MOSFETs at both low and high switching frequencies under nominal load currents. As described in Section 2.1, most synchronous buck converters experience switching loss from the CSI encountered in the board layout and parts placement design stages. In contrast, the evaluated GaN devices achieve much lower CSI. The reason for this is that the lateral structure of the GaN devices allow for all the drain-source connections to be made on the side of the die that mounts directly to the PCB [22]. In doing so the CSI is inherently minimized. In recent years, major MOSFET manufacturers have recognized the CSI problem encountered in common power stage topologies, and have devised ways to minimize this loss by
incorporating two enhancement mode MOSFETs within a single device package size [2]. One example of this is TI’s NexFET™ PowerStack™ technology. This device uses very low resistance copper clips fabricated on the die to connect the high-side source to the low-side drain in order to ensure minimal CSI effects. Figure 4.16 shows TI’s graphical outline of this packaging method.

![Figure 4.16: TI NexFET™ Power Block Technology Dual MOSFET Package](image)

**Figure 4.16:** TI NexFET™ Power Block Technology Dual MOSFET Package

![Figure 4.17: TI NexFET™ Power Block™ Evaluation Platform TPS53819](image)

**Figure 4.17:** TI NexFET™ Power Block™ Evaluation Platform TPS53819

The original efficiency experiment in Figure 4.14 compared new GaN technology to a single package industrial MOSFET. In order to do a more appropriate comparison of the latest technologies, we analyze and compare
the aforementioned Power Block™ design to the results obtained from using GaN FETs. The outcome will define the advantages of GaN technology, and, show that clever MOSFET packaging techniques may overcome the cost disadvantage of current GaN devices for certain applications. Figure 4.17 shows the NexFET™ switching platform that is used for evaluation and comparison of the studied GaN devices. Circled in red is the dual MOSFET package in a 5x6mm SON footprint area.

The initial efficiency measurements are taken under the typical nominal load conditions under which industrial manufacturers usually report performance data. The following experiment was performed to evaluate the efficiency performance across the entire operating envelope. We measure performance metrics under various input and output conditions. The three variables are the output voltage $V_{out}$, output current $I_{out}$, and input voltage $V_{in}$. The output voltage variable is treated as static. The system is designed to regulate this $V_{out}$ variable to a constant 8 VDC. We then evaluate the efficiency performance as a surface function guided by the dynamic relationship between output current $I_{out}$ and input voltage $V_{in}$.

Figures 4.18 and 4.19 show the efficiency surface plots in 3D at 300 KHz and 900 KHz, respectively. Here, 900 KHz is the upper recommended frequency of operation for the studied MOSFETs. The yellow-pink surface plot shows the efficiency curves for the EPC9033 platform, while, the blue-
green surface represents data gathered for the CSD87350 platform. At ~0.6 A the outputs of the two surface plots intersect. The intersection line represents the input/output load conditions where the EPC9033 GaN design begins showing improvement over the CSD87350 MOSFET design. The GaN devices only provide better efficiencies at higher output power levels (>6 W). At low output load conditions, the MOSFET achieves better efficiency performance.

![Efficiency Surface Plot GaN vs MOSFET at 300KHz](image)

**Figure 4.18:** 300 KHz Efficiency Surface Plots of EPC9033 (Yel-Pk) vs. CSD87350 (Blu-Grn)

At higher frequencies, the same observation holds true. However, the margin is smaller. We observe that GaN surpasses the NexFET performance at powers greater than 10 W. The importance of this result is dependent on the design. If a design is expected to operate at low idle power for any
reasonable amount of time, EPC GaN technology may not be an appropriate solution. If the design is consistently operating at high output powers, the improvement in efficiency is \( \sim 4.8\% \) at output currents greater than 2 A.

![Efficiency Surface Plot GaN vs MOSFET at 900KHz](image)

**Figure 4.19:** 900 KHz Efficiency Surface Plots of EPC9033 (Yel-Pk) vs. CSD87350 (Blu-Grn)

### 4.5. Simulation and Modeling of a Zero Voltage Switching Boost Converter

Using the vendor-supplied PSPICE models, simulations are performed according to the power stage design calculations. The OrCAD simulation platform is developed to provide a means for component selection and theoretical parameter validation. Figure 4.20 shows the PSPICE schematic for a two-phase boost converter. The high-side synchronous switches are
operated using the transformer coupled gate drive method discussed in Section 3.3.

![ZVS Two Phase Boost Converter](image_url)

**Figure 4.20:** PSPICE Schematic for ZVS 2-Phase Boost Converter

The critical switching waveforms are shown in Figure 4.21. The results confirm ZVS operation for a 30 W two-phase boost converter. The low side gate in each phase is held off until the inductor current reverses direction, at this point the switch-node voltage reaches 0 V and the low-side gate is turned on, minimizing switching power loss.
4.6. Experimental Results for a ZVS Boost Converter

For the experimental prototype, various EPC GaN FETs were evaluated in a boost configuration at different switching frequencies. The design specifications for the experimental prototype are reported in Tables 4.3 and 4.4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Vin</td>
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<td>V</td>
</tr>
<tr>
<td>Vout</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>Iout</td>
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<td>A</td>
</tr>
<tr>
<td>Fsw</td>
<td>5</td>
<td>MHz</td>
</tr>
</tbody>
</table>

Table 4.3: Input/Output Boost Converter Specifications
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>2222SQ-161J</td>
<td>160 nH RF Inductor</td>
</tr>
<tr>
<td>Q1-Q4</td>
<td>EPC8009</td>
<td>60 V 2.7 A GaN FET</td>
</tr>
<tr>
<td>C1-C4</td>
<td>06031A101JAT2A</td>
<td>100 pF Ceramic Capacitor</td>
</tr>
<tr>
<td>U1</td>
<td>UCC27611DRV</td>
<td>High speed gate driver</td>
</tr>
<tr>
<td>M1</td>
<td>PFD2014</td>
<td>Gate Drive Transformer</td>
</tr>
</tbody>
</table>

**Table 4.4: Input/Output Boost Component Identification**

The experimental prototype was fabricated using standard FR4 material using four PCB layers. Figure 4.22 shows the top and bottom sides of the populated PCB and the associated layout routing design.

![PCB Front and Back](image)

**Figure 4.22:** 30W Multiphase ZVS Boost Converter Prototype and Layout Design

Performance was studied at 1 MHz and 3 MHz, respectively. The prototype was designed to utilize two boost phases operating 180 degrees apart. Figure 4.23 and 4.24 display the critical waveforms for a single phase.
operating under ZVS conditions at 1 MHz and 3 MHz, respectively, at ~15 W output power.

**Figure 4.23:** ZVS Boost Converter Switching Waveforms at 1 MHz

**Figure 4.24:** ZVS Boost Converter Switching Waveforms at 3 MHz
The efficiency improvement between the ZVS boost converter and a traditional hard-switched boost converter is shown in Figure 4.25. The ZVS operation provides from 6% to 10% efficiency improvement over standard hard-switched configurations.

![Efficiency Curves for 30W Boost Converter](image)

**Figure 4.25:** Efficiency Curves Comparing ZVS vs. Hard-switched Boost Converter.

### 4.6.1 Closed Loop System and Frequency Response

Closed loop control was implemented digitally using a C2000 embedded microcontroller. The type II and type III compensator designs reported in Section 4.2 were the SIMULINK/MATLAB models used for comparison purposes to the experimental data. The experimental results are comparable.
and tested against the simulation experiments from Section 4.5. Figures 4.26-4.27 display the loaded and unloaded transient response plots for the ZVS step-down converter operating at 500 KHz and 1 MHz, respectively. A stepped electronic load of 3 A is applied to the system to classify the dynamic performance.

Closed loop control was employed using a third order compensator. The digital compensators are realized using an IIR filter with coefficients that can be tuned in real-time to allow for direct comparison and evaluation. The discrete time difference equation for the compensator structure is given as

\[ u(k) = u(k-1) + b_0 y(k) + b_1 y(k-1) + b_2 y(k-2). \]  

(44)

Figure 4.26: Optimized Transient Response for Digital Step-Down Converter Operating at 500 KHz with 3A Output Loaded (a), and, Unloaded (b), Under Type III Compensation.
Figure 4.27: Optimized Transient Response for Digital Step-Down Converter Operating at 1MHz with 3A Output Loaded (a), and, Unloaded (b), Under Type III Compensation.

One of the advantages of using a digital controller is the ability to obtain frequency response data. Since the compensator is implemented digitally, frequency response measurements can be taken without the need for acquiring an external network analyzer. The control law coefficients can be updated in real-time allowing direct evaluation of parameters. Various control law compensators including Type I, Type II, and Type III can be evaluated simply by updating code builds.

To ensure close-loop system stability, the controller was operated in open loop and a frequency response plot was captured. This data is used to obtain the transfer function of the power stage plant. By evaluating the open-loop plant response in MATLAB, a three-pole three-zero compensator is developed to achieve the desired crossover frequency and stability phase.
margin. The design coefficients were programmed into the MCU and then the frequency response for the compensated closed loop system was captured.

Figures 4.28 and 4.29 report the pole/zero placement design parameters. These feedback coefficients were used to achieve stable operation for the 500 KHz and 1 MHz designs.

**Figure 4.28:** Pole Zero Placement Coefficients for 500KHz Frequency Response

**Figure 4.29:** Pole Zero Placement Coefficients for 1MHz Frequency Response

Figure 4.30 displays the magnitude and phase response of the open loop plant in red, while the compensated system response is shown in blue. The switching frequency for this experiment is 500 KHz.
Figure 4.30: Magnitude and Phase Frequency Response Plots for 500 KHz Operation

Next the compensator coefficients for the 1 MHz system are evaluated. Figure 4.31 reports the magnitude and phase response with a crossover frequency \(\sim 11\) KHz for the faster system.
The use of digital frequency response data can enable diagnostics and adaptive tuning systems at trivial additional cost. The method of digital frequency domain analysis is especially useful for more complicated power stage topologies such as the SEPIC, Cuk, and Flyback designs where wide input/output voltage ranges may cause difficulty in maintaining stability at certain load conditions.
4.7. Conclusion

4.7.1 Summary

This thesis examines various topics in the design, analysis, and application of high performance industrial DC/DC converters. A method of achieving resonant power conversion by controlling the discontinuous/continuous mode boundary is implemented and examined using an experimental hardware prototype.

In Chapter 1, the theoretical framework, relevant to the loss mechanism for typical synchronous step-up and step-down converters is discussed. The main causes for switching losses are studied. An understanding of these fundamental topics is critical to realizing hardware designs that improve performance, transient response, efficiency, and robustness.

In Chapter 2, different methods of ZVS operation are discussed. The critical aspects required to maintain and realize a hardware prototype are identified. The method of boundary mode ZVS operation can be implemented in a wide range of power stage topologies including buck, boost, SEPIC, buck-boost, etc. Designs that require high speed multi-megahertz switching speeds can achieve greater efficiency when realizing ZVS power stage techniques.
Chapter 3 outlines the design specifications for a digital two-phase boost converter operating at 5 MHz. A digital controller implementing a soft-switching ZVS algorithm is proposed. Closed-loop control is designed and developed to obtain a Type III compensator feedback loop. A method for envelope detection is presented and simulated in MATLAB.

In Chapter 4 simulation results are presented and compared against a hardware prototype for the designed boost converter. The 30 W digital ZVS converter was developed to achieve approximately 8% efficiency improvement over the traditional “hard-switched” designs. In open-loop, the system is capable of switching at frequencies higher than 5 MHz, enabling envelope tracking operation. In closed loop, the system is limited by the response time of the digital controller allowing for a maximum frequency of 2 MHz. The limitations of the embedded controller are due to the system clock of the processor and the sampling rate of the onboard analog-to-digital converters (ADC). A MCU with a 60 MHz clock and onboard ADCs with 4 MSPS sampling rates were used for these experiments. The same fundamental principles can be implemented in the future with a faster MCU in order to achieve performance at higher switching frequencies.
4.7.2 Proposal for Future Work

At very high switching frequencies a power electronics design must be studied as an RF circuit. Special attention must be paid to layout, part placement and selection, input/output impedance matching, connector and cabling design, transmission losses, etc. There is much future work on the design optimization for application-specific magnetics, design layout, and mechanical connector design.

For the power stage switching elements, commercial off-the-shelf components were selected for use within the hardware prototype. Efficiency can be improved by redesigning the power stage switch to minimize common source inductance and increasing the gate turn on-off transition speeds.

For the proposed digital controller, MATLAB was used to develop the ZVS algorithms and control loop compensators. This system was implemented using the embedded coder toolbox and transferred to a C2000 evaluation platform to drive the power stage switching elements. The next step for continuing this work would be to port this algorithm development to a suitable FPGA which can provide faster switching speeds.

Much work can be done in the trade-off study and selection of which digital hardware method would most benefit a digital HF and VHF power converter. In recent years the cost, size, and power requirements of FPGA
solutions has decreased dramatically. Future development and realization of a hardware prototype using an embedded FPGA solution are envisioned.
Bibliography


