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Analytical and numerical modeling, fabrication and RF measurement techniques for RF planar micro-inductors on silicon

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Analytical and Numerical Modeling, Fabrication and RF Measurement Techniques for RF Planar Micro-Inductors on Silicon

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ABSTRACT

In mixed signal integrated circuits, the role of passives has become increasingly important. In particular, the characterization and implementation of an embedded planar coil inductor presents several challenges. The present work is a comprehensive study of micro inductors that includes analytical modeling, numerical simulation, in-house fabrication processes, circuit implementation in silicon, and RF measurement techniques.

Although the inductor is widely integrated on silicon, there is still a need for closed form expressions for inductance and the quality factor. In addition, amongst the numerous commercially available simulation packages, there still is a need to identify the tool that best suits the design and implementation of micro-inductors on silicon. In this work, an analytical model is presented based on a desegmentation technique, which removes segments from a rectangular cavity to create the inductor coil geometry. Defining the Green's function for each segment, the boundary conditions are applied to obtain a closed form expression for the Z matrix from which the inductance and Q have been obtained. For a numerical modeling, Ansoft's High Frequency Structure Simulator (HFSS) is chosen as the preferred tool for an accurate and frequency dependent analysis. Several inductor geometries have been modeled analytically and have been validated with HFSS where in each case there is excellent agreement. The model has also been successfully applied to irregularly shaped power planes that commonly occur in mixed signal circuits.

The present work has established a fabrication process for micro-inductors using technologies available in the Semiconductor and Microsystems Fabrication Laboratory

(SMFL) at RIT. A fabrication process has been developed to integrate inductors, transformers, capacitors, and PMOS (P-type Metal Oxide Semiconductor) transistors. Inductors and transformers have been made from copper and imbedded in a thick PECVD SiO_2 film. The process allows for an optional aluminum ground plane under the copper structures. Capacitors have been formed using the gate oxide as a dielectric and heavily doped silicon and aluminum as the electrodes. PMOS transistors have been implemented to control two varieties of LC tank circuits (parallel and series).

The final contribution of the present work is establishing RF test methods for measuring inductance, and calculating the quality factor (Q). Experimental RF testing is performed using high frequency Cascade Microtech ground-signal-ground (GSG) probes and the 9100 probe station. Data has been captured using an Agilent 8363B network analyzer with a frequency range from 10 MHz to 40 GHz. A calibration procedure has been developed for a full two port measurement and a methodology has been optimized for measuring the impedance [Z] matrix and the scattering [S] matrix. The input impedance is extracted from the [Z] matrix and Q has been calculated. There is excellent agreement between experimental results, numerical results from HFSS, and analytical results from the desegmentation technique.

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1. Introduction

The advancement of integrated circuit (IC) technology has enabled aggressive device scaling leading to the present ability to place hundred of millions of transistors on a single silicon chip. Microprocessors, memory, analog IC's and radio frequency (RF) IC's can all be integrated on a single chip, increasing the functionality of fabricated systems [1]. SoC (system-on-chip) systems combine functions such as digital computing, communications, and other non-CMOS technology. IC RF filters and integrated impedance matching networks are RF circuits that require the incorporation of on chip inductors.

On chip passives such as inductors are of interest in this study. Typically, inductors fabricated on silicon suffer from low self resonant frequencies (SRF), as well as low quality factor (Q factor) [2],[3],[4],[5],[6],[7],[8],[9],[10]. A number of attempts have been made to improve both the SRF and Q factor [2]-[10].

A limitation of fabricating inductors on silicon substrate is the fact that silicon is semi-conductive. This introduces an inherent capacitance that ultimately reduces the SRF. As the inductor moves further form the surface of the substrate, the SRF will increase [8],[11]. It has been proposed that the substrate be removed either by backside [12], or frontside bulk silicon etching [8]. The bulk etching of the silicon substrate removes the associated parasitic capacitance, however, decreases the mechanical stability of the substrate itself. Instead of physically removing the silicon substrate, the anodization of the substrate to form a thick porous silicon film can effectively move the

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conductive substrate surface away from the inductor and reduce the parasitic capacitance presented [13],[14], while preserving a greater degree of mechanical stability.

The losses presented by the resistive silicon substrate help to decrease the Q factor [15]. The reduction of resistive losses to the bulk silicon can be accomplished by inserting a solid ground shield made of a highly conductive material. However, a solid ground shield will produce image currents and a negative mutual inductance [3] thereby lowering overall inductance. The insertion of a patterned ground shield has been shown to increase the quality factor of fabricated inductors while limiting image currents that can lower the inductance [3]. However, the use of any conductive ground shield presents a capacitance which lowers the SRF.

The incorporation of ferromagnetic materials has also been proposed to increase both the inductance and quality factor of on chip inductors [16],[17]. By increasing the permeability of the medium that the inductor is immersed, the inductance can be directly affected. The optimal placement of the magnetic material is also of interest and needs to be addressed for inductors with a ground plane.

It is important to consider both cost of integration as well as performance when choosing an improvement method proposed in [3], [16], [6], [10]. Both theoretical modeling and experimental research is required to determine the value of the gains provided by a modified processing scheme. Reduced footprint area, high Q, high SRF, and high EM isolation are all desirable traits for an inductor, but it can be difficult to maximize all simultaneously.

Inductor modeling using a lumped element approach has been extensively reported [5], and [9] and compared with experimental results. Lumped element models have been applied to standard planar spiral inductors [5],[9], as well as multilayer planar spiral inductors [10]. Layout optimization has also been considered [4], where the width of the coil segments varies for a particular coil. By using analytical models, time intensive electromagnetic (EM) full wave solvers can be avoided. The time required for setup and simulation is a disadvantage of numerical full wave solvers. Time intense EM simulations are not practical to implement in mixed signal design. EM full wave solvers are also difficult to integrate into the design process. Analytical methods can also provide a better design methodology and fundamental understanding than numerical tools.

A fabrication process has been to be developed to experimentally test and verify the results obtained through analytical and numerical techniques. In this study, inductors are fabricated with and with out a ground plane. A frequency dependent analytical model has been developed and extended to address circuit patterns such as rectangular inductors above a solid ground plane or shield. Ferrite powder is available, and attempts are being made to characterize the magnetic properties of this material. Attempts are also being made to electroplate the ferrite material between the fabricated inductors and the aluminum ground plane or the inductors and the silicon surface. Modeling has been performed to predict the impedance response when a magnetic medium is inserted in the cavity or placed above the inductor coil pattern.

2. Present Work and Motivation

2.1 Motivation and Purpose

In order to efficiently and accurately model the impedance of on chip passives, an analytical model has been developed. The model presented in this work is tailored to determine the impedance of microstrip geometries that are realized using standard microelectronic processing techniques. The analytical model can provide impedance data over a range of frequencies and incorporates the effect of higher order modes. The effect of permittivity and permeability are also included to account for a variety of materials.

2.2 Major Contributions

2.2.1 Analytical Modeling

The analytical model of desegmentation has been modified and extended to enable the removal of multiple segments. Previously, one segment removal has been investigated [21],[22]. The extension of the technique to multiple segments provides the ability to analyze a wider variety of irregular circuit patterns. The results that can be obtained by the technique consist of the scattering [S] and impedance [Z] matrices over a range of frequencies. The Z matrix is used to determine properties such as inductance, quality factor, and self-resonant frequency. Irregularly shaped power planes and rectangular coils are among the geometries investigated. The results generated by the modeling technique presented in this work have been compared to the widely used

electromagnetic full wave solver HFSS. The validation of the desegmentation technique presented allows for circumvention of numerical solvers for future analysis.

2.2.2 Physical Realization and Testing of Micro-fabricated Circuits

The verification of the technique presented has been done in part through the physical realization and testing of micro-fabricated inductor geometries. A fabrication process has been fully developed that yielded microstrip circuit patterns alongside MOS transistors, transformers, inductors, and capacitors. A thick ($>10\mu$m) inter-level dielectric (ILD) has been patterned with conventional microlithography and etching to produce vias (10μm), as well as trenches (5μm) for copper interconnect. A copper dual-damascene [18] process has been developed to maximize signal trace conductance thereby limiting the loss contributed by the conductor. The incorporation of magnetic materials using electrophoresis (EP) techniques have been investigated both experimentally and theoretically.

A test procedure has been developed and demonstrated for performing on chip measurements and extracting the impedance characteristics of fabricated passives. A network analyzer is used to extract the frequency dependent impedance of the passives under testing. One port and two port measurements have been collected for inductor patterns and each provided inductance values as well as quality factors.

The design, layout, fabrication, testing, simulation, and analytical modeling of on chip inductors have been performed. All aspects have been achieved using technologies available at the Rochester Institute of Technology (RIT).

3. Inductor Design and Modeling

The modeling of microstrip geometries can be performed using a variety of software such as Ansoft HFSS, Designer, and Maxwell 3D. Analytical methods exist for inductor patterns typically consisting of lumped element models or distributed circuit models.

When an integrated inductor is considered, a number of configurations can be used. The direction of the windings can be used to either enhance or reduce overall inductance.

Figure 1. (a) Meander line setup. (b) Rectangular spiral setup. (c) Cross section of metal trace over metal ground plane. (d) Cross section of metal trace over silicon.

Figure 1 (a) shows a layout for promoting negative mutual coupling while Figure 1(b) shows a layout for enhancing positive mutual coupling [19].

The presence of a conductive ground plane greatly affects the electrical response of the inductor. The removal of any effective conductive ground plane is difficult because the silicon substrate is conductive and presents a capacitance associated with the inductor. A well-defined ground plane can be achieved by heavily-doping the silicon or patterning a metallic layer under the dielectric as shown in Figure 1(c). If a ground plane is desired, it should be constructed of metal for maximum conductivity to minimize

conductive losses. Microstrip geometries are of interest in this study and have been implemented using conventional microelectronic fabrication techniques.

3.1 Analytical Modeling

The primary focus for the analytical modeling in this study involves microstrip geometries where a signal trace is routed above a ground plane. For simple rectangular and circular shapes, a Green's function can be directly found. For irregular shapes where a Green's function is not available, the technique of segmentation or desegmentation can be applied. Segmentation and desegmentation provide a means of determining the frequency dependent impedance response for irregularly shaped patterns. To apply segmentation or desegmentation to irregularly shaped patterns, the irregular pattern must consist of the addition or subtraction (segmentation or desegmentation, respectively) of regular shapes for which a Green's function is available.

3.1.1 Segmentation and Desegmentation

The segmentation and desegmentation methods investigated here use the cavity model to determine the impedance parameters between defined ports on a geometry for which a Green's function exists. Segmentation provides the resulting impedance characteristics for an irregularly shaped structure by adding the effects of regularly shaped geometries [20].

Figure 2. (a) Irregular shape for which segmentation can be applied. (b) Regularly shaped segments that constitute irregular shape in Figure 2a.

Desegmentation can also be applied to the irregular geometry seen in Figure 2(a) as shown in Figure 3.

Figure 3. (a) Irregular shape for which desegmentation can be applied. (b) γ segment composed of α and β segments. (c) β segments being removed to yield irregular shape Figure 2a.

When using the desegmentation method, the Green's function is evaluated for the γ segment in Figure 3(b) and the impedance response of the β segments is removed. The β segments must be regular patterns for which Green's functions are available. The application and extension of the desegmentation technique is the focus of this work. The results generated by the desegmentation technique provide an impedance matrix or scattering matrix capable of describing inductor patterns over a wide frequency range.

Accurate inductor modeling is of great interest to analog circuit designers. Physical models typically include lumped elements [5] to combine the parasitics present from on chip fabrication with the series inductance of the designed inductor. Series inductance (L_S), inner turn capacitance (C_S), series resistance (R_S), oxide capacitance (C_{ox}), silicon substrate capacitance (C_{Si}), and silicon substrate resistance (R_{Si}) are considered in the lumped element model shown in Figure 4(a).

Figure 4. (a) Lumped element model of on chip spiral inductor. (b) Z matrix representation.

The equivalent circuit for Figure 4(a) could be represented as a Z or S matrix. Either form can provide accurate characterization of integrated inductors for use in analog circuit design. The level to which coupling parasitics are included determines the overall accuracy and validity of the lumped element model. The technique used in this study

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allows for the direct calculation of impedance parameters from a Green's function for rectangular microstrip cavities.

3.2 Mathematical Formulation

Desegmentation has been previously developed to address the removal of a single segment [21] - [22]. To apply the desegmentation method, a technique to determine impedance must be selected. In this study, rectangular geometries are considered and impedance parameters are found using Green's functions for a rectangular cavity. For thin dielectrics (dielectric thickness, $d \ll \lambda$), the analytical model for the cross section in Figure 1(c) is based on the application of the cavity model. The cavity model assumes perfect electric walls at the metal dielectric interfaces and perfect magnetic sidewalls on the vertical sides, which are perpendicular to the perfect electric conductors. Ports can be defined arbitrarily within the cavity where current is excited perpendicular to the surface of the conductor. The cavity model leads to the electromagnetic solution as a Green's function. The cavity model provides impedance results for regular patterns and the segmentation or desegmentation techniques are used to extend the closed form solution for irregular patterns. The desegmentation technique is considered here and extended to allow for multiple segment removal.

3.2.1 Green's Function for Rectangular Geometries

Figure 5(a) shows a microstrip cavity with perfect electric conductors (PEC) on the top and bottom, as well as perfect magnetic conductors (PMC) on the vertical sidewalls. The dielectric thickness is d, a is the x dimension length, b is the y dimension

length, W_{xi} is the x dimension width of the ith port, W_{yi} is the y dimension width of the ith port, W_{xj} is the x dimension width of the jth port, W_{yj} is the y dimension width of the jth port, μ_r is the relative permeability, ε_r is the relative permittivity, and $\tan(\delta)$ is the dielectric loss tangent. Figure 5(b) shows the port placement where x_i is the center x position of port i, x_j is the center x position of port j, y_i is the center y position of port i, and y_j is the center y position of port j.

(a)   (b)

Figure 5. (a) Microstrip cavity showing port definitions. (b) Plan view of microstrip cavity showing port definitions.

The impedance for a rectangular microstrip segment is expressed using Green's function in (1) [23].

$$Z_{ij} = \frac{1}{W_{xj}W_{xi}W_{yj}W_{yi}} \int_{W_{xi}} \int_{W_{xj}} \int_{W_{yi}} \int_{W_{yj}} G(x,y \mid x_o, y_o) dx dx_o dy dy_o \tag{1}$$

where W_i and W_j are the widths of ports i and j respectively and $G(x,y|x_o,y_o)$ is a Green's function. To describe the electromagnetic condition in the cavity of Figure 5(a), the Helmholtz equation (2) is used.

$$\nabla^2 E_z + k^2 E_z = j\omega\mu I_z \tag{2}$$

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E_z is z component of the electric field, ω is the angular frequency equal to $2\pi f$, μ is the

permeability ($\mu_r\mu_o$), k is the wave number, and I_z is the current directed in the z direction.

For thin cavities (d<<λ) the electric field is found by dividing the voltage by the

dielectric thickness as shown in (3).

$$E_z = \frac{V_z}{d} \tag{3}$$

The voltage variation on the microstrip cavity can be determined by defining the voltage

response as a Green's function due to a current excitation δ as seen in (4).

$$\left(\nabla^2 + k^2\right) G(x, y; x', y') = j\omega\mu d\,\delta(x-x')\delta(y-y') \tag{4}$$

The Green's function can be expressed in series form (5),

$$G(x, y; x', y') = \sum \frac{j\omega\mu d\,\psi_{mn}(x, y)\psi_{mn}(x', y')}{\left(k_{mn}^2 - k^2\right)} \tag{5}$$

where Ψ_{mn} and k_{mn} are the eigenfunctions and eigenvalues respectively.

By applying the electric and magnetic wall boundary conditions described in

Figure 5(a), the Green's function is shown in (6) [23].

$$G(x_i, y_i; x_j, y_j) = \frac{j\omega\mu d}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_x^2 + k_y^2 - k^2} \times \\ \cos(k_x x_i)\cos(k_x x_j)\cos(k_y y_i)\cos(k_y y_j) \tag{6}$$

where $k_x = \dfrac{m\pi}{a}$, $k_y = \dfrac{n\pi}{b}$, $\varepsilon_m = \begin{cases} 1 & m=0 \\ \sqrt{2} & m\neq 0 \end{cases}$, and $\varepsilon_n = \begin{cases} 1 & n=0 \\ \sqrt{2} & n\neq 0 \end{cases}$.

The wave number is,

$$k = k' - jk'' = \varpi\sqrt{\mu\varepsilon} - j\varpi\sqrt{\mu\varepsilon}\frac{\tan(\delta) + \dfrac{r}{d}}{2} \tag{7}$$

where,

$$r = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{8}$$

By applying k'', the loss contributed from the finite metal conductivity (σ) and dielectric loss ($\tan(\delta)$) can be accounted for. Using (1) and (6), the impedance between ports can be found and is expressed in (9) [23].

$$\begin{aligned}
Z(x_i, y_i; x_j, y_j) = \frac{j\omega\mu d}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{\varepsilon_m^2 \varepsilon_n^2}{k_x^2 + k_y^2 - k^2} \times \\
\cos(k_x x_i)\cos(k_x x_j)\cos(k_y y_i)\cos(k_y y_j) \times \\
\operatorname{sinc}\left(\frac{k_x W_{xi}}{2}\right)\operatorname{sinc}\left(\frac{k_x W_{xj}}{2}\right)\operatorname{sinc}\left(\frac{k_y W_{yi}}{2}\right)\operatorname{sinc}\left(\frac{k_y W_{yj}}{2}\right)
\end{aligned} \tag{9}$$

(9) can be applied to rectangular cavities and is used in combination with the desegmentation method to provide solutions to circuit patterns consisting of regular shapes.

3.2.2 Single Segment Removal

The desegmentation method has been proposed and developed in [21]-[22]. In contrast to segmentation, desegmentation subtracts segments for which (9) can be applied from other regularly shaped segments. To illustrate the capability of the desegmentation technique, the ring pattern in Figure 6 is considered.

Figure 6. (a) Rectangular ring pattern. (b) Application of segmentation. (c) Application of desegmentation.

It can be seen that when segmentation is applied to the pattern in Figure 6(a), the addition of S_1, S_2, S_3 and S_4 will result in the desired pattern. If desegmentation is applied, the effect of D_2 is subtracted from D_1. If segmentation is used, (9) must be calculated for four segments, whereas desegmentation requires (9) to be applied on only two segments.

The development of desegmentation stems from the segmentation method for which Z matrices are used [20]. If a Green's function were available for the α segment in Figure 7(a), segmentation in could be applied as shown in Figure 7.

Figure 7. Illustration of segmentation when $Z_{pp.}^{\alpha}$ can not be found. (a) α segment. (b) β segment. (c) γ segment.

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P is the number of externally connected ports ($p_1,p_2...p_P$), while C ($c_1,c_2,...c_C$), and D ($d_1,d_2,...d_D$) are the number of interconnected ports. C must equal D, and the necessary number of ports for convergence is dependent on frequency. Using the segmentation method outlined in [20], impedance matrices can be used to determine $Z_{pp}{}^{\gamma}$ as shown in [21].

$$Z_{pp}{}^{\gamma} = Z_{pp}{}^{\alpha} - Z_{pc}{}^{\alpha}\left[Z_{cc}{}^{\alpha} + Z_{dd}{}^{\beta}\right]^{-1} Z_{cp}{}^{\alpha} \qquad (10)$$

$Z_{cc}{}^{\alpha}$, $Z_{pc}{}^{\alpha}$, and $Z_{cp}{}^{\alpha}$ can not be found directly, however, if a Green's function is known for the γ and β segments, the α matrices can be found in terms of the impedance matrices for the γ and β segments. If D is set equal to C and renamed to Q, the desegmentation formula can be rearranged as (11) [21].

$$Z_{pp}{}^{\alpha} = Z_{pp}{}^{\gamma} - Z_{pq}{}^{\gamma}\left[Z_{qq}{}^{\gamma} - Z_{qq}{}^{\beta}\right]^{-1} Z_{qp}{}^{\gamma} \qquad (11)$$

The Q and P ports are placed as shown in Figure 8.

Figure 8. Desegmentation method applied as expressed in (11).

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As with the segmentation method, P ports are externally connected ports. Q ports, however, serve as internally connected ports on the γ segment and externally connected ports on the β segment. The number of Q ports on the perimeter of the β segment can be increased thereby decreasing the width of these ports. This is normally done until the solution converges to an acceptable level.

$Z_{pp}{}^{\alpha}$ is the impedance between the p ports on the irregularly shaped α segment. $Z_{pp}{}^{\gamma}$ is the impedance between the p ports on the regularly shaped γ segment. $Z_{pq}{}^{\gamma}$ is the impedance between the p and q ports on the regularly shaped γ segment. $Z_{qp}{}^{\gamma}$ is the impedance between the q and p ports on the regularly shaped γ segment. $Z_{qq}{}^{\gamma}$ is the impedance between the q ports on the regularly shaped γ segment. $Z_{qq}{}^{\beta}$ is the impedance between the q ports on the regularly shaped β segment. Each port is defined in terms of center x position, center y position, x width, and y width. In order to apply (9) the port placement must be defined along with the dimensions of the rectangles being analyzed (x_i, x_j, W_{xi}, W_{yi}, W_{xj}, W_{yj}, a, b).

Figure 9. (a) Port definition for $Z_{pp}{}^{\gamma}$. (b) Port definition for $Z_{pq}{}^{\gamma}$. (c) Port definition for $Z_{qq}{}^{\gamma}$. (d) Port definition for $Z_{qq}{}^{\beta}$.

Calculating $Z_{pp}{}^{\gamma}$ shown in Figure 9(a):

For element Z_{11} in $Z_{pp}{}^{\gamma}$, (9) is applied where:

$x_i = x_{i,j}$, $x_j = x_{i,j}$, $W_{xi} = W_{xj} = W_{xi,xj}$, $W_{yi} = W_{yj} = W_{yi,yj}$, $a = A$, $b = B$ as shown in Figure 9(a).

Calculating $Z_{pq}{}^{\gamma}$ shown in Figure 9(b):

For element Z_{11} in $Z_{pq}{}^{\gamma}$, $x_i = x_i$, $x_j = x_{1j}$, $W_{xi} = W_{xi}$, $W_{yi} = W_{yj}$, $W_{xj} = 0$ $W_{yj} = b$, $a = A$, $b = B$ as shown in Figure 9(b).

For element Z_{12} in $Z_{pq}{}^{\gamma}$, $x_i = x_i$, $x_j = x_{2j}$, $W_{xi} = W_{xi}$, $W_{yi} = W_{yj}$, $W_{xj} = a$, $W_{yj} = 0$, $a = A$, $b = B$ as shown in Figure 9(b). Similarly, Z_{13} and Z_{14} for $Z_{pq}{}^{\gamma}$ can be found.

$Z_{qp}{}^{\gamma}$ can be determined a similar manner or a transpose of $Z_{pq}{}^{\gamma}$ can be done to reduce computing time.

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Calculating Z_{qq}^{γ} shown in Figure 9(c):

For element Z_{11} for Z_{qq}^{γ}, $x_i=x_{1i}$, $x_j=x_{1i}$, $W_{xi}=0$, $W_{yi}=b$, $W_{xj}=0$ $W_{yj}=b$, $a=A$, $b=B$ as shown in Figure 9(c).

For element Z_{12} for Z_{qq}^{γ}, $x_i=x_{1i}$, $x_j=x_{2j}$, $W_{xi}=0$, $W_{yi}=b$, $W_{xj}=a$, $W_{yj}=0$, $a=A$, $b=B$ as shown in Figure 9(c). Similarly, Z_{13}, Z_{14}, $Z_{21} \rightarrow Z_{24}$, $Z_{31} \rightarrow Z_{34}$, $Z_{41} \rightarrow Z_{44}$ for Z_{qq}^{γ} can be found.

Calculating Z_{qq}^{β} shown in Figure 9(d):

For element Z_{11} for Z_{qq}^{β}, $x_i=x_{1i}$, $x_j=x_{1i}$, $W_{xi}=0$, $W_{yi}=b$, $W_{xj}=0$ $W_{yj}=b$, $a=A$, $b=B$ as shown in Figure 9(c).

For element Z_{12} for Z_{qq}^{β}, $x_i=x_{1i}$, $x_j=x_{2j}$, $W_{xi}=0$, $W_{yi}=b$, $W_{xj}=a$, $W_{yj}=0$, $a=a$, $b=b$ as shown in Figure 9(d). Similarly, Z_{13}, Z_{14}, $Z_{21} \rightarrow Z_{24}$, $Z_{31} \rightarrow Z_{34}$, $Z_{41} \rightarrow Z_{44}$ for Z_{qq}^{β} can be found.

Once Z_{pp}^{γ}, Z_{pq}^{γ}, Z_{qp}^{γ}, Z_{qq}^{γ} and Z_{qq}^{β} are known, (11) can be used to determine Z_{pp}^{α}, or the impedance matrix for the irregular shape shown in Figure 8 (α pattern). It is also possible to add additional q ports around the perimeter of the segment to be removed. Doubling the number of q ports reduces the width of the q ports by 50%. By reducing the length of the q ports around the perimeter of the β segment, greater accuracy can be obtained.

3.2.3 Convergence Analysis for Single Segment Removal

The convergence behavior of the desegmentation technique for single segment removal described in 3.2.2 is presented to illustrate the steps necessary to obtain a

solution of desired accuracy. The presence of the double summations in (9) allows higher order modes to be discarded when they are insignificant for a particular set of dimensions. The number of m and n modes necessary for convergence is dependent upon the frequency on interest. For relatively low frequencies, fewer eigenmodes are required than for relatively higher frequencies. Consequently, objects with longer physical lengths require a greater number of modes to be summed. The convergence study presented in 3.2.3 investigates the convergence characteristics for the symmetric rectangular ring pattern shown in Figure 10(a). By symmetry, eigenmodes m and n will be set to have equal values.

The procedure for determining convergence involves three parameters: m eigenmodes in the x direction, n eigenmodes in the y direction, and q port width. S_{11} [dB] vs. frequency for a single external p port has been calculated, and the first two resonant frequencies (minimum S_{11} [dB]) are determined. As m and n are increased, the change in the resonant frequencies (Δf_r) is noted. After achieving the desired convergence through the increase in eigenmodes, the width of the q ports is decreased. The resonant frequencies are again inspected as the port width is reduced. The numerical example in Figure 10(b) is considered. The assigned dimensions and material parameters are shown in Figure 10(b).

<table>
<tr><td>A= 2 cm</td></tr>
<tr><td>B= 2 cm</td></tr>
<tr><td>a= 1 cm</td></tr>
<tr><td>b= 1 cm</td></tr>
<tr><td>d= 5 μm</td></tr>
<tr><td>ε_r= 4.00</td></tr>
<tr><td>μ_r=1.00</td></tr>
<tr><td>p_1=[0.15 cm, 1 cm]</td></tr>
<tr><td>LossTan=0.01</td></tr>
</table>

(a)   (b)

Figure 10. (a) Pattern tested for convergence. (b) Dimensions and material parameters.

Using the desegmentation method, convergence data has been collected using single segment removal. The change in resonant frequency, Δf_r, is found by calculating the shift in the resonant frequency when additional modes are included in the double summation of (9). Each data point in Figure 12 contains two additional m and n eigenmodes relative to the previous data point. 4 q ports are evenly distributed around the inner β segment for the eigenmode convergence test.

Figure 11. Eigenmode convergence for S_{11} for ring pattern.

Figure 12. (a) Change in first two resonant frequencies (f_{r1}, f_{r2}) vs. n and m eigenmodes.

After m=n=34 for and 16 q ports are placed, the first two resonant frequencies are,

$$f_{r1} = 2.76 \text{ GHz}$$
$$f_{r2} = 5.84 \text{ GHz}$$

Once the change in frequency is less than equal to 10MHz (<1%), the process is halted and the solution is converged to the desired degree.

Next, m and n are set to 34 and the number of q ports is increased, thereby reducing the width of the q ports.

Figure 13. First resonant frequency vs. q port width (m=n=34).

Figure 14. Second resonant frequency vs. q port width (m=n=34).

As the port width is decreased, the converged resonant frequency is approached. The

resonant frequency is obtained by noting where the change in resonant frequency fell

below the specified tolerance, in this case 10MHz (<1% of f_r). The first resonant

frequency converged with a port width of 5 mm while the second resonant frequency

converged with a port width of 2 mm. Higher frequencies require a reduced port width. The final resonant frequencies are:

$$f_{r1} = 2.69 \text{ GHz}$$
$$f_{r2} = 5.81 \text{ GHz}$$

3.2.4 Two Segment Removal

In order to remove two pieces using the desegmentation method, it is proposed that additional fictitious p ports be placed around the periphery of the additional segment to be removed. For comparison, the rectangular ring in Figure 10(b) is analyzed by dividing the center segment into two segments.

(a)   (b)   (c)   (d)

A= 2 cm
B= 2 cm
a= 1 cm
b= 1 cm
d= 5 μm
ε_r= 4.00
μ_r=1.00
p_1=[0.15 cm, 1 cm]
LossTan=0.01

(e)   (f)

Figure 15. (a) Initial γ segment (γ_1). (b) β_1 segment. (c) α_1 or γ_2 segment. (d) β_2 segment. (e) Final α segment α_2. (f) Physical parameters of rectangular ring under analysis.

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The calculation of the first α circuit in Figure 15 is done in the similar manor described in 3.2.2. For the removal of a second piece, additional fictitious p ports (p$_2$-p$_5$) are placed as shown in Figure 15(a). The fictitious p ports are defined in the same way as q ports. After the removal of the first β segment, the matrix that describes Figure 15(c) comes directly from (11). For four q ports per β segment, (12) is calculated. The α1 segment contains only p-ports. The γ2 segment redefines the p ports around the β2 segment to q ports (p$_2$-p$_5$ to q$_5$-q$_8$).

$$
Z_{pp}{}^{\alpha 1} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} & Z_{15} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} & Z_{25} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} & Z_{35} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} & Z_{45} \\ Z_{51} & Z_{52} & Z_{53} & Z_{54} & Z_{55} \end{bmatrix}
\tag{12}
$$

The submatrices of (12) make up $Z_{pp}{}^{\gamma 2}, Z_{pq}{}^{\gamma 2}, Z_{qp}{}^{\gamma 2},$ and $Z_{qq}{}^{\gamma 2}$ as shown in (13).

$$
Z_{pp}{}^{\alpha 1} = \begin{bmatrix} Z_{pp}{}^{\gamma 2} & \leftarrow Z_{pq}{}^{\gamma 2} \rightarrow \\ \begin{matrix}\uparrow \\ Z_{qp}{}^{\gamma 2} \\ \downarrow\end{matrix} & \begin{matrix}\uparrow \\ \leftarrow Z_{qq}{}^{\gamma 2} \rightarrow \\ \downarrow\end{matrix} \end{bmatrix}
\tag{13}
$$

From this point, $Z_{pp}{}^{\gamma 2}, Z_{pq}{}^{\gamma 2}, Z_{qp}{}^{\gamma 2},$ and $Z_{qq}{}^{\gamma 2}$ are known and $Z_{qq}{}^{\beta 2}$ is found directly by using (9). (11) is then applied again to determine $Z_{pp}{}^{\alpha 2}$ in Figure 15(e).

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3.2.5 Convergence Analysis for Double Segment Removal

For the parameters shown in Figure 15(f) convergence can be collected. First, the number of eigenmodes is increased until the change in the resonant frequency fell to an acceptable level (<10 MHz). Next, the number of q ports is increased until the solution converges. Since the number of q ports are evenly distributed on each side around the β segment, the q port width is taken to be the maximum q port width in each case.

Figure 16. Eigenmode convergence for two segment removal for the first two resonant frequencies.

Figure 16 shows how the first two resonant frequencies change as an increasing number of eigenmodes are summed. When m=n=34 and the q port width is equal to 1 cm, the first two resonant frequencies have been found as,

$$f_{r1} = 2.73 \text{ GHz}$$
$$f_{r2} = 5.86 \text{ GHz}$$

Next, m and n are held constant at 34 as the q port width is decreased. The resonant

frequency is found as a function of decreasing port width.

Figure 17. Convergence for first resonant frequency when two segments are removed (m=n=34).

Figure 18. Convergence for second resonant frequency when two segments are removed (m=n=34).

Figure 17 and Figure 18 show the response in the first and second resonant frequencies

respectively, vs. decreasing q port width for two segment removal. After the reduction of

the port width to 1.67 mm shown in Figure 17 and Figure 18, the resonant frequencies are found as:

$$f_{r1} = 2.69 \text{ GHz}$$
$$f_{r2} = 5.84 \text{ GHz}$$

Increasing m and n to 80 when the q port width is set to 1.67 mm eliminated the 0.03 GHz difference between the single and double segment removal for the second resonant frequency. The final solutions found using double segment removal are:

$$f_{r1} = 2.69 \text{ GHz}$$
$$f_{r2} = 5.81 \text{ GHz}$$

It is evident that multiple segment removal exhibits slightly different convergence characteristics than single segment removal. In two segment removal, as the number of q ports is increased, additional eigenmodes are necessary for convergence. The single segment removal and the double segment removal each yielded a fr_1=2.69 GHz and fr_2=5.81 GHz, where the values are found to the nearest 10 MHz. The solution for one segment removal converged with m=n=34 and a q port width of 1.67 mm, while two segment removal required m=n=100 and a q port width of 1.67 mm for similar convergence.

3.2.6 N Segment Removal

The process in 3.2.4 can be extended to handle the removal of N number of segments. After one segment is removed, (14) is calculated using (11).

$$
Z_{pp}^{\alpha 1} =
\begin{bmatrix}
\overbrace{\begin{matrix} Z_{11} & Z_{12} & \cdots \\ Z_{21} & Z_{22} & \cdots \\ \vdots & \vdots & \ddots \end{matrix}}^{Z_{pp}^{\gamma 2}}
& \overbrace{\begin{matrix} Z_{1(n-k)} & \cdots & Z_{1n} \\ Z_{2(n-k)} & \cdots & Z_{2n} \\ \vdots & \vdots & \vdots \end{matrix}}^{Z_{pq}^{\gamma 2}} \\[4pt]
\underbrace{\begin{matrix} Z_{(n-k)1} & Z_{(n-k)2} & \cdots \\ \vdots & \vdots & \cdots \\ Z_{n1} & Z_{n2} & \cdots \end{matrix}}_{Z_{qp}^{\gamma 2}}
& \underbrace{\begin{matrix} Z_{(n-k)(n-k)} & \cdots & Z_{(n-k)n} \\ \vdots & \ddots & \vdots \\ Z_{n(n-k)} & \cdots & Z_{nn} \end{matrix}}_{Z_{qq}^{\gamma 2}}
\end{bmatrix}
\qquad (14)
$$

where n is the total number of p ports and the k is the number of Q ports per segment -1. Each time a segment is removed and an intermediate α matrix is found, the p-ports on the subsequent segment to be removed are redefined to q ports, which forms the subsequent γ segments (α is converted to γ). Z_{qq}^{β} for the subsequent segment can be found directly and (11) can be applied again. This process is repeated for all segments that are to be removed until the final pattern is achieved. (15) is used for extracting the intermediate Z^{γ} parameters, where x is the segment number being removed, and $Z_{pp}^{\gamma}, Z_{pq}^{\gamma}, Z_{qp}^{\gamma}$ and Z_{qq}^{γ} are the sub matrices from (14).

$$
Z_{pp}^{\alpha(x)} =
\begin{bmatrix}
Z_{pp}^{\gamma(x+1)} & Z_{pq}^{\gamma(x+1)} \\
Z_{qp}^{\gamma(x+1)} & Z_{qq}^{\gamma(x+1)}
\end{bmatrix}
\qquad (15)
$$

The convergence analysis can be carried out in a similar manner as done in 3.2.5.

4. Numerical Modeling

Numerical EM full wave solvers typically require more calculations than simplified analytical models but have greater flexibility for solving a larger variety of problems. Numerical modeling tools also assist in the validation of analytical modeling technique by providing a standard for comparison.

4.1 Available Numerical Modeling Tools

Ansoft HFSS and Maxwell 3D are two modeling tools that provide the electromagnetic response to a given excitation. High frequency structure simulator (HFSS) accounts for high frequency effects that become significant as the wavelength of the excitation approaches the physical dimensions of the circuit under investigation.

4.2 HFSS

HFSS allows for the geometric definition and analysis of structures in a 3D environment. In addition, layouts from other software packages can be directly imported for electromagnetic analysis.

4.2.1 Structure Definition in HFSS

The pattern shown in Figure 19 is investigated. For analytical comparison, perfect electric walls are defined for the signal trace and the ground plane in HFSS. The dielectric is given a permittivity, permeability, and a loss tangent. The loss tangent is provided to yield finite impedances at resonant frequencies.

Figure 19. (a) Plan view of a rectangular ring. (b) Cross section of rectangular ring.

When the pattern in Figure 19 is defined in HFSS, 2-dimensional rectangles are used to define the top ring pattern and a perfect electric conductor boundary condition is assigned. A 3-dimensional box is defined with a thickness of d and is extended beyond the ring pattern. The dielectric characteristics are provided to this box which is positioned under the ring pattern. A perfect electric conductor boundary is assigned to the bottom face of the dielectric box to provide a ground plane. A 3-dimensional box is placed above the surface of the dielectric and assigned the electrical properties of vacuum ($\mu_r=1$, $\varepsilon_r=1$, lossless). Radiation boundaries are assigned to the 5 outer perimeter faces of the vacuum box.

(a) (b) (c)

Figure 20. (a) Perfect electric boundary on ring. (b) Perfect electric boundary on bottom face of dielectric. (c) Radiation boundaries on 5 outer faces of vacuum box.

The thickness of the metal used for the ground plane and ring pattern are not accounted for in the cavity model. When perfect electric boundaries are specified in HFSS, the thickness and loss presented by the metallic layers are neglected.

4.2.2 Port Definition in HFSS

To define an excitation within the cavity, a lumped port is used. The lumped port can be defined anywhere within the structure, which provides flexibility in port placement. First, a placement rectangle is drawn from the signal trace to the ground plane where an excitation port is desired. Next, a lumped port is placed in the center of the placement rectangle by drawing an integration line from the signal trace to the ground plane in the center of the placement rectangle. The impedance of the port can be set in order to match any test equipment being used. 50 Ω is used for all lumped ports for the calculation of the S parameters in this study.

Figure 21. (a) Angle view of rectangular ring. (b) Zoom of port placement.

The 50 Ω lumped port can be seen in Figure 21(b). Figure 21(b) shows a zoom view of the picture in Figure 21(a).

4.2.3 Analysis Setup in HFSS

All simulations are performed using the driven modal solution type. The analysis setup is set to have a solution frequency at least ¾ of the highest frequency of interest. The convergence parameter for maximum ΔS per pass is adjusted for each simulation to yield accurate results. When solutions are collected over a range of frequencies, a discrete sweep is done to maintain accuracy.

5. Comparison of Analytical and Numerical Techniques

The analytical technique of desegmentation has been programmed in MATLAB to provide results and comparison to simulated HFSS results.

5.1 Rectangular Ring

The ring pattern discussed in 3.2.4 is analyzed using HFSS and desegmentation. The boundaries are set up in the same manner shown in Figure 20.

A= 2 cm
B= 2 cm
a= 1 cm
b= 1 cm
d = 5 μm
ε_r= 4.00
μ_r=1.00
p_1=[0.15 cm, 1 cm]
LossTan=0.01

(a)

(b)

S_{11} Parameters for Ring Pattern

(c)

(d)

Figure 22. (a) Planar view of ring pattern. (b) Parameters used for analysis. (c) HFSS capture of ring pattern. (d) S_{11} for ring pattern.

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Figure 22 shows the characteristics of the simulated structure. The parameters for the convergence of the analytical model include m=n=35 and a q port width equal to 1.67 mm (24 q ports). Single segment removal has been applied.

For HFSS, perfect electric conductor walls are defined on the signal trace and on the ground plane. A port placement rectangle is placed at (0.15cm, 1.0cm) with a width of 0 μm in the y direction, 1 μm in the x direction, and 5 μm (thickness of dielectric) in the z direction. A lumped port is defined by placing an integration line down the center of the placement rectangle. The solution frequency is equal to 7 GHz, the max $\Delta S<.0002$, and a discrete sweep has been done from 1 GHz to 7 GHz in steps of 0.01 GHz .

S_{11} Results (Figure 22)	HFSS	Desegmentation	% Difference
f_{r1}	2.69 GHz	2.69 GHz	0.0%
f_{r2}	5.84 GHz	5.81 GHz	0.5%

Figure 23. Table of resulting resonant frequencies for pattern in Figure 22.

5.2 L- Shaped Plane

An L shaped pattern has been analyzed and the resonant frequencies are found using HFSS and the desegmentation technique. Single segment removal is applied to the L-shaped pattern for analytical calculations. The parameters for the convergence of the desegmentation model included m=n=20 and a q port width equal to 3.33 mm (12 ports).

For HFSS, perfect electric walls are defined on the signal trace and on the ground plane. A port placement rectangle is placed at (0.15cm, 1.0cm) with a width of 0 μm in the y direction, 1 μm in the x direction, and 5 μm (thickness of dielectric) in the z

direction. A lumped port is defined by placing an integration line down the center of the placement rectangle. The solution frequency is equal to 4.40 GHz, the max $\Delta S < 0.004$, and a discrete sweep has been done from 1 GHz to 6 GHz in steps of 0.01 GHz .

(a)

A= 2 cm
B= 2 cm
a= 1 cm
b= 1 cm
d = 5 μm
ε_r= 4.00
μ_r=1.00
p_1=[0.15 cm, 1 cm]
LossTan=0.01

(b)

(c)

(d)

Figure 24. (a) Planar view of L-shaped pattern (b) Parameters used for analysis (c) HFSS capture of L shaped pattern (d) S_{11} for L-shaped pattern.

S_{11} Results (Figure 24)	HFSS	Desegmentation	% Difference
f_{r1}	2.89 GHz	2.905 GHz	0.5%
f_{r2}	4.44 GHz	4.49 GHz	1.1%

Figure 25. Table of resulting resonant frequencies for pattern in Figure 24.

5.3 One Turn Inductor

A one turn inductor is analyzed by using two segment desegmentation and HFSS.

The boundaries are again setup as described in Figure 20.

(a)

A= 2 cm
B= 2 cm
a_1= 1 cm
b_1= 1 cm
a_2= 2 mm
b_2=5 mm
$d_{dielectric}$ = 0.7874 mm
ε_r= 2.33
μ_r=1.00
p_1=[0.25 cm, 0 cm]
p_2=[0.70 cm, 2.5 mm]
LossTan=0.01

(b)

(c)

(d)

Figure 26. (a) Plan view of a one turn inductor pattern. (b) Parameters used for analysis. (c) HFSS capture of one turn inductor structure pattern. (d) Inductance for one turn inductor.

Reactance of Z_{11} for One Turn Inductor

Figure 27. (a) Segmentation vs. desegmentation vs. measured data.

The desegmentation technique is applied to the one turn inductor shown in Figure 26 by removing two segments. The eignenmodes necessary for convergence are m=n=250. The maximum q port width used is 1.67 mm (24 q ports per segment). The analytical calculations are performed from 0.1 GHz to 5 GHz in steps of 50MHz. Figure 27 compares the segmentation technique from [24], measured data from [24], and modeled results from the desegmentation technique.

For HFSS, perfect electric conductor walls are defined on the signal trace and on the ground plane. Port placement rectangles are placed at (2.5 mm, 0.0 cm) and (7.0 mm, 2.5 mm) with a width of 0 µm in the y direction, 1 µm in the x direction, and 5 µm (thickness of dielectric) in the z direction. A lumped port is defined by placing an integration line down the center of each placement rectangle. The solution frequency is

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equal to 4.13 GHz, max ΔS<.004, and a discrete sweep is done from 0.1 GHz to 5 GHz in steps of 50 MHz . Only the inductive regions are shown in Figure 26(d). The inductance for the one turn inductor in Figure 26 has been calculated from the impedance matrix by applying equation (16) [26].

$$L = \frac{im\left(Z_{11} - \frac{Z_{12}^2}{Z_{22}}\right)}{2\pi f} \tag{16}$$

Data from (Figure 26)	HFSS	Desegmentation	% Difference
L [nH] (100MHz)	8.59 nH	10.14 nH	18%
SRF₁	0.84 GHz	0.95 GHz	13%
SRF₂	2.52 GHz	2.58 GHz	2.4%
SRF₃	4.24 GHz	4.18 GHz	1.4%

Figure 28. Table of resulting inductance at 100MHz and SRF from Figure 26.

6. Ferrite Filled Inductors

For on chip inductors, the incorporation of a material with a μ>1 allows for the enhancement of inductance without an increase in the footprint area. Ferrites can be used to enhance the permeability of the region around the inductor, and modify the electrical response over a range of frequencies. This modification can cause both desirable and undesirable effects. The modeling performed in this study is capable of addressing microstrip configurations where the inductor is located above a ground plane. The impedance of a microstrip cavity is shown in (9). The impedance is shown to be directly proportional to μ. In addition, the frequency response of the impedance is divided by k^2, which is equal to $(2\pi f)^2 \mu \varepsilon$. With an increase in μ_r, the resonant frequencies will shift down. If an on chip inductor is immersed in a material with a μ_r>1, the low frequency inductance will be increased however, the self resonant frequency will be decreased.

6.1 Predicted Effect of Magnetic Material Filling Using HFSS

The inductor shown in Figure 26 (a) is modeled using HFSS and desegmentation. The inductance looking through the inductor is modeled and compared for the two different configurations shown in Figure 29.

Figure 29. (a) Magnetic material positioned above one turn inductor. (b) Magnetic material positioned between the inductor pattern and the ground plane.

The dimensions of the one turn inductor are listed in Figure 26 (b). The permeability of the medium above and below the inductor pattern is modified and the resulting inductances are calculated. For HFSS, a solution frequency of 4 GHz is used, with an ultimate max $\Delta S < 0.03$. A frequency sweep is performed from 100 MHz to 5 GHz in discrete steps of 50 MHz.

Figure 30. HFSS results for magnetic material placed above one turn inductor.

Figure 31. HFSS results for magnetic material placed between one turn inductor and ground plane.

Desegmentation has been applied to analytically predict the effect of magnetic material filling in the cavity. Desegmentation uses m=n=250 and a maximum q port width of 1.67 mm (24 q ports per segment).

Figure 32. Desegmentation results for a magnetic material placed between one turn inductor and ground plane.

Results from Figure 30 and Figure 31	$\mu_r=1$	$\mu_r=2$	% change
L [nH] (100 MHz, μ_r above inductor)	8.59 nH	9.4 nH	9.4%
L [nH] (100 MHz, μ_r inside cavity)	8.59 nH	15.10 nH	75.8%
SRF_1 (μ_r above inductor)	0.84 GHz	0.84 GHz	0.00%
SRF_1 (μ_r inside cavity)	0.84 GHz	0.61 GHz	28.2%

Figure 33. HFSS Results for magnetic material enhancement.

Results from Figure 32	$\mu_r=1$	$\mu_r=2$	% change
L [nH] (100 MHz, μ_r inside cavity)	10.14 nH	20.45 nH	102 %
SRF_1 (μ_r inside cavity)	0.95 GHz	0.61 GHz	35.8 %

Figure 34. Desegmentation results for magnetic material enhancement.

From the HFSS results it is clear that placing the magnetic material between the inductor and the ground plane produces the greatest increase in inductance.

7. Physical Realization of Microfabricated Circuits

The realization of microfabricated circuits has been performed in order to compare both numerical and analytical modeling to experimental results.

7.1 Design Considerations

The desired on chip devices included transistors, transformers, inductors with and without a metallic ground plane, and capacitors. Electrical characteristics such as conductivity, permittivity, permeability, and dielectric strength are considered when choosing available materials. A process has been designed based on tool availability and process compatibility.

All fabrication has been performed on 4 inch n-type silicon wafers. Transistors and capacitors are formed in the front-end of the process while inductors and transformers are left for back end copper processing. The ability to deposit SiO_2 on top of aluminum enables a two level metal process.

In order to obtain high capacitances on chip, the gate oxide is used as the dielectric for a MOS capacitor. The gate oxide provides a high quality dielectric of approximate thickness equal to 600 Å, and has a relative permittivity (ε_r) of 3.9. MOS (Metal Oxide Semiconductor) capacitors have been implemented using aluminum as the top electrode and heavily doped p-type silicon as the bottom electrode.

Inductors are implemented on silicon and are formed using a dual damascene copper process. Copper is chosen because of its high conductivity to reduce the conductivity losses presented. The inter level dielectric used is PECVD SiO_2. By using

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PECVD, the dielectric thickness could be built up to 10 μm and above with little mechanical film stress. The thickness of the PEVCD SiO₂ film is well suited to reduce the parasitic capacitance presented by the inductor traces. The PECVD SiO₂ deposition could be done on top of aluminum for a dual level metal process. Aluminum is used because of its relatively high conductivity and process compatibility.

The cross section and layout of a series LC tank circuit is shown in Figure 35.

Figure 35. (a) Cross section of LC tank circuit. (b) Plan view of LC tank circuit. (c) Series LC tank circuit (d) Parallel LC tank circuit.

7.2 Process Flow

The full process has been designed to begin with either n or p-type starting wafers. An optional n-well drive in is included to allow for PMOS transistors if p-type wafers are to be used. In this study, n-type wafers are used so the n-well diffusion has been omitted.

7.2.1 Front-End Process

To gain electrical contact to the substrate, n+ regions are diffused. A 0.5 μm wet thermal SiO_2 is grown and patterned where substrate contact is desired.

Figure 36. Wet thermal oxidation and oxide patterning for n+ diffusion regions.

Spin on dopant (n-type) supplies the n-type impurities (phosphorous) that are diffused into the silicon to a depth of about 1 μm.

Figure 37. n+ spin on dopant and subsequent diffusion.

The oxide is etched to the silicon surface and a new 0.5 μm wet thermal oxide is grown to block the following p type diffusion.

Figure 38. Wet thermal oxidation and oxide patterning for p+ diffusion regions.

Spin on dopant (p-type) supplies the p-type impurities (boron) that are diffused into the silicon to a depth of about 1 μm. The p-type diffusions created the source and drain regions of the PMOS and also the bottom electrode of the capacitor as shown in Figure 39.

Figure 39. p+ spin on dopant and subsequent diffusion.

The wafer Figure 39 is etched to the silicon surface and 0.5 μm of field oxide is grown. The field oxide is patterned using the active layer mask which defined dimensions for the gates on the transistors, capacitor dimensions, and regions where electrical contact to the substrate is desired (Figure 40).

Figure 40. Field oxide growth and etch for active regions.

The wafer in Figure 40 is oxidized in a dry O_2 ambient to grow a 60 nm gate oxide. The gate oxide is then etched to the silicon surface for electrical contact.

Figure 41. Growth of dry thermal gate oxide and subsequent etch for silicon contacts.

The wafer in Figure 41 is deposited with 1 µm of Aluminum using PVD (physical vapor deposition) sputtering. The aluminum is then etched to define metal 1. The ground planes for all microstrip circuitry are formed using the metal 1 pattern.

Figure 42. PVD sputter and patterning of aluminum.

The wafers are sintered in an N_2/H_2 ambient to improve the electrical contact between the aluminum and heavily doped silicon. This concluded the front end of the process. The subsequent backend is used to form inductors, transformers, and microstrip circuits.

7.2.2 Back-End Process

The back-end of the fabrication process included the deposition of a thick ILD (Inter Level Dielectric) and patterning of a copper metal level. The back-end is of greatest importance to the operation of the proposed microstrip circuitry. All microstrip patterns are formed in the top level of metal formed in the back-end process. The process has been designed as a dual-damascene copper process for maximum conductivity. After the completion of the front end, 10 μm of PECVD (plasma enhanced chemical vapor deposition) SiO_2 is deposited.

Figure 43. Deposition of ILD.

The vias required the ILD to be etched 10 µm down to the aluminum surface. The etch for metal 2 required the ILD to be etched 5 µm into the film. To create such topology in the ILD, a patterning scheme is used whereby two levels (via and metal 2) are imaged using lithography on the top surface of the ILD.

After the deposition of the SiO_2 ILD, a thin layer (30 nm-50 nm) of amorphous carbon is deposited. The carbon layer is deposited by PECVD using CH_4 as the source gas. The pattern for Metal 2 is transferred into the amorphous carbon film by using an O_2 plasma etch. Amorphous carbon has been selected because of its chemical resistance to HF (hydro-fluoric acid) and acetone. Only a few hundred angstroms are needed to block the etch of more than 10 µm of PECVD SiO_2.

Figure 44. Deposition and patterning of amorphous carbon.

Next, the pattern for via is transferred into a new layer of photoresist, which resided above the patterned amorphous carbon film. By performing the lithography for two

levels on the surface of the ILD, difficulties brought about by significant topology (5 μm-10 μm) are avoided. For example, metal 2 required an etch depth of 5 μm. If the wafer is prepared as shown in Figure 44 and etched in HF to a depth of 5 μm, the resulting topology (5 μm) would make subsequent photoresist coating and lithography very difficult for the via level. Therefore, the etch of the ILD is done after metal 2 and via are patterned in two distinct layers on top of the planar ILD (Figure 45).

Figure 45. Photoresist patterning for via level.

Via is etched to a depth of 5 μm to 6 μm, or a little over half way through the ILD. This etch provides a head start for the vias.

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Figure 46. 5 μm head start etch for vias.

Acetone is used to remove the photoresist layer, leaving the amorphous carbon film exposed. Amorphous carbon is not etched by acetone and it remains in place. The ILD is etched again in HF until the depth of metal 2 is 5 μm. During the second ILD etch, the vias are etched to a final depth of 10 μm (Figure 47). It must be noted that all ILD etching in this process etching is isotropic, which requires the dimensional biasing of the photomasks.

Figure 47. 5 μm etch of metal 2 trenches.

The amorphous carbon layer is removed using a dry O_2 plasma etch.

Next, a tantalum/copper seed layer is sputtered. The seed layer is deposited to enable the electroplating of thick copper to fill the vias and metal 2 trenches. Copper is electroplated to a thickness of 10 μm and polished back to the ILD surface using a copper CMP (chemical mechanical planarization) process. A cross section after copper CMP is depicted in Figure 48.

Figure 48. Cross section schematic after CMP.

7.2 Photomask Layout

The photomasks are designed for the fabrication process in 7.2. Each mask level had critical parameters which are listed in Figure 49.

Level	Min. Dimension [μm]	Bias [μm]	Field Type
N-well	300 μm	-	Dark
N+ select	40 μm	-	Dark
P+ select	10 μm	-	Dark
Active	20 μm	-	Dark
Active Contact	20 μm	-	Dark
Metal 1	10 μm	-	Clear
Via	10 μm	-20 μm	Dark
Metal 2	10 μm	-10 μm	Dark

Figure 49. Table of critical mask dimensions.

The minimum dimensions are listed as they would appear on the wafer after lithography. Each mask level can tolerate a maximum lateral misalignment of 2 μm.

A bias has been applied to some of the mask levels to account for the isotropic nature of the ILD etch. A bias is added to the desired dimensions to reduce the printed feature size. Isotropic etching transfers the printed feature into the ILD film with widened lateral dimension equal to twice the depth of the etch. If the etch is well controlled, the printed feature bias should cancel out the effect of lateral etching.

Figure 50. Capture of die layout showing all process levels.

Figure 50 shows the layout for the die that has been fabricated. The actual size of the die after fabrication is 2 cm x 2 cm on the wafer.

7.4 Ferrite Filling Technology

Ferrite particles have been electroplated on top of the inductors using electrophoresis (EP). EP is a process where charged particles migrate in the presence of an electric field and deposit on an electrode. In this study, ferrite particles have been produced from solid ferrite toroids. The permeability for the solid toroid material used in this study is shown in Figure 51. The material has been supplied by Ferronics Inc.

Figure 51. Permeability of solid toroids made of V-material from Ferronics [25].

Ferrite toroids have been ball milled into a fine powder and suspended in Isopropyl Alcohol (IPA) with a magnesium salt ($Mg(NO_3)_2$). To electroplate the ferrite a bias is been applied (>100V) between the anode and the wafer, which are both immersed in the ferrite/salt/IPA suspension. Ferrite particles have been deposited on top of the inductors, however no significant change in inductance has been measured. Ferrite filling technology is under development to facilitate the transport of ferrite particles under the inductor, where modeling has shown the greatest effect on inductance.

(a)   (b)

Figure 52. (a) Ball milling of toroids resulting in ferrite powder. (b) Depiction of electrophoretic plating of ferrite.

Figure 52(a) shows the resulting powder after ball milling and Figure 52(b) shows the EP electroplating setup.   Figure 53 shows a fabricated micro-inductor electroplated with ferrite.

Figure 53. Scanning electron micrograph of ferrite coated micro-inductor.

8. Experimental Results

The fabrication process yielded the wafer shown in Figure 54.

Figure 54. Photograph of fabricated 4 inch silicon wafer.

Critical measurements needed for modeling have been extracted. Film thickness measurements have been taken using surface profilometry. Profilometry has shown the thickness of the dielectric (d) to be equal to 5 μm between the bottom of the copper trenches and the aluminum metal layer. The permittivity of the ILD is not known precisely and can vary depending on the conditions of the deposition process. Electrical testing has shown that a relative permittivity of 4 produces modeled impedance responses very close to that of measured results. The conductivity of the copper is modified during modeling to estimate the effective conductivity of the electroplated copper.

8.1 Experimental Test Setup

(a)   (b)

Figure 55. (a) Network analyzer and micro-probe station. (b) Probing of copper inductor.

Figure 56. Photograph showing two port RF probing of inductor using 150 μm pitch GSG probes.

Figure 55(a) shows the Cascade Microtech probing station along with an Agilent 8363B network analyzer. Figure 55(b) shows the probing of fabricated micro-inductors. Figure 56 is a photograph taken through the microscope showing a two port measurement. One port measurements are also demonstrated in this study. A number of test setups can be used to extract the inductance of the inductor. The layout must be done considering the fixed RF probe dimensions to ensure that testing at high frequencies can be performed successfully with the available RF probes

8.1.1 RF Testing

High frequency testing has been performed using an Agilent 8363B network analyzer with 150 μm and 1000 μm pitch GSG (Ground-Signal-Ground) probes. Testing from 10 MHz to 40 GHz has been done using the 150 mm pitch GSG probes. Both one port and two port measurements have been taken directly on the wafer.

One port RF testing is the easiest method for extracting the inductance, however, it may require a dual level metal process to provide cross-unders. The inductor under test is probed by placing the center signal probe on the input terminal of the device. After traveling through the inductor, the signal is returned directly to the grounding probes located on the outside of the GSG probes. The completed current loop is necessary if inductance is to be extracted using a one port measurement.

Figure 57. Meander line inductor with a layout designed for one port inductance measurements.

The impedance (Z_{in}) recorded from the network analyzer can be used to directly determine the reactance or inductance.

$$Z_{in} = R + jX_L \tag{17}$$

Z_{in} is the complex impedance in ohms, R is the resistance in ohms, and X_L is the reactance in ohms.

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The reactance for an inductor is:

$$X_L = \omega L \tag{18}$$

where L is the inductance and ω is equal to $2\pi f$. The effective inductance can be found

by dividing the reactance determined by ω or $2\pi f$.

$$L = \frac{X_L}{2\pi f} \tag{19}$$

The quality factor is expressed as shown in (20).

$$Q = \frac{Im(Z_{in})}{Re(Z_{in})} \tag{20}$$

Two port measurements have also been used to determine the inductance,
however, a modified probing procedure must be used. Additional calculations must also
be performed to extract the inductance of the inductor.

Figure 58. Two port meander line inductor showing the placement of two ports.

For two port networks, the impedance matrix is represented as:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{21}$$

The 2 port network can be represented as:

Figure 59. Two port network showing input currents and voltages.

The expansion of (21) yields:

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

(22)

Z_{11} is defined as (23):

$$Z_{11} = \frac{V_1}{I_1}\bigg|_{I_2=0}$$

(23)

Current I_2 it forced to zero by lifting the probe on port 2 off of the wafer. The resulting impedance Z_{11} is measured using the port 1 probe.

Likewise, Z_{22} is defined as (24):

$$Z_{22} = \frac{V_2}{I_2}\bigg|_{I_1=0}$$

(24)

Current I_1 is forced to zero by lifting the probe on port 1 off of the wafer. The resulting impedance Z_{22} is measured using the port 2 probe.

Z_{12} is defined as (25):

$$Z_{12} = \frac{V_1}{I_2}\bigg|_{I_1=0}$$

(25)

If probes are placed on ports 1 and 2, I_1 cannot be forced to zero. This prohibits the direct measurement of Z_{12}. The impedance looking in port 1 can be measured while both probes are down and used to find Z_{12} by applying an equivalent circuit model.

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In order to extract the input impedance of devices from their impedance matrix, it is necessary to define an equivalent circuit representation. The T equivalent circuit can be applied to reciprocal networks in order to simplify impedance computations [26]. The T equivalent circuit is represented in Figure 60 where a, b, and c are impedances. The T equivalent circuit can be obtained as follows.

Figure 60. T equivalent circuit for a 2 port network.

Solving for (23) and (24):

$$Z_{11} = \frac{V_1}{I_1} \bigg|_{I_2=0} = a + c \tag{26}$$

$$Z_{22} = \frac{V_2}{I_2} \bigg|_{I_1=0} = b + c \tag{27}$$

Considering (25), V_1 is equal to I_2 times impedance c when $I_1=0$.

$$Z_{12} = \frac{V_1}{I_2} \bigg|_{I_1=0} = \frac{I_2 c}{I_2} = c \tag{28}$$

Substituting (28) into (27) into leads to:

$$b = Z_{22} - Z_{12} \tag{29}$$

Similarly, substituting (28) into (26) leads to:

$$a = Z_{11} - Z_{12} \tag{30}$$

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The equivalent T circuit is shown in Figure 61.

Figure 61. T equivalent circuit for a two port reciprocal network.

When Port 2 is terminated by a load impedance as shown in Figure 62,

Figure 62. Port 2 terminated by load impedance Z_L.

the input impedance looking into port 1 is written as (31).

$$Z_{in} = Z_{11} - \frac{Z_{12}^2}{Z_{22} + Z_{Load}} \tag{31}$$

In summary, Z_{11} and Z_{22} are directly found by placing a single probe on ports 1 and 2 respectively. Z_{12} cannot be found by direct measurement, however, it can be calculated from measured results if Z_L is known.

The network analyzer used in all on wafer testing had a port impedance of 50 Ω. When two port measurements are taken with both probes down as shown in Figure 58, a 50 Ω load is presented by the probe and the resulting circuit is shown in Figure 63.

Figure 63. Equivalent circuit when two port measurements are performed.

the input impedance in Figure 63 can be expressed using (32),

$$Z_{in} = Z_{11} - \frac{Z_{12}{}^2}{Z_{22} + 50} \qquad (32)$$

which can be rearranged into the form seen in (33) to solve for Z_{12}.

$$Z_{12} = Z_{21} = \pm\sqrt{(Z_{11} - Z_{in})(Z_{22} + 50)} \qquad (33)$$

Now, Z_{12} (=Z_{21}) can be obtained from measured values of Z_{11}, Z_{22} and Z_{in}.

Once the entire Z matrix for the inductor (Z_{11}, Z_{12}, Z_{21}, and Z_{22}) is known, the inductance and quality factor can be calculated for the inductor. (31) is applied by setting the load impedance Z_L to zero. This is equivalent to shorting the second terminal to ground, thereby expressing the impedance of the inductor itself. Inductance and quality factor can be calculated directly from the inductors impedance matrix.

$$Z_{in(inductor)} = Z_{11} - \frac{Z_{12}{}^2}{Z_{22}} \qquad (34)$$

$$L = \frac{Im(Z_{in(inductor)})}{2\pi f} \qquad (35)$$

$$Q = \frac{\text{Im}\Big(Z_{\text{in(inductor)}}\Big)}{\text{Re}\Big(Z_{\text{in(inductor)}}\Big)} \qquad (36)$$

L is the inductance in Henries and Q is the quality factor.

8.2 Comparison of Modeling and Measured Results

Two one turn microstrip inductors are analyzed with varying geometries. The microstrip lines have been designed to have different resonant frequencies. A meander line inductor has also been tested with and without a ground plane. The resulting inductances of the passives have been found and are compared.

8.2.1 One Turn On-Chip Inductor (Thin Side Segment)

Figure 64. Fabricated one turn inductor.

Impedance measurements have been collected using an Agilent 8363B network analyzer with 150 μm pitch GSG Cascade probes. The Z parameters have been collected from 0.5 GHz to 40.0 GHz using 201 data points.

Figure 65. (a) Z_{11} measurement. (b) Z_{22} measurement. (c) 2 ports measurement for calculating Z_{12}.

HFSS and Desegmentation are applied to the pattern in Figure 64. Desegmentation is applied with n=m=40 and a maximum q port width of 180 μm. Impedance calculations are performed from 10 MHz up to 40 GHz in steps of 100 MHz. The dielectric thickness, d, is 5 μm and the dielectric permittivity is 4. The dielectric loss tangent is set to zero and the copper conductivity is set to 5.8e7 S/m.

HFSS is simulated with a solution frequency of 30 GHz and converged to ΔS<.01. Lumped ports of 1 μm width are placed at ports 1 and 2 shown in Figure 64. Frequency steps of 100 MHz are used for the frequency sweep in HFSS. 5 μm of copper (σ=3.7e7 S/m) is used in place of a perfect electric boundary for the simulation. A perfect electric

conductor boundary is used for the ground plane. The relative dielectric permittivity is 4

and dielectric thickness, d, is 5 μm.

Figure 66. Impedance parameters for the one turn microstrip inductor in Figure 64.

Using (35) and (36) the inductance and quality factor are calculated.

Inductance

Figure 67. Inductance for microstrip inductor in Figure 64.

Quality Factor

Figure 68. Quality factor for microstrip inductor in Figure 64.

8.2.2 One Turn On-Chip Inductor (thick side segment)

Figure 69. Plan view of fabricated one turn inductor.

An Agilent 8363B is used with 150 μm pitch GSG Cascade probes. The Z parameters are collected from 0.5 GHz to 40.0 GHz with 201 data points.

Desegmentation has been applied to the pattern in Figure 69. Desegmentation is applied with n=m=40 and a maximum q port width of 180 μm. Impedance calculations are performed from 10 MHz to 40 GHz in steps of 100 MHz. The dielectric thickness, d, is 5 μm and the dielectric permittivity is 4. The dielectric loss tangent is set to zero and the copper conductivity is set to 5.8e7 S/m.

HFSS is simulated with a solution frequency of 30 GHz and converged to ΔS<.01. A lumped port of 1 μm width is placed at port 1 shown in Figure 69. Frequency steps of 100 MHz are used for the frequency sweep in HFSS. 5 μm of copper (σ=3.7e7 S/m) is used in place of a perfect electric boundary for the simulation. A perfect electric conductor boundary is used for the ground plane. The dielectric loss tangent is set to zero and the dielectric thickness, d, is 5 μm. The dielectric's relative permittivity is set to 4.

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Figure 70. Impedance parameters for the one turn microstrip inductor in Figure 69.

Using (35) and (36) the inductance and quality factor are calculated and plotted in Figure

71 and Figure 72 respectively.

Inductance

Figure 71. Inductance for one turn microstrip inductor in Figure 69.

Quality Factor

Figure 72. Quality factor Inductance for one turn microstrip inductor in Figure 69.

8.2.2 Meander Line Inductors

Meander line inductors have been designed with and without a ground plane. Two meander line inductors are shown in Figure 73.

Figure 73. Meander line inductors with and without an aluminum ground plane.

Figure 74. Zoomed plan view of meander line inductor with aluminum ground plane.

The meander line inductors have a spacing of 10 μm and a trace width of 20 μm. The meander line inductors have 31 turns resulting in a total path length of 22.8 mm. The impedance for the inductors shown in Figure 73 has been collected experimentally. Experimental data is taken using an Agilent 8363B network analyzer, and 150 μm pitch Cascade Microtech probes. A frequency sweep from 0.5 GHz to 10 GHz using 1601 frequency data points has been used.

Figure 75. One port meander line inductor with and without an aluminum ground plane.

Quality Factor

Figure 76. Quality factor for two meander line inductors with and without an aluminum ground plane.

Figure 75 shows the experimental inductance for two fabricated meander line inductors. The effect of the ground plane can clearly be seen. The self resonant frequency is lower when the aluminum ground plane is present. Figure 76 shows the effect of an aluminum ground plane on the quality factor.

8.2.3 PMOS Transistor and Diode Testing

PMOS transistors and pn diodes have been fabricated on the same wafer as inductors and capacitors. Electrical testing has been performed after copper CMP. The current-voltage relationship for the devices has been measured using an HP 4145 parameter analyzer. The a photograph of the PMOS transistor is shown in Figure 77.

(a)   (b)

Figure 77. (a) Photograph of PMOS transistor showing substrate (Sub), source (S), gate (G), and drain (D) contacts. (b) Circuit symbol for a PMOS transistor.

The transistors are tested holding the source terminal constant at ground (0V) while sweeping the drain voltage from 0 to −16 V. The gate voltage is swept from -3 V to −8 V. The current is measured and plotted versus the source-drain bias in Figure 78.

Figure 78. PMOS I-V characteristics for W=400 μm, L=10 μm.

The data collected was analyzed to extract the threshold voltage. Equation (37) describes the I-V relationship of a long channel PMOS transistor in the region of saturation [27].

$$I_{SD} = \frac{W}{2L}\left(\frac{\mu_p Cox'}{2}\right)\left(V_{SG} - |V_T|\right)^2 \tag{37}$$

W is the gate width of the transistor, L is the gate length of the transistor, μp is the effective hole mobility and Cox' is the gate oxide capacitance per unit area. I_{SD} is the source to drain current, V_{SG} is the source to gate voltage, and V_T is the threshold voltage. By plotting the square root of the drain current versus the gate voltage in the saturation region, the threshold voltage can be found as the x-intercept. The threshold voltage (V_T) has been extrapolated as −1.65 V. A photograph of the fabricated pn diode is shown in Figure 79(a).

(a)   (b)

Figure 79. (a) Photograph showing fabricated pn diode. (b) Circuit symbol for a diode.

The I-V characteristics for a diode on the fabricated wafer have been measured. The measured results are shown in Figure 80.The cathode of the diode, or the n-type region, is held constant at 0 V. The anode, or p type region, is swept from −2 V to 2 V.

Figure 80. I-V characteristics of fabricated silicon pn diode.

9. Conclusion

The characterization and implementation of an embedded planar coil inductor presents several challenges. The present work is a comprehensive study of micro inductors that includes analytical modeling, numerical simulation, in-house fabrication processes, circuit implementation in silicon, and RF measurement techniques.

9.1 Summary of Contributions

9.1.1 Analytical and Numerical Modeling

A major focus of this work is the development of an analytical technique to provide a closed form solution for rectangular inductors capable of providing input impedance data. The method is based on a desegmentation technique which removes segments from a rectangular cavity to create the inductor coil geometry. The technique has been modified and extended to allow for multiple segment removal. This adds a great deal of flexibility and allows for a greater number of geometries to be addressed. By defining the Green's function for each segment, the boundary conditions are applied to obtain a closed form expression for the Z matrix from which the inductance and Q have been obtained. The model has also been successfully applied to irregularly shaped power planes that commonly occur in mixed signal circuits.

For numerical modeling, Ansoft's High Frequency Structure Simulator (HFSS) is chosen as the preferred tool for an accurate and frequency dependent analysis. Several inductor geometries have been modeled analytically and have been validated with HFSS.

Excellent agreement has been shown for structures of millimeter and micrometer dimensions.

9.1.2 Fabrication and Circuit Implementation of On-Chip Micro-Inductors

A fabrication process has been developed to physically realize inductors and transformers with microscale dimensions using copper embedded in a thick PECVD SiO_2 film. This has been performed exclusively using technologies available in the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT. Circuits have been made that integrate the inductor with capacitors and PMOS (P-type Metal Oxide Semiconductor) transistors. The process allows for an optional aluminum ground plane under the copper structures. Capacitors have been formed using the gate oxide as a dielectric, and heavily doped silicon along with aluminum as electrodes. PMOS transistors have been implemented to provide a variable resistance leading to two varieties of LC tank circuits (parallel and series).

9.1.3 Measurement Techniques

RF measurement techniques have been developed for wafer level testing of micro-inductors on silicon. Data has been captured using an Agilent 8363B network analyzer with a frequency range from 10 MHz to 40 GHz, in conjunction with the Cascade Microtech GSG (ground-signal-ground) probes and the 9100 probe station. A calibration procedure has been developed for full two port measurements and a methodology has been optimized for measuring the impedance [Z] matrix and the scattering [S] matrix. The input impedance is extracted from the [Z] matrix and Q has been calculated. There is

agreement between experimental results, numerical results from HFSS, and analytical results from the desegmentation technique.

9.2 Future Work

A method has been developed to implement circuits with inductors and capacitors and transistors on chip as discussed in Chapter 7. Photomasks are available for the implementation of the LC tank circuits and all structures discussed in this work. The front end of the process for PMOS transistors and MOS capacitors has been completed and produced working transistors along with nanofarad range capacitors. The incorporation of the inductors has been performed on top of the PMOS and capacitors. A number of inductors exhibited successful results, however the inductor designed for the tank circuits contained fabrication defects stemming from the ILD etch. The defects seen caused both severed copper interconnect and shorted copper interconnect, ultimately resulting in failed inductor patterns. Research is underway to determine the cause of the defects so that they may be eliminated.

Improvements need to be made to enhance the performance of the fabricated circuits. It is proposed that a low temperature PECVD SiO_2 film be used for the majority of the field oxide rather than a thermal oxide. This will reduce dopant diffusion and lower the on state resistance of the transistors. The incorporation of ferrite on top of the fabricated inductors has been performed. Modeling has shown that maximum increase in inductance will be obtained when the magnetic material is placed inside the cavity formed by the inductor and ground plane. Work is currently being done to etch away the ILD and transport ferrite into the cavity.

Publications from the Present Work

Daniel W. Brown, Jayanti Venkataraman, *"Desegmentation Technique to Address Coupling in Irregularly Shaped Power Planes and Passives for Mixed Signal Application,"* IEEE AP-S International Symposium and USNC/UNC/URSI National Radio Science Meeting, Washington, DC, July 2005.

Cody Washburn, Daniel Brown, Jay Cabacungan, Jayanti Venkataraman, and Santosh K. Kurinec, *"Application of Magnetic Ferrite Electrodeposition and Copper Chemical Mechanical Planarization for on chip Analog Circuitry,"* in Materials, Integration and Technology for Monolithic Instruments edited by Jeremy A.Theil, Markus Böhm, Donald S. Gardner, and Travis Blalock (Mater. Res. Soc. Symp. Proc. 869, Warrendale, PA , 2005 D3.2.

Appendix A

A.1 MATLAB Code for Desegmentation Technique

A.1.1 Desegmentation.m (main program)

The input variables in Desegmentation.m can be edited for the desired pattern.

```
% Desegmentation Method for Multiple Segment Removal
% Daniel W. Brown
% Electrical Engineering
% Advisor: Dr. Venkataraman
% 5-03-05
% Rochester Institute of Technology

clear all % clear all variables

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Input Variables%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Material Parameters %
d=.7874e-3;sigma=inf;LossTan=0.01;er=2.33;ur=1;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Frequency Inputs %
f_start=.0001e9;                        % Start frequency
f_step=.0001e9;                         % Step frequency
f_stop=.0002e9;                         % Stop frequency
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Segment Dimensions %
A_Alpha=2e-2;                           % X dimension of gamma segment
B_Alpha=2e-2;                           % Y dimension of gamma segment
P1=[2.5e-3 0e-3];                       % Port 1 position
P2=[7e-3 2.5e-3];                       % Port 2 position
WidthP1=[0 0];                          % Port 1 width
WidthP2=[0 0];                          % Port 2 width
Segments=[1e-2 1e-2 1e-2 1e-2;6e-3 2.5e-3 2e-3 5e-3]; % [xcen1 ycen1 a1 b1;xcen2 ycen2 a2 b2;...;xcenN ycenN aN bN]
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Convergence parameters %
m_max=4;                               % x dimension eigenmodes
n_max=4;                               % y dimension eigenmode
PortsPerSeg=40;                        % Minimum of 4, and multiples of 4% (Qports per segment)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
%**************************************** PreProcessing ***********************************************

NumberOfSegments=size(Segments,1);                                  % Determines the number of segments
NumberOfPoints=(f_stop-f_start)/f_step+1;                           % Number of fequency Samples

% Place ports around the segment to be removed
for seg=1:1:NumberOfSegments
    PortPosWid(:,:,seg)=Ports(PortsPerSeg,Segments(seg,:));         % For loop that creates port placement and width matrix
end                                                                 % Different segments stored in 3rd dimension (:,:,k)
%*******************************************************

%****** Create temporary P-ports for future removal of segments and combine real unconnected P-ports ******
TempPort=[P1 WidthP1;P2 WidthP2];
if (NumberOfSegments>1)
    for addseg=2:1:NumberOfSegments
        TempPort=[TempPort;PortPosWid(:,:,addseg)];
    end
end
Pports=TempPort;                                                    % Creates initial Pport matrix
PportLength=size(Pports,1);                                         % Returns # of p ports
%*******************************************************

% Define initial Q ports 1st segment %
    Qports=PortPosWid(:,:,1);
    Ftest=Qports;
    QportLength=size(Qports,1);
%*******************************************************

%************** Fill Matrix for 2D graphing (Convert to vertices) ***************************************
FillMatrixTemp=[0 0;0 B_Alpha;A_Alpha B_Alpha;A_Alpha 0];

for FillSeg=1:1:NumberOfSegments
    FillMatrixSeg(:,:,FillSeg)=[Segments(FillSeg,1)-Segments(FillSeg,3)/2  Segments(FillSeg,2)-Segments(FillSeg,4)/2;...
                                Segments(FillSeg,1)-Segments(FillSeg,3)/2  Segments(FillSeg,2)+Segments(FillSeg,4)/2;
                                Segments(FillSeg,1)+Segments(FillSeg,3)/2  Segments(FillSeg,2)+Segments(FillSeg,4)/2;
                                Segments(FillSeg,1)+Segments(FillSeg,3)/2  Segments(FillSeg,2)-Segments(FillSeg,4)/2];
end

for FillSeg=1:1:NumberOfSegments
    FillMatrixTemp2([(1+(FillSeg-1)*4):4+(FillSeg-1)*4],:)=[FillMatrixSeg(:,:,FillSeg)];
end

FillMatrix=[FillMatrixTemp;FillMatrixTemp2];
%*******************************************************

%****************** Frequency Sweep and Segment Loop *******************************************

for f=f_start:f_step:f_stop
    f*10^-9 % display current frequency in Matlab
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Gamma Parameters (Zpp gamma) %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
JS=1;

    for iPorts=1:1:PportLength
    for jPorts=JS:1:PportLength

        a=A_Alpha;        b=B_Alpha;        %Outer Square Dimensions
        Txi=Pports(iPorts,1); Tyi=Pports(iPorts,1); Txj=Pports(jPorts,2); Tyj=Pports(jPorts,2);
        Wxi=Pports(iPorts,3); Wyi=Pports(iPorts,4); Wxj=Pports(jPorts,3); Wyj=Pports(jPorts,4);
        zij=Zij(Txi, Txj, Tyi, Tyj, Wxi, Wxj, Wyi, Wyj, a, b, d, sigma, LossTan, er, ur, f, m_max, n_max);
        Zpp(iPorts,jPorts,(f-f_start)/f_step+1)=zij;

    end
    JS=JS+1;
    end

% reflect upper triangle down to lower triangle %
LowerZpp(:,:,(f-f_start)/f_step+1)=triu(Zpp(:,:,(f-f_start)/f_step+1),1).';
Zpp(:,:,(f-f_start)/f_step+1)=LowerZpp(:,:,(f-f_start)/f_step+1)+Zpp(:,:,(f-f_start)/f_step+1);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%% Gamma Paramters (Zpq) gamma  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    for iPorts=1:1:PportLength     %P ports
    for jPorts=1:1:QportLength     %Q ports

        a=A_Alpha;        b=B_Alpha;        %Outer Square Dimensions
        Txi=Pports(iPorts,1); Tyi=Pports(iPorts,1); Txj=Qports(jPorts,2); Tyj=Qports(jPorts,2);
        Txj=Qports(jPorts,1); Tyi=Pports(iPorts,2); Wxi=Pports(iPorts,3); Wyi=Pports(iPorts,4);
        Wxj=Qports(jPorts,3);Wyj=Qports(jPorts,4);
        zij=Zij(Txi, Txj, Tyi, Tyj, Wxi, Wxj, Wyi, Wyj, a, b, d, sigma, LossTan, er, ur, f, m_max, n_max);
        Zpq(iPorts,jPorts,(f-f_start)/f_step+1)=zij;

    end
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%% Gamma Parameters (Zqq)gamma  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
JS=1;

    for iPorts=1:1:QportLength     %Q ports
    for jPorts=JS:1:QportLength     %Q ports

        a=A_Alpha;        b=B_Alpha;        %Outer Square Dimensions
        Txi=Qports(iPorts,2); Tyi=Qports(iPorts,3);Wxi=Qports(iPorts,4);
        Txj=Qports(jPorts,1); Tyi=Qports(iPorts,2);Wxj=Qports(jPorts,3);Wyi=Qports(iPorts,4);
        Txj=Qports(jPorts,2);Wxj=Qports(jPorts,3);Wyj=Qports(jPorts,4);
        zij=Zij(Txi, Txj, Tyi, Tyj, Wxi, Wxj, Wyi, Wyj, a, b, d, sigma, LossTan, er, ur, f, m_max, n_max);
        ZqqGamma(iPorts,jPorts,(f-f_start)/f_step+1)=zij;
```

```matlab
    end
    JS=JS+1;
end

% reflect upper triangle down to lower triangle %
LowerZqgGamma(:,:,(f-f_start)/f_step+1)=triu(ZqgGamma(:,:,(f-f_start)/f_step+1),1).';
ZqgGamma(:,:,(f-f_start)/f_step+1)=LowerZqgGamma(:,:,(f-f_start)/f_step+1)+ZqgGamma(:,:,(f-f_start)/f_step+1);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

end % Frequency Loop 1

%%%%%%%%%Generate Zqp by transpose%%%%%%
for flip=1:1:NumberOfPoints
    Zqp(:,:,flip)=Zpq(:,:,flip).';
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% From this point, only ZqqBeta will need to be calculated using zij sub-function %

                        % Beta Transformation
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Beta for Segment 1 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
BetaQports=Qports;
BetaQports(:,1)=BetaQports(:,1)-Segments(1,1)+Segments(1,3)./2;    % Beta x position transform
BetaQports(:,2)=BetaQports(:,2)-Segments(1,2)+Segments(1,4)./2;    % Beta y position transform
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

for BetaSegment=1:1:NumberOfSegments
    clear ZppAlpha;

if (BetaSegment==2)    % if there is more than one segment to be removed, set this initial condition
    BS=NumberOfSegments+1;
end

if (BetaSegment>1)
    clear Qports;
    clear BetaQports;
    BS=BS-1; %segment to remove

    Qports=Pports[3+QportLength*(BS-2):2+QportLength*(BS-2)+QportLength,:);
    BetaQports=Qports;
    BetaQports(:,1)=BetaQports(:,1)-Segments(BS,1)+Segments(BS,3)./2;    % Beta x position transform
    BetaQports(:,2)=BetaQports(:,2)-Segments(BS,2)+Segments(BS,4)./2;    % Beta y position transform
end

if (BetaSegment==1)
    BS=1;
end

clear ZqqBeta;
for f=f_start:f_step:f_stop
    f*10^-9 %Display Frequency%
```

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```
%%%%%%%%%%%%%%%%%%%%%%%%%%%% Beta Paramters   (Zqq) Beta   %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
JS=1;

    for iPorts=1:1:QportLength       %Q ports
    for jPorts=JS:1:QportLength      %Q ports

        a=Segments(BS,3) ; b=Segments(BS,4) ;
        Txi=BetaQports(iPorts,1); Tyi=BetaQports(iPorts,2);Wxi=BetaQports(iPorts,3);Wyi=BetaQports(iPorts,4);
        Txj=BetaQports(jPorts,1); Tyj=BetaQports(jPorts,2);Wxj=BetaQports(jPorts,3);Wyj=BetaQports(jPorts,4);
        zij=zij(Txi, Txj, Tyi, Tyj, Wxi, Wyi, Wxj, Wyj, a, b, d, sigma, LossTan, er, ur, f, m_max, n_max);
        ZqqBeta(iPorts,jPorts,(f-f_start)/f_step+1)=zij;

    end
    JS=JS+1;
    end

    % reflect upper triangle down to lower triangle %
    LowerZqqBeta(:,:,(f-f_start)/f_step+1)=triu(ZqqBeta(:,:,(f-f_start)/f_step+1),1).';
    ZqqBeta(:,:,(f-f_start)/f_step+1)=LowerZqqBeta(:,:,(f-f_start)/f_step+1)+ZqqBeta(:,:,(f-f_start)/f_step+1);

end % Main Frequency Loop End
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%Generate ZppAlpha to determine properties of matrix %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
for FShoot=1:1:(f_stop-f_start)/f_step+1
    ZppAlpha(:,:,FShoot)=Zpp(:,:,FShoot)-Zpq(:,:,FShoot)*((ZqqGamma(:,:,FShoot)-ZqqBeta(:,:,FShoot))^-1)*Zqp(:,:,FShoot);
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

if (BetaSegment<NumberOfSegments)
    n=size(ZppAlpha,1);         %Return size of ZppAlpha
PortsPerSeg=QportLength;

%%%%%%%%%%%%%%%%%%%%%%%%%%%Reorders P ports to Q ports %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Zpp=ZppAlpha([1:n-PortsPerSeg],[1:n-PortsPerSeg],:);                %ZppNEW
Zpq=ZppAlpha([1:n-PortsPerSeg],[n-PortsPerSeg+1:n],:);              %ZpqNEW
Zqp=ZppAlpha([n-PortsPerSeg+1:n],[1:n-PortsPerSeg],:);             %ZqpNEW
ZqqGamma=ZppAlpha([n-PortsPerSeg+1:n],[n-PortsPerSeg+1:n],:);    %ZqqNEW
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
end

end % Beta Segment Loop End

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Extraction of Z and S Parameters %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
for f=f_start:f_step:f_stop
    Z11pp((f-f_start)/f_step+1)=ZppAlpha(1,1,(f-f_start)/f_step+1);
    Z12pp((f-f_start)/f_step+1)=ZppAlpha(1,2,(f-f_start)/f_step+1);
    Z21pp((f-f_start)/f_step+1)=ZppAlpha(2,1,(f-f_start)/f_step+1);
    Z22pp((f-f_start)/f_step+1)=ZppAlpha(2,2,(f-f_start)/f_step+1);
    Zmatrix(:,:,(f-f_start)/f_step+1)=[Z11pp((f-f_start)/f_step+1) Z12pp((f-f_start)/f_step+1); Z21pp((f-f_start)/f_step+1)...
                     Z22pp((f-f_start)/f_step+1)]/50;
```

```
        Smatrix(:,:,(f-f_start)/f_step+1)=(Zmatrix(:,:,(f-f_start)/f_step+1)+eye(2))^-1*(Zmatrix(:,:,(f-f_start)/f_step+1) -
eye(2));
        S11pp((f-f_start)/f_step+1)=20*log10(abs(Smatrix(1,1,(f-f_start)/f_step+1)));
        S12pp((f-f_start)/f_step+1)=20*log10(abs(Smatrix(1,2,(f-f_start)/f_step+1)));
        S21pp((f-f_start)/f_step+1)=20*log10(abs(Smatrix(2,1,(f-f_start)/f_step+1)));
        S22pp((f-f_start)/f_step+1)=20*log10(abs(Smatrix(2,2,(f-f_start)/f_step+1)));
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Plotting Options %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
f=[f_start:f_step:f_stop]; %Frequency Vector

% Plotting S, Z, L,Q %
figure()

% Plotting of 2-D Circuit Pattern %
subplot(2,2,1)
patch(FillMatrix([1:4],1),FillMatrix([1:4],2),'b')

for Seg=1:1:NumberOfSegments
    patch(FillMatrix([Seg*4+1:Seg*4+4],1),FillMatrix([Seg*4+1:Seg*4+4],2),'w','EdgeColor','r');
end
patch(P1(1,1),P1(1,2),'r');
patch(P2(1,1),P2(1,2),'r');

xlabel('X [m]')
ylabel('Y [m]')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Plot Impedance Parameters vs. Frequency %
subplot(2,2,2)
plot(f*1e-9,imag(Z11pp),'b',f*1e-9,imag(Z21pp),'g',f*1e-9,imag(Z22pp),'r',f*1e-9,real(Z21pp),'r')
title('Imaginary Part of Z11(blue), Z21(green), Z22(red)')
xlabel('Frequency [GHz]')
grid on
ylabel('Imaginary part of Impedance [ohms]')
grid on
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% S parameters %
subplot(2,2,3)
plot(f*1e-9,S11pp,'b')%,f*1e-9,S12pp,'g',f*1e-9,S22pp,'r');
title('Scattering Matrix S11(blue), S21(green),S22(red)')
xlabel('Frequency [GHz]')
grid on
ylabel('S in [dB]')
grid on
%%%%%%%%%%%%%%%

% Inductance, Quality factor
```

```
L=10^9*(imag(Z11pp-Z12pp.*Z21pp./(Z22pp)))./(2*pi*f);
R=(real(Z11pp-Z12pp.*Z21pp./(Z22pp)));
C=-1./(imag(Z11pp)*2*pi.*f);
Zoo=real(sqrt((L*10^-9)./(C)));
Q=(imag(Z11pp-Z12pp.*Z21pp./(Z22pp)))./(real(Z11pp-Z12pp.*Z21pp./(Z22pp)));
subplot(2,2,4)
plot(f*1e-9,L),f*1e-9,Q);
title('Inductance')
xlabel('Frequency [GHz]')
grid on
ylabel('Inductance [nH]')
grid on
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

A.1.2 Zij.m

This module is called from the main program (Desegmentation.m) and returns the impedance between two ports on a rectangular microstrip cavity.

```
% Zij.m
% Zij using Green's Function for Rectangular Geometries
% This program will determine the Zij for a 2 ports
% network.  The port can be placed anywhere in the x-y plane.
% This code was intended to be used in conjunction with a Desegmentation program.
% Daniel W. Brown
% 10-28-04
% Advisor: Dr. Venkataraman
% 2-port verified 11-1-04

function [Z]=Zij(Txi, Txj, Tyi, Tyj, Wxi, Wxj, Wyi, Wyj, a, b, d, sigma, LossTan, er, ur, f, m_max, n_max)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Constants%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    uo=1.25663706144e-6;                    %Permeability of Free Space
    eo=8.85418781762e-12;                   %Pemmitivity of Free Space [F/cm]
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Variables%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    m=[0:1:m_max]';                         %m vector
    n=[0:1:n_max];                          %n vector
    chi=4.*ones(m_max+1,n_max+1);chi(1,:)=2;chi(:,1)=2;chi(1,1)=1;   %NormConsts for greens (m&n dependent)
    bx=m.*ones(m_max+1,1).*pi./a;bx=nncopy(bx,1,n_max+1);           %kx matrix
    by=n.*ones(1,n_max+1).*pi./b;by=nncopy(by,m_max+1,1);           %ky matrix
    Skin=sqrt(2/(2*pi*f*uo*ur*sigma));       %Skin depth
    beta=2*pi*f*sqrt(eo*er*uo*ur)-j*2*pi*f*sqrt(eo*er*uo*ur)*(LossTan+Skin/d)/2;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%Impedance Equation and Summation - result is in variable
Z%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Z=j*(2*pi*f)*ur*uo*d/(a*b).*chi./(bx.^2+by.^2-
beta.^2).*cos(bx.*Txi).*cos(bx.*Txj).*cos(by.*Tyi).*cos(by.*Tyj).*sinc(bx.*Wxi./(2*pi))...
    .*sinc(bx.*Wxj./(2*pi)).*sinc(by.*Wyi./(2*pi)).*sinc(by.*Wyj./(2*pi));
Z=cumsum(Z);Z=Z(m_max+1,:);Z=sum(Z);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

A.1.3 Ports.m

The dimensions and placement of the segment to be removed is input into this

module and the placement and dimensions of the ports around the periphery of the

segments is returned.

```
% Ports.m
% Geometrical Definition of Port Placement %
% Daniel W. Brown
% Places ports around a given rectangle
% Returns a Matrix with port characteristics [posx posy widx widy]
% Used for 4 Rectangle
% 1-26-05

function [P]=Ports(PortsPerSeg,Segments)

x_cen=Segments(1,1);
y_cen=Segments(1,2);
a=Segments(1,3);
b=Segments(1,4);

 SideMultipleX=PortsPerSeg/4;
 SideMultipleY=PortsPerSeg/4;

 SideWidthX=a/SideMultipleX;
 SideWidthY=b/SideMultipleY;

% Revert Back to Initial Port Code %

%%%%%%%Top And Bottom%%%%%%%%%
for index=1:1:SideMultipleX
    PositionXT(index,1)=x_cen-a/2-SideWidthX/2+index*SideWidthX;
    PositionYT(index,1)=y_cen+b/2;
    WidthXT(index,1)=SideWidthX;
    WidthYT(index,1)=0;
end
    PositionXB=PositionXT;
    PositionYB=PositionYT-b;
    WidthXB=WidthXT;
    WidthYB=WidthYT;
Answer=[PositionXT PositionYT WidthXT WidthYT;PositionXB PositionYB WidthXB WidthYB];
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%Left and Right%%%%%%%%%
for index=1:1:SideMultipleY
    PositionXL(index,1)=x_cen-a/2;
    PositionYL(index,1)=y_cen-b/2-SideWidthY/2+index*SideWidthY;
    WidthXL(index,1)=0;
    WidthYL(index,1)=SideWidthY;
end
    PositionXR=PositionXL+a;
    PositionYR=PositionYL;
    WidthXR=WidthXL;
    WidthYR=WidthYL;
Answer=[Answer;PositionXL PositionYL WidthXL WidthYL;PositionXR PositionYR WidthXR
WidthYR];
P=Answer;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

Appendix B

B.1 Back-End Process Flow

The back-end of the process discussed in this work received the greatest amount of development. The detailed steps used are expanded upon in Appendix B.

B.1.1 Amorphous Carbon Deposition

The deposition of amorphous carbon has been performed in chamber 4 of the DryTek Quad cluster tool located in the Plasma Etch of the SMFL.

Parameter	Value
Chamber	4
Gas	CH_4
Gas Flow	55 sccm
Power	300 w
Pressure	165 mT
Time	30 seconds
Deposition Rate	0.99 nm/sec

Figure 81. Parameters for amorphous carbon deposition in DryTek Quad.

The film thickness can only be measured if the deposition in done on a bare silicon wafer using an ellispometer. Once verified, the deposition is done on the 10 μm SiO_2 ILD.
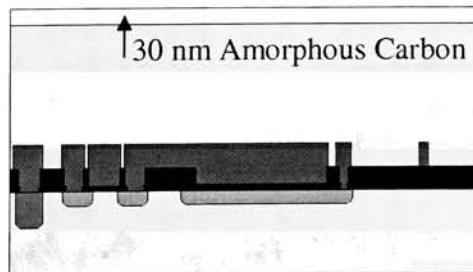

Figure 82. Deposition of amorphous carbon.

B.1.2 Patterning of Amorphous Carbon Film

Once the amorphous carbon film is deposited, photoresist is coated. The dehydration bake is bypassed and the wafer is spin coated with approximately 1 μm of photoresist. A soft bake is performed at 65 degrees Celsius for two minutes. Lithography is then performed to transfer the pattern for metal 2 into the photoresist. A manual hand develop is done in CD-26 TMAH (tetra methyl ammonium hydroxide) developer for 60 seconds and rinsed with DI water. After development, a post bake is done at 65 degrees Celcius for two minutes. The temperature is kept low to prevent the degradation of the carbon film. The amorphous carbon etch is performed in chamber 4 of the DryTek Quad located in the Plasma Etch of the SMFL. A dry oxygen plasma is used to etch the carbon film, but also etches the photoresist. The etch is stopped once the carbon film is over etched by 100%. It has been found that 1 mm of photoresist will block the etch of the carbon film. When the etch is complete the photoresist is stripped off with acetone. The acetone will not etch the carbon film.

Parameter	Value
Dehydration Bake	NONE
Soft Bake Temp	65 C
Soft Bake Time	120 seconds
Post Bake Temp	65 C
Post Bake Time	120 seconds
Development Time	60 seconds

Figure 83. Specialized lithography details.

Parameter	Value
Chamber	4
Gas	O_2
Gas Flow	55 sccm
Power	200 W
Pressure	300 mT
Time (100% Over Etch)	120 seconds
Etch Rate	0.52 nm/sec

Figure 84. 30 nm amorphous carbon etch.

Figure 85. Completed etch of amorphous carbon film and strip of resist.

B.1.3 Patterning of Photoresist for Vias

The dehydration bake is bypassed and the wafer is spin coated with approximately 1 µm of photoresist. A soft bake is performed at 65 degrees Celsius for two minutes. Lithography is then performed to transfer the pattern for via into the photoresist. A manual hand develop is done in CD-26 TMAH (tetra methyl ammonium hydroxide) developer for 60 seconds and rinsed with DI water. After development, a post bake is done at 65 degrees Celsius for two minutes. The temperature is kept below 65 degrees Celsius to prevent the degradation of the carbon film.

Parameter	Value
Dehydration Bake	NONE
Soft Bake Temp	65 C
Soft Bake Time	120 seconds
Post Bake Temp	65 C
Post Bake Time	120 seconds
Development Time	60 seconds

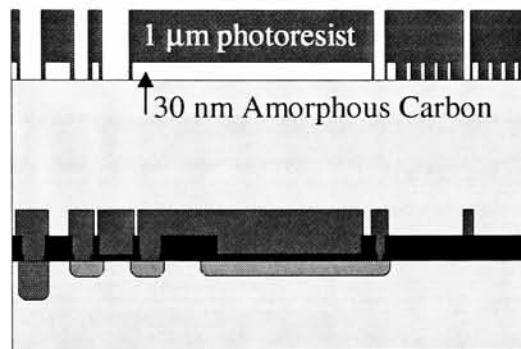Figure 86. Specialized lithography details.

Figure 87. Cross section of via pattern in photoresist and metal 2 in carbon film.

B.1.4 Two Level Etch Process

Etching the ILD film has been performed using a buffered oxide etch (BOE). The etch has been performed in a BOE bath where aluminum contaminants are acceptable. The etch rate of the SiO_2 film is 120 nm/min. This etch rate is dynamic and must be measured prior to etching the device wafers. The first etch step is done to a 5 μm or 6 μm depth.
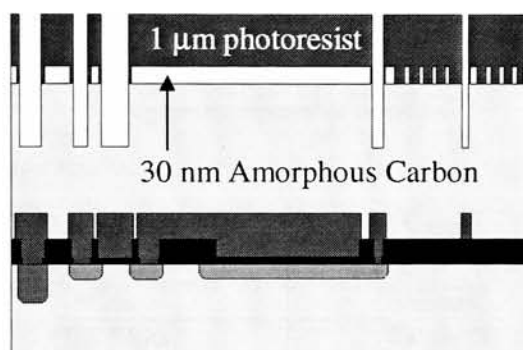

Figure 88. 5 μm etch into SiO_2 film (ILD).

The photoresist is stripped off leaving the amorphous carbon film to block the metal 2 etch. Metal 2 is etched to a depth of 5 μm.
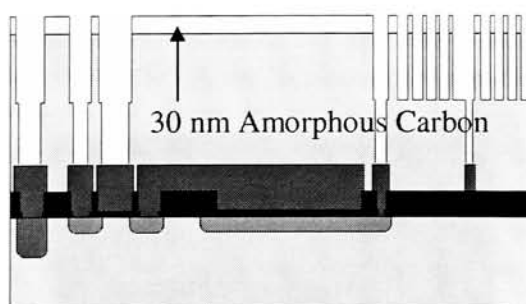

Figure 89. Additional 5 μm etch for vias, and 5 μm etch for metal 2.

The amorphous carbon film is removed using the etch recipe in Figure 84 for 10 minutes.

B.1.5 Metalization and CMP

Once the stencil is in place for the vias and metal 2 a deposition of a thin seed layer is performed to enable thick electroplating. A tantalum layer is deposited first using sputtering, then a copper layer is sputtered without breaking vacuum.

Parameter	Value
Base Pressure	1.3×10^{-6} Torr
Gas	Argon
Gas Flow	45 sccm
Power	250 W
Pressure	9.7 mT
Sputter Time	5 min

Figure 90. Sputter of tantalum.

Parameter	Value
Base Pressure	1.3×10^{-6} Torr
Gas	Argon
Gas Flow	45 sccm
Power	250 W
Pressure	9.7 mT
Sputter Time	10 min

Figure 91. Sputter of copper.

The copper seed layer is then electroplated in a copper sulfate solution at a current of about 1 A for 30 minutes. The deposition rate has been measured to be approximately 0.37 μm/min at 1 A.
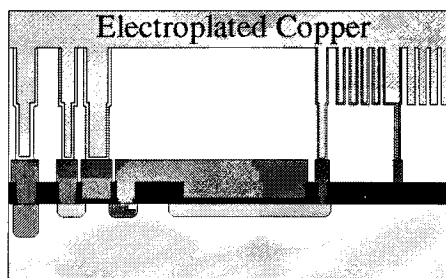

Figure 92. Thick electroplated copper.

Parameter	Value
Chemical	Copper Sulfate
Current	1.0 A
Deposition Rate	0.37 μm/min

Figure 93. Electroplating parameters.

Chemical mechanical planarization has been performed using a two phase slurry from EKC Micorplanar. CMP2001 and CMP2007 have been used for polishing. CMP2001 is an alumina based abrasive. CMP2007 is a copper oxidizer. 5 lbs/in^2 is used for the down-force. Polishing times of 1 hour to 3 hours have been necessary for planarization to the SiO$_2$ surface. Visual endpoint detection is used and the wafer is inspected every 10 minutes.

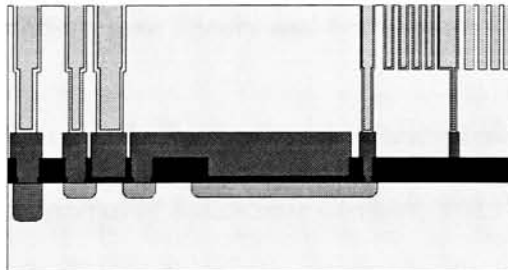| Component	Volumetric Percentage
CMP9001	25 %
CMP9007	50 %
DI water	25 %

Figure 94. Composition of slurry for copper polishing.

Figure 95. Polished wafer.

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