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Built-in-self-test of RF front-end circuitry

Anand Gopalan

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BUILT-IN-SELF-TEST OF RF FRONT-END CIRCUITRY

by

ANAND GOPALAN

A DISSERTATION

Submitted in partial fulfillment of the requirements
For the degree of Doctor of Philosophy
in
Microsystems Engineering
at the
Rochester Institute of Technology

May 2005

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Built-In-Self-Test of RF Front-end Circuitry

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ABSTRACT
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Title Built-In-Self-Test of RF Front-end Circuitry

Fuelled by the ever increasing demand for wireless products and the advent of deep submicron CMOS, RF ICs have become fairly commonplace in the semiconductor market. This has given rise to a new breed of Systems-On-Chip (SOCs) with RF front-ends tightly integrated along with digital, analog and mixed signal circuitry. However, the reliability of the integrated RF front-end continues to be a matter of significant concern and considerable research. A major challenge to the reliability of RF ICs is the fact that their performance is also severely degraded by wide tolerances in on-chip passives and package parasitics, in addition to process related faults. Due to the absence of contact based testing solutions in embedded RF SOCs (because the very act of probing may affect the performance of the RF circuit), coupled with the presence of very few test access nodes, a Built In Self Test approach (BiST) may prove to be the most efficient test scheme. However due to the associated challenges, a comprehensive and low-overhead BiST methodology for on-chip testing of RF ICs has not yet been reported in literature.

In the current work, an approach to RF self-test that has hitherto been unexplored both in literature and in the commercial arena is proposed. A sensitive current monitor has been used to extract variations in the supply current drawn by the circuit-under-test (CUT). These variations are then processed in time and frequency domain to develop signatures. The acquired signatures can then be mapped to specific behavioral anomalies and the locations of these anomalies. The CUT is first excited by simple test inputs that can be generated on-chip. The current monitor extracts the corresponding variations in the supply current of the CUT, thereby creating signatures that map to various performance metrics of the circuit. These signatures can then be post-processed by low overhead on-chip circuitry and converted into an accessible form. To be successful in the RF domain any BIST architecture must be minimally invasive, reliable, offer good fault coverage and present low real estate and power overheads. The current-based self-test approach successfully addresses all these concerns. The technique has been applied to RF Low Noise Amplifiers, Mixers and Voltage Controlled Oscillators. The circuitry and post-processing techniques have also been demonstrated in silicon (using the IBM 0.25 micron RF CMOS process). The entire self-test of the RF front-end can be accomplished with a total test time of approximately 30µs, which is several orders of magnitude better than existing commercial test schemes.

Abstract Approval: Committee Chair _______________________________________
Program Director _______________________________________
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4
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My time at RIT, completing my graduate studies has been a wonderfully illuminating and yet an incredibly humbling experience. I came here thinking that I knew a little bit about electrical engineering and circuit design. I leave knowing, that I know nothing in comparison to the infinite landscape of knowledge that is out there waiting to be re-discovered. All that I can do is to express my sincere and humble gratitude to the people who have made this journey a fruitful one.

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You have always believed in possibilities for my life that I could not even imagine. Through all my trials and tribulations, your mere presence has given me all the strength and stillness that I have ever needed.

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Thank you for introducing me to the wonderful world of RF engineering. I have truly come to appreciate the science and the art of circuit design under your able tutelage.

To Ajay
Now I know what it feels like to have a brother. I mean that in both a positive and negative way!

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Thank you for just being there, and for putting up with me and my weirdness.
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CHAPTER 1: INTRODUCTION

“There is plenty of room at the bottom”, Feynman said. The room in the bottom is rapidly running out for standard CMOS. The relentless march towards miniaturization, driven by the implacable demands of Moore’s law has led us into the murky depths of the nanometer regime. With gates a few atoms thick and close to 200 million transistors on a single chip, the boundaries of science are being tested with every new technology node.

The far reaching implications of this new era have not gone unnoticed in the glamorous world of digital design. Several scientists have tried to estimate the fundamental limits of existing digital design paradigms from various perspectives [1,2,3] in the quantum era. However, future directions are less clear along the rarified paths of analog and RF design. It is only over the past few years that challenges and paradigm shifts on the nanometer horizon are beginning to be examined in the analog world.

The most visible effect of the mounting challenges is a drastic drop in the reliability and yield of RF and high speed analog parts over the last few technology nodes. Many major design houses now go through iterations numbering in double digits to realize a successful part. There are several specific reasons for this phenomenon. The advent of deep submicron CMOS has enabled the integration of RF circuits along with analog, mixed-signal, digital and DSP subsystems on a single die. Thus the complexity and diversity of the environment in which the RF part resides has increased considerably. Interactions occur at various hierarchical levels on the chip and in the package though diverse mechanisms such as substrate coupling, the power supply system and other electrical/electromagnetic effects.
Although considerable research time and dollars have been devoted to the
development of accurate models to predict and quantify these interactions, there is still no
comprehensive technique that can accurately model all them. The other key factor in
determining yield is the list of process related factors (both faults and soft variations) that
can affect the performance of the part. This list has continued to grow exponentially with
each major technology node. RF circuits are not only affected by hard process faults as in
the case of digital circuits, but also by soft variations in process parameters, quality
factors of on-chip passives and effects in the package. Each scaling step calls into serious
question, the ability to design and fabricated RF IC products in the presence of this
massive list of process, package and passive related variations.

The most important technique used to enhancing the reliability of integrated
circuit products in general and RF ICs in particular, is the test and verification flow. This
is also a complex issue in the GHz domain. Probing solutions cannot be used due to the
high frequencies involved. The very act of probing will often modify the performance of
the circuit under test (CUT). Additionally, in highly integrated transceivers with tightly

Fig.1. Typical commercial System in a Package with integrated RF circuits
integrated RF cores, probing may not even be possible due to the absence of valid test access points. Even standalone RF ICs, such as single chip LNAs or Mixers require the use of expensive high frequency ATE testers that take several hundred milliseconds to test a single part [4]. There is therefore no accepted test practice that can ensure successful binning of parts in the GHz regime; already plagued by the expanding list of challenges described earlier.

The current work offers a cost-effective, on-chip solution to this reliability conundrum that is facing the wireless and high speed communication industry. We demonstrate a current-based technique for the self-test of RF and high speed communication circuitry functioning in the GHz regime. The self-test methodology resides completely on-chip and can self-test the entire RF front-end in a matter of microseconds, with very minimal real-estate and power overheads. The technique uses test stimuli of moderate precision and mostly baseband or DC processing circuitry. The BIST architecture does not require sophisticated off-chip computation or the presence of a DSP core.

The application of this current-based self test technique is demonstrated, both through simulation and experimentation for the three most commonly used circuits in the RF front-end; the Low Noise Amplifier, The Single Balanced Mixer and the Voltage Controlled Oscillator.
CHAPTER 2: BACKGROUND WORK

RF integrated circuits have become ubiquitous in the current age of high speed communication. Fuelled by this dramatic increase in the demand for wireless IC products, RF testing has begun to receive some attention in recent literature. A few attempts have been made in the recent past to address the increasingly critical issue of RF IC testing. Most of these techniques are either partially or completely off-chip. This chapter will briefly describe and critique the foremost among these methods. It is important to note at this point, that a comprehensive self-test methodology for on-chip testing of RFICs, has not yet been observed in literature.

2.1. Advances in Mixed-Signal Testing

For the purpose of the current discussion, one can broadly define the mixed-signal domain to comprise of circuits such as ADCs and DACs, PLLs and other analog circuits that function in the low MHz frequency range. The key element that sets these circuits apart from RF circuits, is the fact that the parasitics associated with the transistor and interconnects can still be neglected in the “mixed-signal” domain. It is however instructive to examine the self-test techniques that have been proposed in this regime, since they are the first testing schemes that use “analog” specifications to successfully bin parts. These methods, therefore form the basis for analog specification based testing, which is also the underlying approach used in the current work. Additionally, some of the tests developed in this area may form the basis for future techniques that can be applied to RF testing.
Analog to Digital Converters have received considerable attention for the implementation of built-in-self-test (BiST) schemes. Many of these techniques use on-chip DACs to test the ADC and vice versa [5,6]. Significant research has been carried out towards reducing the resolution requirements of the DAC that is used for the self-test of the ADC. The ultimate aim of this work is to be able to test a high resolution ADC with a DAC of much lower precision and associated overheads [7]. Techniques such as the histogram based self-test, examine a histogram of ADC's response to a fixed analog stimulus such as a ramp or sinusoid to quantify its performance [8]. The MADBIST technique uses a complex on-chip system comprising of ADC, DAC and processing circuitry to create a test framework for a wide range of mixed-signal circuitry (including sigma-delta converters) [9]. Most of these techniques utilize significant on-chip circuitry such as converters, digital logic and memory. Some of these techniques may have applicability in the RF domain as well. Many RF transceiver systems have on-chip ADCs, and currently research work is currently being carried out to examine the possibility of using them to test for certain structural faults in the RF CUT [10].

Another mixed-signal circuit that has the subject of considerable investigation is the Phase Locked Loop (PLL). Several on-chip techniques have been proposed, to quantify various PLL parameters such as jitter, lock frequency, cycle slip and zero-crossings. Additionally, a completely on-chip scheme to self-test high speed PLLS has also been demonstrated [11]. Some of these techniques such as the use of the Hilbert or Morlet transform require the presence of a DSP core and consequently have high overheads associated with them. Some of the other approaches, such as the zero crossing
detector [12] may have applicability in RF test as well, for example in the quantification of VCO phase noise. However, the challenges involved in adapting these circuit topologies to the GHz regime have not been surmounted yet.

### 2.2. Optimized Test Stimulus Generation & Signature based Testing

The optimal stimulus testing approach is a statistical approach that has been developed by the Packaging Research Center at Georgia Tech. This approach was developed initially for the testing of low frequency analog circuits such as OPAMPS. Figure 3 shows a simplified flow chart of this approach.

![Optimized Test Stimulus Approach](image)

**Fig.2. Optimized Test stimulus approach**
The starting point for the approach is the circuit under test (Circuit C) and a comprehensive list of soft faults that could degrade its performance. Using these two sets of information, “Fault simulation” is performed as described in [13]. The fault simulation develops a mapping between the process parameters that could vary, and the corresponding degradation in the specifications of the circuit. This information is then used to define the boundaries of an optimization problem. Using an optimization algorithm such as the genetic algorithm and with massive amounts of simulation, an optimal test stimulus is arrived at, that would cause the largest perturbation in the output space for variations in the parameter space [13]. The circuit is then tested with this test stimulus to arrive at a signature, which maps to variations in the specification space. This signature can then be compared with the output of the CUT, to determine the extent of variation in the parameters. This method is basically a statistical approach to the problem of testing. The method is also very time and computation intensive. Every new circuit requires massive amounts of prior simulation and optimization. This information must then be used to create optimal stimuli and signatures, which then need to be integrated into the system [14]. Both the stimuli and the signatures can vary vastly even within the same class of circuits. In the RF domain, the optimal test stimulus can be very complex and impossible to generate on-chip without significant overheads. Additionally, this approach only accounts for process variations, but not for performance degradation due to package and passive effects which are more frequent in RF circuits. In the case of RF circuits, the technique uses very simplistic “behavioral models” to perform fault simulations. These models are not adequate to represent the performance metrics of the RF CUT [15]. This work is however important from the point of view of its contribution
to the general field of signature based testing, although its application to the RF domain remains limited.

2.3. Loop-Back BiST

A technique that has received significant attention over the past couple of years is the loop-back approach to RF BiST. The approach in itself is not new and has been derived from testing techniques used in point-to-point radios. [16]. A similar technique was proposed by [17] for integrated RF transceivers. This work proposed that the digital data after being processed through the entire transmitter chain, should be “looped back” to the receiver. The data received at the output of the receiver is then processed using sophisticated DSP techniques to extract fault information about the entire system. The technique is only successful in quantifying very general performance metrics that affect global transceiver performance. In order to accomplish this, it requires the presence of a sophisticated DSP core on-chip. The loopback technique was further refined by the work in [18]. In this work, the authors now proposed the use of the on-chip base-band processor itself to post-process the received data. They also presented a theoretical basis for co-relating certain vector based digital tests with spot defects in RF circuit blocks. However, as in most work on fault signatures proof that a particular fault causes a change in the signature, does not conclusive establish that the signature can be used to distinguish all classes of that fault either by itself or taken concurrently with other faults. Additionally, the method has been proved using a very simplistic MATLAB based behavioral model of the RF transceiver. Even in the presence of these caveats the technique demonstrates only a moderate ability to isolate faults in the RF block. For example faults close to the receiver output cannot be detected [18]. In summary, although
the loop-back BiST does offer some fault coverage and is completely on-chip, the associated overheads do not adequately justify its use. The end-to-end approach described in [19] also proceeds along similar lines to the loopback technique.

2.4. Other techniques proposed in literature

There have been some other minor efforts published in literature, which have varying degrees of applicability to integrated RF front-end testing. One approach that has been suggested in [20] is to use an on-chip signal generator to feed a test input to the CUT, the output of which is then digitized using a sigma delta converter. This digital signature is then used to map to soft faults in the mixed signal circuit [20]. All though this technique has been applied very successfully to mixed signal circuits, its application to RF circuits is very challenging and has not yet been successfully demonstrated. A technique called the oscillation technique [21] has been successfully used with amplifiers where positive feedback is deliberately introduced into the amplifier and the performance of the circuit can be judged by measuring the frequency of oscillation. All though this techniques has some merit it cannot be easily integrated into an RF front end environment without intruding significantly on the performance of the circuits. Also, this technique cannot be applied to other classes of circuits such as VCOs and Mixers. The possible instability introduced into the system, by including a positive feedback loop may act as a deterrent towards its commercial applicability. A technique that uses the transient voltage at the output of LNAs to achieve self-test has been proposed in [22]. However, this method has very little practical applicability, due to the massive overheads and significant intrusion on the CUT.
2.5. Commercial Techniques for RF Testing

The main emphasis of commercial production based techniques is the successful and reliable binning of parts while minimizing test cost. In RF parts, test cost can comprise up to 50% of the device cost [23], with the part spending as many as 4-5 seconds on the tester. In the absence of comprehensive BiST solutions, testing in the commercial arena has proceeded along mostly traditional lines. Most RF test regimes in the industry today, utilize extremely expensive high speed testers in conjunction with standard S parameter and spectrum based tests [24]. In the early nineties, there was a major effort to move towards single frequency measurements in conjunction with optimization of hardware resources and the number of software instructions [23]. With the advent of high speed ATE, these activities have now moved into the arena of ATE design. In recent literature, some attempts have been made to move towards modulated and multi-tonal test signals to enhance fault coverage and reduce the total number of tests. [24,25]. Although this holds considerable promise, comprehensive multi-tonal test solutions have not yet been reported in literature. The current work will demonstrate the efficacy of this approach, by using tests based on multi-tonal test inputs, as part of the on-chip self-test.
CHAPTER 3: THE CURRENT-BASED APPROACH TO TESTING

Fuelled by the extensive demand for wireless products, the reduction of test cost and time to market of RF ICs has become a critical need. As seen in Chapter 2, although some attempts have been made, a comprehensive on-chip test solution for integrated RF front-ends has not yet been achieved. This chapter examines the overall concept of the current-based self-test approach and establishes a theoretical validity for its use in the context of RF front-end circuitry.

3.1. The proposed approach

In the current work, we propose an approach to RF self-test that has hitherto been unexplored both in literature and in the commercial arena. We propose to use a sensitive current monitor to extract variations in the supply current drawn by the CUT. These variations are then processed in time and frequency domains to develop signatures. The acquired signatures can then be mapped to specific behavioral anomalies and the locations of these anomalies.

Supply current based testing schemes have been used on a widespread basis in the digital world [26] [27]. In schemes, such as the IddQ and Delta IddQ, the magnitude of the supply current above or below a predetermined threshold is used to detect faults in the circuit under test (CUT) [26]. However, in the analog domain, more complex methods need to be applied. Although, there have been a few investigations in this area in the low frequency domain [28-30], this approach is completely novel when applied to the high frequency RF world. In this domain, the circuit performance information is usually contained in the high frequency current spectrum of the circuit under test.
The process of self-test can be split into three key functions. 1) Generating a test stimulus. 2) Extracting current variations and mapping them to hard and soft faults in the RF circuit. 3) Analyzing the current signatures at the output of the monitor and converting them into an easily accessible form.

![General Architecture for current-based Self-Test of RF circuits](image)

**Fig.3. General Architecture for current-based Self-Test of RF circuits**

Figure 3 shows a functional block diagram describing the proposed architecture of the current-based self test scheme for RF circuits. The CUT is first excited by simple test inputs that can be generated on-chip. The current monitor extracts the corresponding variations in the supply current of the CUT, thereby creating signatures that map to various performance metrics of the circuit. These signatures can then be post-processed by low overhead on-chip circuitry and converted into an accessible form. To be successful in the RF domain any BIST architecture must be minimally invasive, reliable, offer good fault coverage and present low real estate and power overheads. The current-based self-test approach successfully addresses all these concerns. However, in order to
achieve self-test in lieu of all these factors, several important issues need to be investigated and addressed.

Firstly, the point of interface between the BiST circuitry and the RF CUT needs to be determined, such that there is minimal intrusion on the CUT performance. As described in detail in Chapter 4, there are several choices for the point of interface. As a result of a detailed study, the BIST circuitry has been interfaced with the various circuits in the RF front-end through a sensing resistor, which is connected with minimal intrusion in the return current path of the LNA, mixer and VCO. Additionally, the process of self-test must also not be affected by variations in the BIST circuitry itself. To ensure this, the current monitor and the post-processing circuitry used for self-test have been constructed to be fairly robust with respect to process, supply and temperature variations. All the circuitry is also designed to occupy minimal area and consume relatively low power. It is important to note that since the same current monitor and post processing circuitry are used to self-test all the circuits in the front-end, overall area and power overheads are extremely small. Further more, since these circuits will only be powered on during self-test, the power consumption is only temporary. The proposed methodology can also handle concurrent faults since it shifts the focus from quantifying the faults themselves to quantifying the performance parameters that they will affect. Due to this the technique also has very good fault coverage as will be demonstrated in the results presented in Chapter 4.
3.2. Validity of the current-based approach

In this section, we examine the theoretical validity of the current-based approach to self-test introduced in the previous section. In order to do this, we have to theoretically prove that perturbations in the RF circuit performance, caused by process related faults in its components can be correlated to variations in its current spectrum. As a test case, let us consider a standard cascode LNA, which has a widespread presence in several terrestrial RF applications, as well as in current day RF literature. The input section of this amplifier consists of the gate inductor, the active amplifying device and source inductor as shown within the dotted box in the Figure 4(a). We also add a very small resistor $R_s$ (7 ohms) in series with the source coil to serve as a sensing element. The motivation behind the choice of this particular position for the sensing resistor is explained further in Chapter 4.

![Fig 4(a) Standard Cascode LNA (b) Simplified Equivalent circuit of input section](image)

Fig 4(a) Standard Cascode LNA (b) Simplified Equivalent circuit of input section
The equivalent circuit of this section obtained by replacing the lower transistor with its basic equivalent model is as shown in Figure 4(b). We have elected to ignore the Miller capacitance due to the gate drain capacitor because it is an extremely small valued capacitor going to ground that can be ignored in practical cases. If we assume the resistor to be ideal, then the instantaneous voltage across the resistor will be directly proportional to the transient current flowing through the main branch of the LNA. This current is the same as the instantaneous current drawn by the LNA from the power supply or the return current from the LNA to ground. If the input voltage to the LNA is $V_{IN}$, then we have

$$V_{DS} = i \frac{g_m}{C_{GS}} + i \left[ j \omega (L_S + L_G) \right] + \frac{1}{j \omega C_{GS}} + i R_s + i \frac{g_m R_s}{j \omega C_{GS}}$$

$$\therefore i = \frac{V_{IN}}{\frac{g_m L_S}{C_{GS}} + j \left( \omega (L_S + L_G) - \frac{1}{j \omega C_{GS}} \right) + R_s - \frac{j g_m R_s}{\omega C_{GS}}}$$

(1)

Therefore, the voltage across the resistor $R_S$ is given by

$$V_{GS} = i R_s + i \frac{g_m R_s}{j \omega C_{GS}}$$

$$= \frac{V_{DS} R_s \left[ 1 - \frac{j g_m}{\omega C_{GS}} \right]}{\frac{g_m L_S}{C_{GS}} + j \left( \omega (L_S + L_G) - \frac{1}{j \omega C_{GS}} \right) + R_s - \frac{j g_m R_s}{\omega C_{GS}}}$$

(2)

In the presence of the resistor the input match frequency occurs when

$$\omega (L_S + L_G) = \frac{1 + g_m R_s}{\omega C_{GS}}$$

(3)

As seen from the equation (2), the voltage across the resistor $R_S$ will also be its maximum at this frequency.
\[ V_{Rs} \text{(match)} = \frac{V_{IN} R_S \left[ 1 - \frac{jg_m}{\omega C_{GS}} \right]}{\frac{g_m L_s}{C_{GS}} + R_S} \]

Hence, the current in the return path of the LNA due to the test input \( V_{IN} \) is given by

\[
\frac{V_{Rs}}{R_s} = \frac{V_{IN} \left[ 1 - \frac{jg_m}{\omega C_{GS}} \right]}{\frac{g_m L_s}{C_{GS}} + j\left( \omega (L_s + L_G) - \frac{1}{\omega C_{GS}} \right) + R_s - \frac{jg_m R_s}{\omega C_{GS}}} \quad (4)
\]

This analysis indicates that the voltage across the resistor \( R_S \) is dependant on the frequency of match as dictated by the inductances and capacitances in the input network of the LNA, in addition to being frequency dependant. This is an important result because it establishes that any fault in a component in the input section indicated in Figure 2 will be reflected as a variation in the current spectrum (since voltage across \( R_S \) is directly proportional to the current). The above mathematical analysis can be carried a step further to determine the variation in the current spectrum due to soft variations in the various components in the network. Figure 5 shows the variation in the current spectrum due to a +/- 25% variation in gate inductance which is typical in most applications. The resultant spectrum shows that the point of maximum current (and maximum voltage across the resistor) moves with the variation in gate inductance.
This is due to the fact that the variations in $L_G$ cause a variation in the optimal match frequency of the LNA. Similarly, Figure 6 shows the variation in the current spectrum due to a +/- 25% variation in $L_S$.

In the cascode LNA, the variation in $L_S$ does not significantly change the optimal frequency of the match, but varies the magnitude of the match. As seen in Figure 6, this phenomenon is also accurately reflected in the current spectrum where the peak current.
varies in magnitude, although the frequency at which this occurs stays constant. It is important to note here that the change in current spectrum due to a change in the sense resistor $R_S$, would have a similar effect on the current spectrum as a change in $L_S$. This is however acceptable because the change in magnitude of the input match ($S_{11}$) would also be similar for these to variations. Since we are attempting to quantify the specification of the CUT (in this case $S_{11}$) and not the actual cause of the fault, this is acceptable. However, to be useful, the technique must be able to distinguish between a variation in the current spectrum due to an actual fault versus a variation in the spectrum due to a slightly different value in the quiescent current drawn from the supply. Figure 7 shows the variation in the current spectrum due to a +/- 30 % variation in the bias current of the LNA.

![Graph showing theoretical variation in sensed current spectrum with +/- 30% variation in Id]

**Fig.7. Theoretical variation in sensed current spectrum with +/- 30% variation in Id**

It can be seen from Figure 7, that the variation in the current spectrum due to change in the quiescent current is much lower and of a different nature than variations due to the above described faults. In fact, it is apparent that the instantaneous ac voltage across the resistor is much more sensitive to faults in the LNA rather than to variations in the
quiescent bias current. In Figure 4(b), we have assumed a complete isolation between the input and output side due to the cascode. However, if a finite coupling were assumed, it would be possible to quantify faults on the output side of the LNA as well. A similar analysis can also be carried out for single balanced mixers and VCOs indicating that faults in the RF circuit due to soft variations in the passives as well as process related faults can be quantified in the current spectrum as sensed by a resistor in the return path of the circuit-under-test. From equation (4) one can also see that the resultant current spectrum is directly dependent on $V_{\text{IN}}$ or the test input voltage. From the above discussion one can envisage using a carefully selected set of test inputs at different frequencies to quantify the variations in the current spectrum, thereby carrying out a “self-test” of the RF circuit.

Another fact that becomes apparent from the Figures (5-7) is that the magnitude of the voltage variations across the resistor $R_S$ corresponding to faults is in the order of a few mV. So an important piece of such a current based BiST system is a sense amplifier or current monitor circuit that would amplify these variations to a level where they can be processed by other post-processing circuitry. Since all these current variations occur in the GHz frequency range such an amplifier must also have a wide bandwidth so that it can provide sufficient magnification of the signal at the frequencies of interest.

### 3.3 Merits and Demerits of the current-based self-test approach

The greatest advantage of the current-based approach to self-test is minimal intrusion. Since the return current of the CUT is being tapped to estimate its performance, there is very little need for redesign or co-design of the RF circuit. Also, in integrated RF front-ends this maybe the only test access point that is universally available for all
circuits. It has also been shown that perturbation in any of the major performance parameters of any major RF front-end block will be reflected in a change in its current spectrum. These two factors together make return current, the ideal vehicle for extracting performance information. When used in conjunction with smart test stimuli and robust post-processing the method achieves self-test with extremely low test times in the microsecond range. This is several orders of magnitude better than previously reported test times which range in hundreds of milliseconds. Since all circuits have the same test access point (namely the return path), it is now possible to use the same circuitry to self-test the entire front-end. This results in dramatically low real-estate and power overheads.

The current based approach does however have some inherent drawbacks. Although the power overheads are insignificant when taken in the context of the entire front-end, they may be significant during test mode, if the methodology were applied to a stand alone RF circuit such as a single chip LNA. The power overhead for the entire test scheme is about 15% of the power consumption of a standard LNA. Having said that, it must be noted that due to extremely small test times in the microsecond range, which represents only transient power consumption during test mode. The other major drawback of the technique is its inability to detect noise performance using simple, low overhead circuitry. In order to estimate noise performance from current, significantly more sophisticated circuitry and processing techniques need to be developed.
CHAPTER 4: IMPLEMENTATION AND SIMULATIONS

Having previously established the general approach towards RF self-test, this chapter will delve into the implementation of the various blocks that make up the BiST scheme. With the help of theory and Spectre simulations, we will establish the performance of a wide bandwidth current monitor that extracts the high frequency current information from the RF CUT and low overhead post-processing circuitry that can convert this information into an easily accessible form. We will also demonstrate the minimally intrusive interface of the BiST circuitry with various RF circuits under test. Finally, with the use of smart test techniques and test stimuli of moderate precision, the entire BiST scheme will be utilized to self-test a cascode LNA, a Mixer and a Voltage controlled oscillator.

4.1. A Wideband Current Monitor for self-test of Low GHz RF circuits

4.1.1. Requirements of a Sense Amplifier for current based BiST of RF circuits

One of the key requirements for a current monitor used in high frequency applications is high bandwidth, in the order of several GHz, to enable the circuit to sense performance information over the entire frequency range of operation of the CUT. This would enable sensing of high frequency current transients in the supply current. Traditional RF circuits, like LNAs, draw several milliamperes of current. The monitor must, therefore, have a sufficiently high input dynamic range to be able to sense currents of that order. The circuit must also be relatively insensitive to process variations so that non-catastrophic faults in the sensor itself will not affect the process of information gathering and self-test. Most importantly, the monitor should be non-intrusive such that
its presence does not affect the performance of the CUT. Additionally, it is desirable that it has low real estate and power overheads.

4.1.2. Modified Current Amplifying Cell-Theory

Traditional trans-impedance amplifiers such as those used in optical communication systems [32] occupy significant real estate. In many cases, the resultant area of the sense amplifier would be larger than the LNA itself. [33]. Therefore, this work presents an alternate approach to this problem by using a modified wideband current conveying structure to carry out the bulk of the amplification. Figure 8 shows the diagram of the current amplifying cell [34] which was developed by the authors initially for the purpose of current-based testing of digital circuitry.

![Current Amplifying Cell Diagram](image)

**Fig.8. Current Amplifying Cell**

The current amplifying cell essentially uses the current conveyer in inverse operation [35] thereby causing it to function as a “voltage mirror”. Figure 9 shows the schematic of such a simple “voltage mirror”. As seen in the figure, if the current ratios and transistor sizes are set as shown, then the voltage at the gate of M2 will be the same as the voltage applied at M1 ($V_G$). This property allows one to convey the same voltage level from the
input of the cell to its output. One result of this property is that it is possible to cascade several of these amplifying cells without the need for a level shifter. Additionally due to the transistor ratios, a current at the input branch will be amplified at the output branch similar to a current mirror.

\[ \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_5}{L_5} = M \]

Additionally the sizes of the output transistors M7 and M8 are related to the input transistors in the ratio

\[ \frac{W_8}{L_8} = \frac{W_7}{L_7} = N \]
Now if the input current is say increased by $\Delta I$ then current in M1 decreases and that in M2 increases by $\Delta I_1$. This also means that a negative feedback current of $M\Delta I_1$ is fed back to the input node, resulting in

$$\Delta I = \Delta I_1 + M\Delta I_1$$

(7)

And

$$\Delta I_1 = \frac{\Delta I}{M + 1}$$

The load current $\Delta I_L$ is given by

$$\Delta I_L = N\Delta I_1 = \frac{N}{M + 1} \Delta I$$

Consequently the DC current gain $A_i$ is given by

$$A_i = \frac{\Delta I_L}{\Delta I} = \frac{N}{M + 1}$$

(8)

In order to calculate the AC gain, we use the small signal model shown in Figure 8

From the figure, we can derive the following system of equations

$$\begin{cases}
g_{m1}v_{in} - g_{m1}v_{s2} = i_{in} - g_{m3}v_{gs3} \\
-g_{m1}v_{in} + (g_{m1} + g_{m2})v_{s2} = 0 \\
g_{m4}v_{gs7} = g_{m2}v_{s2}
\end{cases}$$

(9)

Also at the output node we have

$$i_L = g_{m7}v_{gs7}$$

(10)

This system of equations can be written as
\[
\begin{pmatrix}
g_{m1} & -g_{m1} & g_{m3} \\
g_{m1} & g_{m1} + g_{m2} & 0 \\
0 & -g_{m2} & g_{m4}
\end{pmatrix}
\begin{pmatrix}
v_{in} \\
v_{x} \\
v_{y}
\end{pmatrix}
= \begin{pmatrix}
i_{in} \\
0 \\
0
\end{pmatrix}
\]  

(11)

Therefore, we can solve for \(v_y\) as

\[v_y = \frac{i_{in}}{g_{m3} + g_{m4}}\]

Using eqn 10 we have

\[
\frac{i_L}{i_{in}} = \frac{g_{m7}}{g_{m3} + g_{m4}}
\]  

(12)

Although this structure has a relatively high bandwidth in comparison to traditional current mirrors, the bandwidth is still insufficient for its use in the GHz regime. So the current work presents a modification to the current amplifying cell, trading off its gain for a higher bandwidth by using a “current sample-voltage summing” type of feedback structure. Figure 11 shows a schematic of the new current amplifying cell.

![Modified Current Amplifying Cell](image)

**Fig. 11. Modified Current Amplifying Cell**
The resistors $R_{f1}$ and $R_{f2}$ are used to feed back a part of the load current to the input. When the input current is zero, the output current is also zero as dictated by equation (5-8) and the circuit is in equilibrium. Now, if the input current increases, the load current increases, which causes a part of the load current to flow through $R_{f2}$. The corresponding voltage across $R_{f2}$ is feedback to the input side. Therefore, the effective $V_{IN}$ increases causing the resultant $\Delta I$ to decrease due to equation (7). This establishes a negative feedback structure where gain is traded off for a higher bandwidth. To explore this trade-off further, we consider the small signal equivalent of the modified amplifying cell. It must be emphasized that even the small signal model is only a low frequency equivalent of the circuit. At the GHz frequency range, the equivalent circuit encompassing parasitic capacitances becomes too complex for a detailed mathematical analysis. However, the small signal analysis presented below serves to illustrate the trade-off of the current gain of the cell towards greater bandwidth. The increase in bandwidth to the GHz range will then be demonstrated further using simulation and experimental results.

The output voltage for the cell $V_{OUT}$ in this case is given by

$$V_{OUT} = \frac{i_L[R_L R_{f2}]}{R_L + R_{f2}} (13)$$

The system of equations in (9) now becomes

$$g_{m1}V_{IN} - g_{m1}V_{SG2} = i_{IN} - g_{m3}V_{GS3} + \frac{i_L R_L R_{f2}}{R_L + R_{f2}} + \frac{V_{IN}}{R_{f1}}$$

$$-g_{m1}V_{IN} + (g_{m1} + g_{m2})V_{SG2} = 0$$

$$g_{m4}V_{GS7} = g_{m2}V_{SG2} (14)$$

Also, we have the load current $i_L$ given by
\[ iL = \left[ g_{M1}V_{GS1} + \frac{V_{IN}}{R_{f1}} \right] \frac{R_{f1}(R_L + R_{f2})}{(R_{f1}R_{f2} + R_{f2}R_L + R_{f1}R_L)} \]  

(15)

The above system of equations can be written in matrix form as

\[
\begin{bmatrix}
g_{M1} & \frac{-1}{R_{f1}} & -g_{M1} & g_{M3} \\
-g_{M1} & (g_{M1} + g_{M2}) & 0 & V_x \\
0 & -g_{M2} & g_{M4} & V_y \\
\end{bmatrix}
\begin{bmatrix}
V_{IN} \\
V_x \\
V_y \\
\end{bmatrix}
= \begin{bmatrix}
i_{IN} + \frac{i_L R_L}{R_L + R_{f2}} \\
0 \\
0 \\
\end{bmatrix}
\]

(16)

It can be seen that if feedback is removed in the above system it reduces to the basic

current amplifying cell case in equation (11)

Solving the above system, we have the current gain \( A_i \) is given by (Eqn 17)

\[
A_i = \frac{\left[ g_{M1}g_{M2}g_{M4} + g_{M1}g_{M4} + g_{M2}g_{M4} \left( R_{f2} + R_L \right) \right]}{g_{M1}g_{M2}g_{M4} \left( R_{f2} + R_L + R_{f1} + R_{f2} \right) + \left( R_{f2} + R_L \right) g_{M1} + g_{M2}g_{M4} + g_{M1}g_{M2}g_{M3} \left( R_{f2} + R_L + R_{f1} + R_{f2} \right) + \frac{R_{f2} R_L}{R_{f1} R_{f2}}} \]

(17)

Therefore, the current gain as indicated by equation 12 has now been degraded to that
indicated by equation (17). To illustrate this, let us consider all trans-conductances to be

equal. In this case, the current gain in equation 12 reduces to \( A_i = 0.5 \). If the same

assumption made with equation 17, \( A_i \) reduces to

\[
A_i = \frac{(g_M + 2)(R_{f2} + R_L)}{g_M \left( R_{f2} R_L + 2R_{f1} R_L + 2R_{f1}R_{f2} \right) + 2(R_{f2} + R_L)}
\]

This term has a value less than 0.5 for any realistic selection of resistances \( R_{f1} \), \( R_{f2} \) and

\( R_L \). In addition to increasing the bandwidth, the feedback mechanism also significantly
enhances the insensitivity of the circuit to process variations as will be demonstrated in

next section.
4.1.3. Current Monitor Design

![Figure 12: Current based Sense amplifier for RF testing](image)

Fig.12. Current based Sense amplifier for RF testing

The schematic of the complete current monitor is shown in Figure 12. The sensing element ($R_S$) is used to drop part of the supply current across itself and generate a voltage which is used for further processing. Investigations were carried out on using inductive, capacitive and resistive elements to sense the current. The resistor was chosen because it provides a frequency independent, linear relationship, between the relevant current information and the input to the current monitor. The sensing resistor connects to the rest of the circuit through a source follower (Stage1). The current flowing through the source follower is set by the voltage drop across the sensing resistor and it provides the bias for the inverter following after. The first stage is chosen as a source follower to isolate the RF CUT from the remainder of the self-test circuitry. Additionally, it also provides a relatively broad and flat bandwidth over the entire range of frequencies of interest. The inverter (Stage2) acts as a buffer between the sensing stage and the amplifying cell (Stage 3), increasing the current swing and providing additional gain. In order to increase the
bandwidth, it was found necessary to limit the number of inverting amplifiers in the gain stage to just one, which resulted in increasing the cutoff frequency of the pole in the gain stage. The operation of the amplifying cell is explained in sub-section 4.1.2.

In order to achieve a constant gain over the frequency range of interest, sizes of M7 and M8 have been increased. This caused a reduction in the channel resistance of the transistors, seen at the output of the amplifying cell, thus increasing the pole frequency of the amplifying cell. The other transistors in the amplifying cell were resized to maintain the ratios for current gain and appropriate DC levels. In addition to readjusting the sizes of the transistors in the current amplifying cell, while maintaining the same basic circuit configuration, feedback was added to the amplifying cell as described in sub-section 4.1.2, yielding a higher bandwidth, as well as stability and insensitivity to process variations, by sacrificing the gain. The feedback also removes the sensitivity to the bias point.

The value of the sensing resistor has been chosen to be 7Ω and has been implemented as the effective resistance of four resistors at higher values in parallel with each other, taking into account high resistor tolerances. The lower resistor value avoids a significant loss of dynamic range and intrudes minimally on the RF circuit-under-test. However, a lower sensing resistor value minimizes the sensitivity of the amplifier to faults in the CUT. Therefore the resistor value is an optimal solution for the trade-off between reducing the intrusion on the CUT on one side and achieving sufficient sensitivity to be able to adequately detect variations in the RF circuit specifications.

Since the gain stage, consisting of only one inverting amplifier, is not extremely sensitive to the bias point, variations in the value of the resistor can be tolerated without
affecting the overall circuit performance. Finally, since the feedback mechanism depends on the ratio of the two resistors, and not their actual values, it is also fairly insensitive to the resistor tolerance. The circuit was designed in the IBM 0.25 micron 6 metal layer RF CMOS process. Table 1 shows the dimensions and values of the various devices in the circuit.

<table>
<thead>
<tr>
<th>Source Follower</th>
<th>M5(W/L) (µm/µm)</th>
<th>136./0.5</th>
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</thead>
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<tr>
<td>MSF(W/L)(µm/µm)</td>
<td>100/0.24</td>
<td></td>
</tr>
<tr>
<td>Rf (Ω)</td>
<td>331</td>
<td></td>
</tr>
<tr>
<td>Rs (Ω)</td>
<td>7</td>
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<tr>
<td><strong>Second Stage</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MP1(W/L)(µm/µm)</td>
<td>60/0.24</td>
<td></td>
</tr>
<tr>
<td>MN1(W/L)(µm/µm)</td>
<td>2.64/0.24</td>
<td></td>
</tr>
<tr>
<td><strong>Amplifying Cell</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1(W/L) (µm/µm)</td>
<td>100/0.5</td>
<td></td>
</tr>
<tr>
<td>M2(W/L)(µm/µm)</td>
<td>36.3/0.5</td>
<td></td>
</tr>
<tr>
<td>M3(W/L) (µm/µm)</td>
<td>36.6/0.5</td>
<td></td>
</tr>
<tr>
<td>M4(W/L) (µm/µm)</td>
<td>12.12/0.5</td>
<td></td>
</tr>
<tr>
<td>M7(W/L) (µm/µm)</td>
<td>110/2 m:2</td>
<td></td>
</tr>
<tr>
<td>M8(W/L) (µm/µm)</td>
<td>147/2 m:6</td>
<td></td>
</tr>
<tr>
<td>M9(W/L) (µm/µm)</td>
<td>7.6/0.5</td>
<td></td>
</tr>
<tr>
<td><strong>Feedback</strong></td>
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<td></td>
</tr>
<tr>
<td>Rf1 (Ω)</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>Rf2 (Ω)</td>
<td>323</td>
<td></td>
</tr>
<tr>
<td>RL (Ω)</td>
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<td>Ibias (µA)</td>
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</tr>
<tr>
<td>C (bypass) (pF)</td>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

Table 1. Current Monitor Design Parameters
4.1.4 Simulation Results for Current Monitor

The sense amplifier circuit was designed in the IBM 0.25 micron 6 metal RF CMOS process. The functionality of the circuit was verified by simulating it in the Cadence environment with signal source frequencies of 10Hz-9GHz, DC current of 10mA and AC magnitude ranging from 500uA to 2mA.

![Current Gain Diagram](image)

**Fig.13. Gain and 3dB frequency of sensor (Simulation)**

Figure 13 shows current gain measured across the load $R_L$. Current gain of the amplifier is 29.8 dB with –3dB frequency at 3.7GHz, which makes this circuit suitable for testing of RF circuits operating in the lower Gigahertz range. The feedback in the current amplifying cell establishes a gain vs. bandwidth trade-off, enabling us to choose optimum values for the gain and bandwidth depending on the requirements and frequency of operation of the CUT. In addition to gain, it is also very important for the behavior of the sensor to be in itself relatively independent of process variations, so that the behavior of the self-test mechanism is robust and reliable. To validate this, a Monte Carlo analysis was performed using a three sigma distribution for process variations on all components.
and transistor mismatches. Added feedback in the current sensor makes the circuit less sensitive to the process variations and, although the gain varies by about 10dB, the frequency response stays relatively constant (see Figure 14). This is an acceptable performance, since the test methodology used to estimate performance (explained in Section 4.4) will depend on relative amplitudes between two signals and thus be independent of the actual numerical gain. One of the process corners shows a slight bump in the frequency response of the monitor. This could cause a problem in detection if the test inputs used for self-test fell on either side of the bump. For a reliable self-test the frequency response of the monitor must be monotonic and predictable over the frequency range of interest. Taking into consideration that some RF circuits, such as LNAs, might be drawing high DC current, it is important for the sensor to perform satisfactorily over this current range. Figure 15 shows the linearity of the sensor in range of +/- 20mA. The output is inverted due to the inverter in the second stage. The sensor was found to exhibit a high degree of linearity over the entire range of possible currents drawn by the RF CUT.

![Fig.14. Monte Carlo analysis for the current sensor](image-url)
4.1.5. Current Monitor Layout Issues

The layout of the RF current sensor was done in IBM, 6 metal layers, 0.25\(\mu\)m technology and is shown in Figure 16. The total area of the sensor layout is 2760\(\mu\)m\(^2\) (where as half of it is occupied by the bypass capacitor), which represents a real estate overhead of approximately 0.5% for a standard LNA.

A large fraction of the area is occupied by an on-chip MIM capacitor that provides a high frequency bypass for the monitor. This ensures that the performance of the circuit is not affected drastically by parasitics in the power supply system. The resistors used in the circuit have also been laid out in a symmetrical scheme using the same building blocks to
ensure superior matching. The sense resistor has been constructed using silicided polysilicon to achieve the smallest tolerance that is afforded by the IBM process. The expected tolerance of the sense resistor [31] is 11%.

4.2. Minimally Invasive Interface of Bist Circuitry

4.2.1 Minimally invasive Interface of Sense Amplifier with RF CUT (LNA) – Theory and Simulation

The most important property of any successful BIST scheme is that it should have a minimal impact on the performance of the CUT. In the entire RF front-end, the LNA is the sub-circuit whose performance is most sensitive to external factors. Therefore, the issue of minimal intrusion is especially critical to the LNA. Due to this, the standard single ended cascode LNA has been used as a test case to examine the optimal means of interfacing the sense amplifier with the RF CUT. The analysis presented in this section can however be extended to RF mixers as well, since they have the same general topology at the RF input port. In order to sense the current drawn from the power supply, the sensing resistor $R_S$ needs to be in the main current path. As described in Section 4.1, the voltage across $R_S$ acts as the input to the current monitor.

![Fig.17. Possible Insertion points for sensing element](image-url)
Figure 17 shows the three possibilities for inserting the sensing element in the signal path. In order to perform these tests, a 1.67GHz single ended LNA designed in the IBM 0.25-micron process was used. Fig 18 shows the performance of the LNA in the absence of the testing circuitry. The four parameters that have been measured are the Input match (S11), the output match (S22), the gain (S21) and the noise figure (NF).

![Graph showing performance of LNA in absence of sensor](image)

**Fig 18 Performance of LNA in absence of sensor**

The first possibility, as shown in Figure 17(a), is to insert $R_s$ near the drain of the upper transistor in the cascode pair of the LNA. In this case, the resistor is in series with the drain inductor, degrading its Q. Therefore, the gain of the LNA ($S_{21}$) and the output match ($S_{22}$) will be degraded. The noise figure is also slightly degraded. As seen in Figure 19, $S_{22}$ is degraded drastically from $-15.98\text{db}$ at operating frequency to $-5.28\text{db}$. The gain also degraded from $11.79\text{ db}$ to $5.59\text{ db}$. There is no significant change in $S_{11}$, but noise figure goes up slightly from the initial value of $2.1\text{db}$ to $2.5\text{db}$ due to the presence of the resistor.
The second option is to insert the sensing resistor in series with the bypass capacitor as shown in Figure 17(b). Almost every RF circuit has a bypass capacitor connected between its supply rails to supply a majority of the high frequency current for the circuit, thereby avoiding the high impedance parasitics of the bond wire or solder bump on the power supply path from the external world. Therefore, a resistor in series with this capacitor would be able to sense a significant fraction of the high frequency supply current drawn by the CUT. This seems like an ideal solution since the resistor is not even directly in the signal path. Fig 20 shows the LNA performance in this case. Again as seen from Fig 20, $S_{22}$ degrades very significantly to $-6.37\text{db}$. The gain $S_{21}$ is also reduced from $11.79\text{ db}$ to $6.4\text{db}$. The noise figure however, is not as affected as in the first case. This massive degradation in gain and output match is because although the resistor does not seem to be in the direct current path, since a large portion of the current is drawn from the bypass capacitor, the resistor is in the low resistance path to ground. Therefore, this is also not a viable insertion point for the sensor. The final option as...
shown in Fig 17(c), is to insert the sensor in series with the source inductor. In essence, we are measuring the current flowing into ground. Fig 21 shows the LNA performance in this case. As seen in Fig 21, $S_{22}$ and $S_{21}$ are almost completely unaffected. $S_{11}$ as expected degrades from $-31 \text{ db}$ to $-16.3 \text{ db}$. From these results, it can be seen that the degradation in $S_{11}$ is not as severe as that seen in $S_{22}$ and $S_{21}$ in the previous cases.

![Fig.20. LNA parameters with sensing resistor in series with bypass capacitor](image)

**Fig.20. LNA parameters with sensing resistor in series with bypass capacitor**

The main advantage of this configuration however, is that it is possible to co-design the LNA with the resistor in the equation for input match. When the LNA was redesigned using this method, simply by adjusting the values of gate and source inductors by less than 25% it was possible to achieve an input match almost identical to the one in the absence of the resistor as shown in Figure 11. As seen in Figure 22, it was possible to redesign the LNA for an input match of $-27.09 \text{ db}$, which buys back most of the input match for the circuit. The noise figure also degrades from $2.178 \text{ db}$ to $2.6 \text{ db}$. Addition of the sensing resistor at the source also increases the linearity of the amplifier. Therefore, we conclude that the least intrusive point of insertion for the current sensor is in series with the source inductor as shown in Figure 17(c). Even though this affects the input
match slightly, it is possible to co-design the LNA with the sensing resistor in mind and get a comparable S11. The only drawbacks of using this insertion point are a slight degradation in noise figure, and the loss of some dynamic range.

![Fig.21. LNA parameters with sensing resistor in series with source inductor](image1)

**Fig.21. LNA parameters with sensing resistor in series with source inductor**

![Fig.22. S11 of the LNA after co-design](image2)

**Fig.22. S_{11} of the LNA after co-design**
4.2.2 Interfacing the BiST circuitry with a VCO

We use the standard balanced LC oscillator, designed for a fundamental oscillation frequency of 2.2GHz for the simulations in this section. There are two possible locations again for the insertion of the sensor, at the supply side and at the return path. If the sensor were inserted in series with the tail current transistor of the oscillator at the supply side, it would not be possible to capture the actually oscillation current. We would only be looking at the mirror current. Therefore, we insert the sensing resistor in the return path in series with the oscillating transistor pair as shown in Figure 23.

![Schematic of typical VCO interfaced with sensing resistor (Rs)](image)

**Fig.23. Schematic of typical VCO interfaced with sensing resistor (Rs)**

This has a very small affect on the performance of the VCO. The only appreciable affect was a 40M shift in the VCO frequency. This is due to the small difference between the source and the back gate voltage for the NMOS transistors. However, the presence of the resistor can be taken into account during design to compensate for the shift. The resistor will also introduce phase noise into the oscillator. But if the value of the resistor is much
smaller than the inverse of the transconductance (1/gm) for the MOSFETs, the channel noise due to the FETs will dominate the phase noise expression. This condition is easily satisfied in most standard sub micron CMOS processes. In the current example 1/gm = 800 ohms, which is two orders of magnitude greater than the value of the sense resistor (7 ohms). Due to this, the sense resistor contributes negligibly to the overall phase noise of the VCO. Figure 24 shows the phase noise profiles in the presence and absence of the resistor. As seen from the simulations in figure, the presence of the sense resistor has an extremely minimal impact on VCO phase noise.

Fig.24. Phase noise of VCO with and without Rs

In the case of the standard balanced VCO, it is also possible to completely dispense with the sense resistor and current monitor, by directly interfacing the post-processing circuitry to the output of the VCO as shown in Figure 25. The VCO output is usually designed to maximize output power making it possible to directly extract performance information without the need for amplification. Also, interfacing the circuit to the output of the VCO does not drastically impact its performance. The only effect is a reduction in the tuning range of the VCO, due to the fixed input capacitance of the post-processing circuitry now directly shunted across the tank.
Fig. 25. Schematic of typical VCO directly interfaced to post-processing circuitry

However, this would require the use of separate post processing circuitry for the self-test of the VCO. Since it is absolutely necessary to use a sensing element to self-test the LNA and the mixer, we use the same system for the VCO as well to minimize the overhead due to extra VCO post-processing circuitry.

4.2.3 Interfacing the BiST circuitry with a Single Balanced Mixer

In this section, we use the test case of a standard CMOS single sideband mixer designed for an RF input of 2.45 GHz and a local oscillator frequency of 2.4GHz. The sensor has two points of interface with the mixer, the RF signal path and the local oscillator signal path. Therefore, while testing the mixer the sensor first switches to the RF path and then to the Local oscillator (LO) path. The sensing resistors in both these paths, as shown in Figure 26, do not affect the performance of the mixer significantly. In fact the sensing resistor in the RF path increases the source degeneration, thereby improving the linearity of the mixer. The 1 dB compression point for the mixer went
from **-4.86 dbm to -0.8 dbm** after introducing the resistor. There is no affect on input match since the mixer can be co designed with the resistor to get back the input match similar to the LNA as described in sub-section 4.2.3. In the LO side the resistor is in the bias network and therefore has no effect on the LO path which is usually 50 ohm terminated.

![Fig.26. Schematic of Single Balanced mixer](image)

### 4.3. Extracting Performance Information from the Sensed Current

#### 4.3.1. Sensing LNA performance

Three types of faults were introduced into the input side of the LNA. The first fault involved an error between actual inductance of the gate inductor and the inductance value in design. Figure 21 shows the variation in the input match (S11) of the LNA. As seen in Figure 27, the input match shifts to the left as the gate inductance increases from 4nH to 8nH. The frequency of match moves from the original 1.68 GHz to 1.4 GHz.
Figure 27. Variation of $S_{11}$ with gate inductance

Figure 28. Amplitude Spectrum of Sensed current

Figure 28 shows the spectrum of the corresponding sensed current at the output of the current sensor. When the input match frequency reduces, the frequencies that are slightly lower than the match frequency get amplified much more than the frequencies which are slightly higher. This is reflected in the spectrum of the sensed current. Since higher frequencies are not amplified as much as the lower frequencies their relative amplitude
stays more or less the same, as indicated by the crowding of the curves at higher frequencies. In practice, the shift in the match can be detected by measuring the relative change in the amplitude of the sensed current at frequencies lower and higher than the match. The second fault involved an error in the gate source capacitance $C_{GS}$ of the input transistor or the LNA due to process variations. As seen in Figure 29, the input match shifts to the right as the capacitance decreases from 311fF to 111fF.

![Graph showing variation of S11 with Cgs](image)

**Fig. 29. Variation of S11 with Cgs**

Figure 30 shows the output spectrum of the sensed current. As seen in Figure 30, the shift in the match towards higher frequencies is seen as the crowding of the curves towards lower frequencies, since now lower frequencies get amplified less.
The third type of fault which most common in RF circuits is the degradation of the Q of the on-chip inductor. In this case we increase the parasitic resistance of the gate inductor from 0 to 8 ohms. Figure 31 shows the corresponding degradation in input match. Figure 32 shows the spectrum of the corresponding sensed current. Since there is no shift in the match frequency, there will be no crowding of curves at the adjoining frequencies.
Fig. 32. Spectrum of sensed current

Therefore the change in gate parasitic resistance will only cause a change in the magnitude of current spectrum without any shift in balance. Since the LNA is a cascode structure with a finite coupling between the output side and input side, the sensor will also be able to estimate parameters in the output side such as gain and output match. To demonstrate this we vary the voltage across a varactor at the output side of the LNA to perturb the output match as shown in Figure 33.

Fig. 33. Variation of S22 with varactor voltage
As seen in Figure 34, the variation in both the amplitude and frequency of match are sensed accurately in the output current spectrum. Since the shift in frequency is very large and is accompanied by large variations in amplitude, one can actually see the shift in the balance clearly accompanied by the familiar crowding of the curves on one side.

4.3.2 Sensing VCO performance

The tail current in the VCO has a large 2f component to it. Therefore, the current sensor actually measures twice the VCO frequency of oscillation. By looking at this component of the sensor output it is possible to determine, firstly if the VCO is actually achieving oscillations and also whether these oscillations are error free. This is possible because one can infer both the magnitude and frequency of oscillation of the VCO from the sensed current spectrum. A major source of errors in the VCO is the on-chip inductor. Even a small variation in this inductor can significantly affect the VCO performance. The first fault that we introduce is to degrade the Q of the on-chip inductor by varying the
parasitic resistance from 2 ohms to 6 ohms. This degrades the amplitude of oscillation achieved. Figure 35 shows the output spectrum of the sensed current.

![Figure 35. Sensed Output current spectrum for variation in parasitic resistance of on chip inductor](image)

As seen in Figure 35, the maximum frequency component exists at 4.4GHz which is twice the oscillation frequency. As the parasitic resistance increases, the amplitude of the 2f components drops. This drop in amplitude can be used to quantify the degradation in the amplitude of oscillation. The second fault that we introduce is to an error between the actual value and the design value of the inductor. Therefore the value of the inductor is varied from 1.8nH to 2.2nH. Figure 36 shows the spectrum of the sensed current.
Fig. 36. Sensed Output current spectrum for variation in value of on chip inductor

As seen in Figure 36, now there is a shift in the 2f frequency component corresponding to a shift in the fundamental frequency of oscillation of the VCO. By measuring the magnitude of this shift, the change in the actual oscillation frequency can be measured.

4.3.3. Sensing Mixer Performance

Two faults are introduced on the LO side to demonstrate the effectiveness of the current sensor. The sensor essentially measures and quantifies the strength and frequency of the local oscillator signal entering the mixer. This can be used to infer that there are no soft faults on the path from the VCO to the LO input of the mixer. We first vary the frequency of the LO input from 2.2 GHz to 2.6GHz around the actual desired LO frequency of 2.4GHz. This could happen due to the presence of inductive or capacitive parasitics in the LO path to the mixer. Figure 37 shows the output spectrum of the sensed current. As seen in Figure 37, the strongest frequency component at the output is the LO
component. The changes in input LO frequency, are detected by the current sensor, and can be seen as changes in the frequency of the largest component. Secondly, we vary the amplitude of the LO signal entering the mixer from 300m to 1.1V. The LO magnitude entering the mixer can be attenuated due to improper termination or attenuation of the signal due to resistive parasitics. Figure 38 shows corresponding variations in the spectrum of the sensed current. As seen in Figure 38, there is no variation in the frequency of the sensed current, however the change in LO amplitude is detected and reflected in changes in the amplitude of the largest component in the sensed current spectrum. The input match in the RF path can be sensed in exactly the same way that is sensed in the LNA as demonstrated in Section 4.3.1. The current sensor is also fairly sensitive to the amplitude of the RF signal coming in to the mixer which can be used to estimate the gain and output match provided by the low noise amplifier.

![Fig.37. Spectrum of sensed current with LO frequency variation](image-url)
4.4. Post-Processing Circuitry and Test Techniques for LNAs

4.4.1. Low overhead post-processing circuitry for self-test of LNAs.

Having extracted the current information from the LNA in a minimally intrusive manner, the final step is to convert this high frequency information into an easily accessible form. In order to achieve this, we use the BiST architecture shown in Figure 39.
The return current drawn by the CUT (which is the same as supply current) is tapped off using a small sensing resistor $R_S$ (7 ohm) connected at the source of the LNA. As explained in detail in subsection 4.2.1 this technique is a minimally intrusive method of extracting current information from the CUT. Although the input match of the LNA will degrade in the presence of the resistor (in addition to a slight degradation in noise figure and dynamic range), it is possible to co-design the LNA taking into account the value of the resistor in the equation of the input match, thereby eliminating this effect. The resistor value is an optimal solution for the trade-off between reducing the degradation of noise figure and dynamic range of the LNA on one side and achieving sufficient sensitivity to be able to adequately detect variations in the LNA specifications.

The voltage across this resistor is then applied to a source follower that isolates the LNA from the rest of the BiST circuitry. As shall be described in the succeeding sections, it is the peak-to-peak amplitude of this voltage that will contain LNA performance information and hence we need to convert this RF voltage into D.C. Consequently, any amplification of the voltage signal mentioned above, need not be noise-free or low-noise. This allows one to use low overhead amplifiers to carry out the
required amplification, such as the current monitor described in section 4.1, or even a cascade of common source stages with resistive biases. In Figure 39, the source follower and current monitor together constitute the sense amplifier (SA). Further, the amplitude of the test signal can be considerably higher than the typical input signal amplitudes to the LNA, within the limits of its linearity and dynamic range. This in turn brings down the amplification needs of the sensing amplifier. This signal is then input to a peak detector which outputs a DC signal in proportion to the functional specification of the LNA that is being measured. The CUT is excited by test inputs that can be generated on-chip, designed such that the variation in the required LNA specification is captured as variations in current amplitude.

A standard half-wave diode voltage doubler has been designed to peak detect the sense-amplifier’s output. The diodes are current-biased in the linear region for the range of its input signals. Since the P.D output has to be stored on multiple capacitors, the output capacitor is replicated a number of times, which are connected to N1 through transmission gates. This eliminates the need to external memory capacitors. The ratio of input and output capacitance values was chosen to be 5:3 to ensure optimum charge transfer.

Fig.40. Half-wave inverting diode Peak detector
The peak detector was extremely robust across process, supply and temperature. The drift in diode characteristics will not affect the testing process, since all the signals pass through the same PD. The diode area is a trade-off between on-resistance and capacitive parasitics. The outputs of the PD are fed to standard OPAMP based subtractors through unity gain buffers.

Due to the presence of the buffers, the peak detector capacitors have no discharge path thereby retaining most of the charge except for leakage. A separate discharge path is provided to ground through transmission gate switches. Figure 41 shows the simulated charge leakage across the capacitor for times in the order of expected test times.

![Fig.41. Charge leakage is negligible due to the presence of buffers](image)

Since all the voltages being processed by the opamps are extremely low frequency, a standard folded cascode opamp has been used to implement both the buffer and subtractor operations. Figure 42 shows a schematic of the opamp. The folded cascode configuration is chosen because of its high output impedance, high gain and high output swing for the given process. The opamp is biased using a wide-swing current mirror with an external 1V bias. The opamp was designed to have a gain>1000, power consumption<1mW and was compensated using a 7pF on-chip capacitor. The gain of the
subtractors can be designed depending on the resolution and full scale testing range required by the application. The gain is implemented using resistive feedback. Since the gain is dependant on the ratio of resistors, it is not subject to very high variations.

![Folded-cascode op-amp connected as a unity-gain amplifier with current mirror bias.](image)

4.4.2. Self-Test technique for input match \((S_{11})\)- Theory

The input match frequency of the LNA can be shifted due to process faults or parasitic inductances at its input node. This variation in the input match can be reflected in terms of change in the match frequency as well as magnitude. Both these kinds of variations can cause failures in the LNA. The technique used to quantify the input match, must be able to capture both these effects accurately. This section presents a novel approach termed as the three tonal approach that can be used to accurately quantify the match in any RF section.
Fig. 43. Three tonal Approach

At a given frequency, the current in the LNA and hence the sensed voltage varies monotonically as the S\textsubscript{11} (input match) frequency is increased or decreased. Three frequencies are chosen as test frequencies to be applied to the LNA. Two frequencies, one on either side of the designed input match frequency are chosen (shown in figure 43 as Tone 1 and Tone 2) such that the S\textsubscript{11} variation lies within their bounds. The third tone is chosen to be the desired match frequency. The peak to peak value of the current response to this tone is a direct indication of the magnitude of input match (fig. 43 (c)). Two test signals corresponding to the first two tones are applied to the LNA one after the other. Decreasing the input matched frequency results in the peak-to-peak amplitude of the sensed voltage increasing for the first tone (V\textsubscript{tone1}, as depicted in fig. 43 (b)) and decreasing for the second tone (V\textsubscript{tone2}, as depicted in fig. 43 (b)). The difference between V\textsubscript{tone1} and V\textsubscript{tone2} provides a measure of the shift in S\textsubscript{11}. The outputs of the peak detector for Tone 1 and Tone 2 are stored on the two peak detector output capacitors. These voltages are then fed to a subtractor through unity gain buffers. The output of a subtractor is a DC voltage which when compared with the corresponding value for the fault free LNA indicates the magnitude and direction of shift in the match frequency from ideal.
The third test signal corresponding to the third tone is then applied. Output of the peak detector for this tone is stored on a single capacitor and compared with an ideal value yielding the magnitude of the input match. The current information contained in the responses to all three tones is down converted to DC using the peak detector described in preceding sections. Therefore, all comparisons are carried out in DC, resulting in extremely low overhead post-processing circuitry such as low frequency subtractors and comparators. Since all three tones are passed through the same sensing and peak detector, the technique is fairly insensitive to process variations, temperature and power supply variations. The input match frequency, as described above, is ascertained by quantifying the difference between responses to two tones. This differential method of ascertaining input match frequency renders the technique immune, for example, even to a 50% variation in the gain of subsequent amplifying circuitry, tolerances in the sensing resistor value or the precision of the input test signal itself. Since all three test tones are frequencies around the operating frequency of the front-end, (namely the frequency of input match for the LNA) they can be easily generated by using the on-chip VCO, which is part of the RF front-end.

4.4.3 Self-Test for input match – Simulation Results

It is important to note that the three-tonal approach will work successfully irrespective of the absolute gain of the BiST circuitry. However, it is necessary to ensure that the spectral response of the BiST circuitry is monotonic and predictable over process, supply and temperature.
Fig. 44. Spectral Response of Sensor Chain over process temperature and voltage corners. Strongest corner is simulated for temp=10°C and Vdd+4%. Weakest corner is simulated for temp=50°C and Vdd-4%.

As seen from the figure, although the magnitude of the spectrum varies over the corners, the shape of the curve remains monotonic which is sufficient to ensure that the success of the self-test scheme.

If the inductance of the gate coil varies over approximately 25% of its designed value (7.5nH) from 6nH to 9.4nH, the corresponding shift in input match frequency is shown in figure 45(a)
Fig. 45. (a) Variation in $S_{11}$ with 25% variation in $L_G$; (b) BiST output for first two tones test $i/p$; (c) BiST output for third tone test $i/p$.

The first two tones described in section 4.1 of magnitude 130mV pp are applied to the LNA. Figure 45(b) shows the corresponding DC output of the subtractor SB1 in Figure 39. This is the output of the BiST for the first two tones. As seen in figure the output voltage varies monotonically with change in frequency. The output voltage corresponding to the desired match is 1.010V. The difference of the BiST voltage from this value indicates the magnitude and direction of the shift in match frequency (corresponding to change in gate inductance as shown in figure 45(b)). Then the third tone is applied to the LNA with the same magnitude (130mV pp). The output of the third
tone shown in figure 45(c) indicates the variation in the magnitude of the match. As seen in the figure, the slight variations in magnitude of match shown in figure are also captured. However, it is readily apparent that the fault has predominantly caused a change in the match frequency. If desired, this output can be converted to a digital word using a low precision ADC. Another possible fault that may cause a variation in the input match frequency is any process variation that affects the input transistor.

\[ S_{\text{Parameter Response}} \]

![Graph showing S-parameter response with variations in different capacitances.](image)

(a)

\[ \text{Fig.46. (a) Variation in } S_{11} \text{ with 33\% variation in } C_{GS} \text{ (b) BiST output for first two}

\text{tones test i/ps; (c) BiST output for third tone test i/p.} \]

(b) (c)
Figure 46 shows the variation in input match frequency due to 33% change in the gate source capacitance of the input FET (46(a)) and the corresponding output of the BiST for the first two tones (46(b)) and the third tone (46(c)). As seen from figure, the output of the BiST successfully tracks the variation in the match frequency for two very diverse faults. Therefore the self-test approach is not restricted to a class of faults since the input match frequency is being quantified directly. This approach inherently yields very high fault coverage. Now let us consider a case where the Q of the gate coil varies due to variation in the parasitic resistance of the gate coil.

**Fig. 47.** Variation in $S_{11}$ with variation in parasitic resistance of $L_G$ (b) BiST output for first two tones test i/p; (c) BiST output for third tone test i/p.
Figure 47 (a) shows the variation in input match due to variation in gate coil Q. As seen from figure, there is no significant change in the frequency of match, but the magnitude of match varies significantly. Figure 47 shows the output of the BiST for the first two tones (47(b)) as well as the third tone (47(c)). Here we can see that the variations in the magnitude of the match are captured along with the slight variation in the frequency as well. Again, it is apparent to the test engineer that there has been a predominant change in the magnitude of the match without significant change in frequency. Therefore, faults in the input side that vary the magnitude of the match can also be successfully detected. The test time is dictated by the time required by the base band circuitry to settle down to a steady value corresponding to the peak value of the sensed signal. In general, the limiting factor for this time is the slew rate of the base-band circuitry, since the peak detector and sense amplifier have nanosecond response times. The worst case time taken to process a single tone in the given process is 1.5us. So the total test time for the entire three tone approach is measured to be 4.5us.

4.4.4. Self-Test for Gain and output Match – Theory

A traditional cascode LNA is designed to have very little coupling between the input and output side. Therefore any fault in the output side will not be reflected strongly on the input side of the LNA and therefore on the current through the sensing resistor at the source. However, the LNA will usually feed a mixer either directly or through a filter. If the same test scheme is applied at the RF input of the mixer, this can be used to quantify faults in the output side of the LNA in addition to faults on the input side of the mixer. The three tone technique described previously can be used again for this purpose.
An alternative manner of viewing the three tone technique, described previously, is that it enables one to essentially quantify the magnitude and frequency of the signal entering the gate of the FET through the preceding circuitry. Therefore, by quantifying the magnitude of the signal entering the mixer it is possible to test for faults that affect the gain and output match of the LNA. Figure 48 shows a schematic of the proposed technique. It may be argued that it is not possible to use this technique to distinguish between faults in the input match of the mixer and output of the LNA. However, if the LNA is connected directly to the mixer, a fault on the output side of the LNA has the same effect on overall performance as a fault on the input side of the mixer. As stated earlier, this method quantifies the overall variation in the RF front-end performance without regard for the actual location of the fault.

*Fig.48. Self-Test for gain and output match at mixer*
For example, the signal coming into the RF input of the mixer at the frequency of the mixer may be attenuated either due to change in the LNA gain due to degradation of the Q in the drain coil or variation in the mixer input match due to degradation of Q of the gate coil. However, the effect of both these faults with respect to the magnitude of signal entering the mixer will be the same. Hence, although this BiST technique does not provide fault localization, it quantifies the effect of any of these faults on the performance metric of the circuit under test. Therefore, this approach is an effective means of self-test for faults on the output side of the LNA that will impact the gain and output match. Since this is essentially the same three tone approach as described above, this test is also fairly robust and insensitive to variations in process and temperature and requires similarly generated test inputs of moderate precision applied to the input of the LNA.

4.4.5. Self-Test for gain and output match – Simulation Results

If the resonant frequency of the output side varies due to 30% variation in the drain inductance, output resonance frequency will vary as shown in figure 49(a). The output represents both the frequency of maximum gain as well as the frequency of optimal match. Therefore this fault is reflected in both the gain as well as output match.
Let us consider that the LNA is connected to a standard single balanced mixer (RF = 1.9GHz, LO = 1.95 GHz) through a matching network. Since the technique uses the same BiST to quantify performance across the entire front-end, the mixer is also designed with the sensing resistor at its source. Now the three tones are applied as before, to the input of the LNA, and the output of the BiST is observed at the source end of the single balanced mixer. The output of the subtractor SB1 representing the response to the first two tones, indicates the degree of variation in the output resonant frequency (49(b)). Similarly, if the gain of the LNA degrades due to variation in the parasitic resistance of the drain coil as shown in Figure 50. This degradation is also captured at the output of the BiST in the response of the circuit to the third tone as shown in Figure 60(b).
Since the same three tone approach is used to test gain and output match as well, the test time for the output side is also 4.5 us.

4.4.6. Self-Test for Linearity – Theory

The linearity of an LNA is critical in determining its ability to reject intermodulation products. The self-test for linearity quantifies the linear behavior of the
voltage transfer characteristic of the LNA, thereby presenting a quantitative measure of its linearity. This result can then easily be used to extract traditional specifications such as the 1dB compression point.

![Graph showing voltage transfer characteristic of LNA](image)

**Fig. 51. Self-Test Methodology for Linearity**

Consider the transfer characteristic of the LNA shown in Figure 51. Now if two test inputs ($V_{IN\ 1}$ and $V_{IN\ 2}$ in figure 51) are applied to the LNA at its frequency of operation, with a fixed difference between their amplitudes, then the differences between the current responses of the LNA to the two inputs will be proportional to the slope of the transfer curve. ($V_{OUT\ 1}$ and $V_{OUT\ 2}$) The current responses are peak detected using the scheme described in preceding sections and a difference voltage is generated. Now a second set of inputs with the same difference between them ($V_{IN\ 3}$ and $V_{IN\ 4}$) are applied to the LNA about a point B which is the maximum input voltage where it is still desirable for the LNA to be linear. If the BiST circuitry is linear over the entire input range, then the difference between the corresponding outputs ($V_{OUT\ 4}$ - $V_{OUT\ 3}$) will be nearly same as
the difference in the first case ($V_{OUT \, 2} - V_{OUT \, 1}$). However, if the linearity of the LNA has deteriorated beyond its desired specification as shown by the dotted curve in Figure 51, the difference between the outputs will be much lower ($V_{OUT \, TEST \, 4} - V_{OUT \, TEST \, 3}$). If the gain of the LNA has been quantified using the self-test technique previously described, it is possible to precisely calculate the change in slope of the transfer curve. Even if the gain test has not been executed, this method will still provide a pass-fail test for linearity. In other words, if the change in slope is greater than a particular percentage, the linearity has degraded beyond the specification defined for the given application. As in the case of the previous tests, the technique quantifies the actual change in linearity independent of its cause. Again, since the technique uses two inputs and a differential scheme, it is independent of actual numerical value of gain, resistor tolerance etc.

4.4.7. Self-Test for Linearity – Simulation Results

![Fig.52. Transfer characteristic of LNA compared with ideal characteristic](image)

(a) Designed LNA  
(b) LNA under test

Figure 52(a) shows the transfer characteristic of the designed 1.9 GHz cascade LNA in comparison with the ideal transfer curve. Two inputs ($V_{IN \, 1} = 20 \text{mV}$ and $V_{IN \, 2} = 50 \text{mV}$) with a difference of 30mV are first fed into the LNA. The difference between the corresponding outputs represents the slope in the linear condition as shown in Table 2.
(Slope 1). Then, two other inputs \((V_{IN3} \text{ and } V_{IN4})\) are applied to the LNA such that they bound the maximum expected point of linearity on the transfer curve. Now, the difference between the output responses for these two frequencies indicates the worst case degraded slope that is acceptable for the given application. The difference between the two slopes indicates the degree of non-linearity in the circuit. Now let the linearity of the LNA vary due to a fault in the drain inductor. Figure 52(b) shows the new transfer curve of the LNA. If the same set of inputs is applied to the LNA under test and the change in slope is calculated as described above. This change in slope indicates the extent of degradation in linearity as shown in Table 2.

<table>
<thead>
<tr>
<th>Circuit under consideration</th>
<th>(V_{OUT1} V_{IN1}=20) mV (mV)</th>
<th>(V_{OUT2} V_{IN2}=50) mV (mV)</th>
<th>(V_{OUT3} V_{IN3}=180) mV (mV)</th>
<th>(V_{OUT4} V_{IN4}=210) mV (mV)</th>
<th>Slope1 (\alpha) ((V_{OUT2} V_{OUT1}))</th>
<th>Slope2 (\alpha) ((V_{OUT4} V_{OUT3}))</th>
<th>Non Linearity (\alpha) (Slope1 – Slope 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Designed LNA</td>
<td>104.485</td>
<td>250.199</td>
<td>900.502</td>
<td>1039.57</td>
<td>145.714</td>
<td>139.06</td>
<td>6.649</td>
</tr>
<tr>
<td>LNA under Test</td>
<td>86.3128</td>
<td>213.073</td>
<td>723.057</td>
<td>830.152</td>
<td>126.76</td>
<td>107.09</td>
<td>19.66 (5)</td>
</tr>
</tbody>
</table>

**Table 2. Output of Linearity BiST for various test inputs**

Since the degradation in slope is much more in the LNA under test than the designed one, the test engineer may decide that the linearity is unacceptable depending upon the degree of linearity required for the application. Since 4 tones need to be used, the test time for the linearity test is 6us.
4.5. Post-Processing Circuitry and Techniques for VCOs.

4.5.1. Post-processing circuitry for VCOs

As described in subsection 4.2.2, there are two possible interface points for post-processing circuitry with a standard VCO. To preserve the generality of the self-test approach and enable reuse of self-test circuitry, we adopt the approach of placing a resistor in the return path of the VCO. The resultant architecture of the VCO BiST is shown in Figure 53.

![Fig. 53. BiST Architecture for Self-Test of VCO](image)

The first feature that becomes readily apparent from Figure 53 is that most of the circuitry in the VCO BiST architecture has already been implemented in the BiST scheme for LNAs described in Section 4.4 (Figure 39). In fact, the entire chain comprising of the SA, the peak detector, capacitors, buffers and subtractors is common to both architectures. This is a greatest advantage of the current-based technique, since it allows the use of the same BiST chain, to test all the major circuits in the RF front-end. In
addition to providing a very elegant implementation, this dramatically reduces real-estate and power overheads associated with the BiST. Since the same chain is being used, the implementation of the various sub-circuits such as the peak detector, buffers and subtractors are the same as described in section 4.4. The \( V_{\text{CALIBRATE}} \) is an external calibrate signal that is used to calibrate for the gain of the sensor chain. This de-embeds the effect of variations in the sensor chain gain due to supply, temperature and process, giving a BiST output that is solely dependant on the performance of the VCO. Since the VCO may be used to generate test inputs for self-testing the rest of the front-end, it is necessary to ensure the absolute magnitude of its oscillations to a moderate degree of precision. This is why the \( V_{\text{CALIBRATE}} \) signal has been incorporated only into the VCO BiST architecture. The only additional block in the VCO BiST is the CML/Static CMOS counter. This is a standard 8 bit counter implemented using CML and Static CMOS Logic. Figure 54 shows a block diagram of the counter.

\[\text{Fig. 54. Block Diagram of CML/Static CMOS Counter}\]

The size of the counter is a trade-off between the overheads associated with the counter and the maximum achievable resolution. In the current implementation, we have
designed a 1.2 GHz RF VCO. Therefore the fundamental frequency of the sensed signal is 2.4GHz (2f). In the IBM 0.25 micron, the maximum frequency that can be successfully sampled by a static CMOS D-FF is approximately 800MHz. Due to this the first two flip-flop stages are implemented in current-mode logic. Figure 55 shows the schematic of the CML D latch, which is a standard CML latch topology [36].

![Schematic of typical CML D-Latch](image)

**Fig.55. Schematic of typical CML D-Latch**

The larger the transistors M3 and M4 are, greater is the cross-coupling action, however correspondingly larger is the capacitance at the output node. Similarly increasing the sizes of M1 and M2 also improves the transconductance and hence the switching efficiency of the differential pair. But increasing their sizes also increases the capacitance at the output node. Ultimately, increasing the sizes of the cross-coupling pair as well as the differential pair only improves the speed of the latch up to a point. Beyond this, the
only method of improving switching time is to increase the bias current of the circuit. Therefore, in the final analysis the design of the CML latch trades-off speed of switching with static power consumption. CML buffers, such as the one in Figure 56, were used between intermediate latch stages of a flip flop to ensure stable input levels. Two CML latches were used to construct a single edge triggered flip-flop.

![Image](image.png)

**Fig. 56. Standard CML Buffer [37]**

The largest frequency that could be counted using the CML topology of Figure 55, in the IBM 0.25 micron process was about 3.4GHz. At higher frequencies, more novel topologies, such as those suggested in [37] need to be used. However, these topologies often lead to larger real-estate and power overheads. For the current application involving the self-test of a 1.2GHz VCO, the standard CML flip-flop circuit was found to be sufficient.

Figure 57 shows output waveform for the CML D flip-flop. As seen in figure 57, the rise time for the flop is 97.21ps, which makes it sufficient for signals in the 2-3 GHz frequency range. Although rise time is just one of the factors that determines the
maximum frequency at which the latch can operate, it often offers a good indication of its limitations.

**Fig.57. Typical output wave form of CML D FF**

The CML stages are followed by a CML to static CMOS buffer as shown in figure 58.

**Fig.58. CML to Static CMOS buffer**

Here V1 and V2 are the Q and Qbar outputs of the final CML flip-flop. Therefore, when V1 is high, V2 will be low and vice versa. By proper sizing of the PMOS and NMOS
transistors, it can be ensured that the circuit responds to the voltage levels at the output of the CML latch. Although the circuit in Figure 58 has a high power supply dependence, since the current CML implementation has logic swings of about 1.4V, the scheme can tolerate very large variations in power supply. The output of the buffer is used to drive a standard 6 bit synchronous counter designed in static CMOS. The static CMOS section is used, because CML circuits have a very large power overhead associated with them. Due to this the low frequency bits of the counter are implemented in static CMOS.

4.5.2. Self-Test for Amplitude of VCO oscillations

The amplitude of the VCO output can be affected by a number of factors such as the Q of the tank circuit, the transconductance of the active devices and the DC bias conditions of the VCO. It is important to be able to achieve optimum oscillation amplitude to ensure good sensitivity to AM noise. Also, if the VCO is driving the input to a mixer (which is the case in most front-ends) a VCO input with substandard oscillation can often effect the efficiency of switching and hence the IIP3 or IIP2 of the mixer. For these reasons the amplitude of the VCO oscillations is an important parameter to test for.
Fig. 59. VCO BiST  
a) Variation of VCO amplitude with bias current  
b) Corresponding Output of VCO BiST

\[ \text{Output of VCO BiST} \]
Figure 59 shows the output of the VCO for variations in bias current and the corresponding output of the BiST. It should be noted that the output of the BiST is inverted due to the use of the inverting peak detector. In other words, the lowest BiST output corresponds to the highest VCO amplitude.

**Fig. 60. VCO BiST**

(a) Variation of VCO amplitude with parasitic resistance of tank coil

(b) Output of VCO BiST
Similarly, Figure 60 shows the variation in the VCO amplitude due to variation in the parasitic resistance of the tank circuit coil (Q of the tank coil is varied) and the corresponding BiST output. As expected, the amplitude of oscillation degrades with the increase in parasitic resistance and the BiST output correspondingly increases.

4.5.3. Self-Test for VCO frequency

The simple and elegant technique is used to quantify the frequency of the VCO. The technique uses a CML/Static CMOS counter to simply count the number of current pulses in the VCO (which are available at the output of the current monitor). To explain this method let us consider a hypothetical VCO designed to oscillate at 1GHz. Therefore the fundamental frequency of the current pulse signal will be 2GHz (2f). We have designed an 8 bit CML/Static CMOS counter as described in detail in sub-section 4.5.1. The Enable signal shown in Figure 54 is a low frequency control signal that is generated by the external test control. Let us assume that this signal has a frequency of 5MHz, in other words the time duration of the enable is given by

$$T_{enable} = \frac{1}{2 \times 5 \times 10^6} = 100\text{ns}$$

If we assume the enable signal to be synchronized with the clock, the number of VCO current pulses that will be counted in this duration is given by

$$Count = 2 \times 10^9 \times 100 \times 10^{-9} = 200$$
Therefore when the Enable signal goes low, the counter should read the binary equivalent of 200 counts. Now suppose the counter instead reads 204 counts. This means that the actual VCO frequency is given by

\[ F_{\text{actual}} = \frac{204}{2 \times 100 \times 10^{-9}} = 1.02 \text{GHz} \]

Note the factor of 2 in the denominator, since VCO frequency is actually half the counted frequency. Therefore the resolution of this counting technique is given by

\[ \text{Resolution} = \frac{1}{2 \times 100 \times 10^{-9}} = 5 \text{MHz} \]

Which is expected, since this the time window for the counting process. The resolution can be increased by increasing the number of bits of the counter, allowing a smaller timing window to be used. After including time for counter reset and clear sequences, the entire self-test process for frequency can still be completed in less than 200ns. In situations where it is not possible to synchronize the Enable signal with the VCO pulses, the test may have to be performed several times to eliminate errors due to a fixed phase difference between the VCO signal and the Enable signal. Although, the VCO will suffer from jitter, this is seldom large enough to cause the VCO to slip an entire cycle. In such a situation, the final counter value may differ by 1 unit in successive tests. In most cases the VCO jitter, will be well below the time duration of half a VCO cycle. Therefore VCO phase noise will usually not affect the self-test mechanism.
4.6. Post-Processing Circuitry and Techniques for Mixers

4.6.1. Post processing circuitry for Mixers

The post processing circuitry for mixers is simply a combination of the schemes used for the LNA and the VCO. Figure 61 shows the BiST architecture for a single balanced mixer.

As discussed in sub-section 4.2.3, there are two test interface points for the single balanced mixer. The first interface point is in series with the source degeneration inductor of the RF stage. This is exactly the same structure, as the input section of a cascode LNA. Therefore, the same post-processing techniques that have been demonstrated for the LNA in section 4.2 can be applied to this case. The second interface point is in the LO path leading into the oscillator. Here the circuitry associated with the self-test of the VCO can be used to completely quantify the magnitude and frequency of the LO signal entering the mixer. Although Figure 61, shows two separate sets of amplitude detection circuitry for
the RF and LO paths, it is readily apparent that the same circuit blocks are actually being used in both chains. In reality, the same sensor chain will be used for both functions by implementing a switching matrix that will first switch in turn from between the RF and LO section. Additionally, the same counter that is used to self-test for VCO frequency, will be used to quantify the frequency of the LO signal entering the mixer. Although, the output of the VCO has already been quantified, a separate self-test has been implemented for the LO signal. This is because the performance of the mixer is very sensitive to the quality of the LO signal, which in turn determines the efficiency with which the mixer switches the RF signal (which in turn influences the conversion gain of the mixer).

4.6.2. Self-Test at RF stage of mixer

Since the RF input stage of the single balanced mixer is very similar in topology to the input stage of a cascode LNA, the “three-tonal approach” described in sub-section 4.4.2 can be used to accurately quantify the match at the RF input of the mixer. Figure 62 (a) shows the variation in the input match of the RF section due to a 25% variation in the coil at the RF transistor gate. Figure 62(b) and 62(c) show the corresponding outputs of the three tones. It can be seen that difference between the first two tones captures the monotonic decrease in match frequency, while the third tone captures the minor change in magnitude of RF match.
Fig. 62. Three Tonal Approach applied to mixer RF stage (a) Variation in match of RF input with variation in gate inductance, (b) Output of BiST for first two tones, (c) Output of BiST for third tone

It is also extremely important for the RF trans-conductance stage to be linear to ensure good overall linearity in the mixer. The linearity of the trans-conductance stage can also be accurately quantified by using the self-test for linearity described in subsection 4.4.6 (for determining LNA gain compression).
4.6.3. Self-Test at LO input of mixer

The LO signal is tested for both its magnitude and frequency. The magnitude of the LO signal entering the mixer often gets attenuated due to parasitics on its way from the VCO. This leads to less than optimal switching in the mixer. As shown in Figure 61, a termination resistor is used to terminate the LO side at 50 ohms. If this resistor is implemented on-chip, tolerances in its value can often cause attenuation in the LO amplitude entering the VCO. Figure 63 shows the variation of LO amplitude with variations in the termination resistor. Figure 64 shows the corresponding output of the mixer BiST. Therefore, the attenuation of the LO signal is promptly reflected as a variation in the DC output of the BiST. This output can be therefore used to self-test for the amplitude of the LO signal entering the mixer.

![Fig. 63. Attenuation in LO input with variation in termination resistance](image)

Fig. 63. Attenuation in LO input with variation in termination resistance
The frequency of the LO signal can also be quantified accurately using the CML/Static CMOS counter described in sub-section 4.5.3. However here the frequency counted is the actual frequency and not 2f as in the case of the VCO. This reduces the overheads associated with the counter, since fewer CML stages need to be reduced. Another way of looking at this is that if the same counter that was used for the self-test of the VCO is now used to quantify the LO signal, it can do so with half the resolution.

4.7. Use of Source Degeneration for Non-Intrusive BIST (Ls Method)

In the work discussed so far, a resistor has been used as the sensing element, the drop across which is directly proportional to the current in the corresponding circuit branch and serves as the input to the current monitor. The resistor was chosen because it provides a frequency independent, linear relationship between the relevant current information and the input to the current monitor. Although minimally intrusive, (due to its small value) it still affects certain aspects of the RF circuit performance. It contributes
to the noise figure of the RF CUT. In case of the LNA, this contribution could be significant in certain extremely low noise applications. Another drawback is the loss of dynamic range. Finally, the circuit under test needs to be co-designed to account for the additional resistance in the equation for input match. Although these trade-offs are necessary to enhance the testability of the RF CUT in general, the current work offers a better solution for terrestrial RF communication circuits, which often utilize inductive source degeneration. This class of circuits includes the standard cascode LNA, certain types of differential LNAs, the standard single balanced mixer and some double balanced mixers also. Here we propose to use the voltage dropped across the source degeneration inductor ($L_S$) to extract and quantify information about the performance of the CUT. This eliminates the use of a sense resistor and results in a technique that makes the leap from minimal intrusion to true non-intrusion, where the presence of the BiST will have no measurable effect on the performance of the CUT. Figure 65 shows a block diagram of the modified BiST scheme.

**Fig.65. Modified BiST Architecture for Source Degenerated Circuits**

The return current drawn by the CUT (which is the same as supply current) is tapped off from the source degeneration inductor. By using a source follower as the first stage of the sensing process, the CUT is completely isolated, and as the results confirm, the BiST
circuitry does not affect its performance in any measurable way. This is due to the fact that the source follower that connects to the LNA only presents a small capacitance (in the order of tens of femtofarads) across the coil. This capacitance is in the same order of magnitude as the parasitic capacitance associated with the on-chip coil and only affects its self-resonant frequency, which will not impact the performance of the LNA in our frequency range of interest (low GHz).

4.7.1. $L_S$ Method – Theory

In this section we establish the usability of tapping into the source coil instead of using a small valued resistor. In principle, the three tones used for testing occur within a narrow frequency range, and more importantly, since we use discrete single-frequency test stimuli, the inductor can be viewed as a frequency-varying resistance. In order to quantify and verify this concept, we present the voltage drop equations and graphically compare the two methods for a source degenerated cascode LNA. If the input voltage to the LNA is $V_{IN}$ then we have (see Figure 66)

$$V_{IN} = i \frac{g_m L_S}{C_{GS}} + i \left[ j \omega (L_S + L_G) + \frac{1}{j \omega C_{GS}} \right] + i R_S + i \frac{g_m R_S}{j \omega C_{GS}}$$

$$i = \frac{V_{IN}}{V_{IN}} = \frac{\frac{g_m L_S}{C_{GS}} + j \left[ \omega (L_S + L_G) - \frac{1}{\omega C_{GS}} \right] + R_S - j \frac{g_m R_S}{\omega C_{GS}}}{\frac{g_m L_S}{C_{GS}} + j \left[ \omega (L_S + L_G) - \frac{1}{\omega C_{GS}} \right] + R_S - j \frac{g_m R_S}{\omega C_{GS}}}$$
Therefore the voltage across the resistor $R_S$ is given by:

$$V_{gs} = iR_s + \frac{g_m R_s}{j\omega C_{gs}}$$

$$V_{gs} = V_{gs} R_s \left[1 - \frac{jg_m}{\omega C_{gs}}\right]$$

$$\frac{g_m L_s}{C_{gs}} + j\left(\omega(L_s + L_g) - \frac{1}{\omega C_{gs}}\right) + R_s - \frac{jg_m R_s}{\omega C_{gs}}$$

In the absence of the sensing resistor, the voltage across $L_S$ is used, and equation (1) becomes ($L_S$ case):

$$V_{ls} = V_{in} L_s \left[ jw + \frac{g_m}{C_{gs}} \right]$$

$$\frac{g_m L_s}{C_{gs}} + \left(\omega(L_s + L_g) - \frac{1}{\omega C_{gs}}\right)$$

Five instances of a 1.9 GHz cascode LNA were created by varying its input match (using different gate inductors). Figure 67 compares the voltage developed across the sensing resistor with that of the source inductor for these instances. It is evident that, as long as the tone 1 and tone 2 (sec 3) are selected to lie outside of the maximum expected match variation, the $L_S$ approach provides similar HF current information as the $R_S$ approach. The only difference was that this separation (the dotted lines in Figure 67) was marginally higher in the $L_S$ case. In other words, the three-tonal approach can be successfully used in the $L_S$ case but a larger separation between Tone 1 and Tone 2 is required. In this example, the value of $R_S$ was 7 ohms and that of $L_S$ was 0.9 nH, and the voltages developed across them were in the same order of magnitude.
4.7.2. Advantages of $L_S$ method over $R_S$ method

In order to demonstrate the superiority of the $L_S$ method, we consider three situations: a) The standard LNA in the absence of an BIST circuitry b) The LNA interfaced to the BiST circuitry through a sensing resistor $R_S$ c) LNA interfaced to the BiST circuitry by taping the source degeneration inductor $L_S$. Figure 68(b) shows the input return loss ($S_{11}$) for all three cases. It is evident from the figure that the return loss degrades slightly from -38dB to -28dB due to the presence of $R_S$. However, when voltage across $L_S$ is used as the input to the BiST the return loss degrades very marginally from -38dB to -37dB. The other parameter that would be affected due to the presence of the resistor is the noise figure. Figure 68(a) compares the noise figure of the LNA under test in the three cases. As seen in the figure, the noise performance of the LNA is completely unaltered when the $L_S$ technique is used. However, in the presence of $R_S$ the noise figure degrades by 0.2dB.

**Fig.67. Voltage versus frequency across (a) $R_S$ and (b) $L_S$ for 5 different LNAs with input match varying from 1.7GHz to 2.2GHz**
Fig. 68. a) Noise Figure  b) $S_{11}$ for a stand alone LNA (No BiST), LNA with sensing resistor ($R_S$) and proposed LS method ($L_S$)

The dynamic range of the LNA is also unaffected in the $L_S$ method. The gain and output match of the LNA under test are unaffected in both techniques. Therefore, we have achieved self-test with absolutely no-measurable intrusion on the performance of the CUT. This represents the greatest advantage of the proposed technique. The same post-processing circuitry and techniques described in previous sections can be used in conjunction with the inductive sensing element as well.

4.8. Fault Coverage

Fault coverage is an important parameter to validate any testing approach. It not only provides information about the practical applicability of the approach, but also often highlights the bottlenecks to the accuracy of the methodology. Since the current work takes a specification based approach to testing, we define a faulty part as one in which any specification (for example return loss $S_{11}$ of an LNA) is beyond the bounds defined for it during design. These bounds are the minimum and maximum values of the specification within which the circuit can still be considered to function satisfactorily. Therefore fault coverage for a particular test is the ratio of the number of faulty parts
(with out of bound specifications) detected by the BIST to the total number of faulty parts.

To examine fault coverage, we consider the test for input match of a 1.9GHz LNA (the three tonal approach). The input match of the LNA is varied through a combination of various process related parameters by performing a Montecarlo analysis. Figure 69 shows the variation in $S_{11}$ for the 75 sample LNAs generated using the Montecarlo.

![Fig.69. $S_{11}$ curves for various Montecarlo runs](image)

Points A and B are chosen as the two bounds for input match frequency of the LNA. Any LNA with an input match frequency beyond this bound is considered faulty. Here we have only considered the test for change in match frequency. So A & B have been selected by fixing bounds only on the frequency axis (X axis). Figure 70 shows a scatter plot of the BiST output (difference between responses to Tone1 and Tone2) for the various LNAs.
**Fig. 70. Scatter plot of BiST output for various Montecarlo runs**

The dotted lines indicate the two DC voltages corresponding to the BiST output for match frequencies at the two bounds, point A and point B indicated in Figure 69. Any point that is outside these bounds (greater than 762mV of less than 620mV) indicates a faulty part. Any point within these bounds indicates a fault-free part. The fault coverage using in this particular test was found to be 93.33%. The faulty detections occurred for LNAs that had their match frequencies outside the acceptable bounds, but very close to them. This faulty detection occurs due to offsets in the OPAMPS and the minimum resolution of the peak detector (4-6mV). It is possible to improve the fault coverage by using a larger number of test tones (5 or 7 tones). This would improve fault coverage at the cost of more post-processing circuitry and a larger test time. Another method to improve fault coverage is to use OPAMPS with extremely low offsets. It is also possible
to replace the simple diode detector with more sophisticated test techniques such as a synchronous detector. This could improve the resolution of the peak detector as well.

A similar test can be carried out with the test for VCO amplitude. The amplitude of a 2.4GHz VCO is varied by performing a Montecarlo analysis. Figure 71 shows the variation in oscillation amplitude for 125 samples created by the montecarlo.

![Fig. 71. Variations in VCO oscillation amplitude for various Montecarlo runs](image)

A range of optimum amplitudes is chosen for the VCO. An oscillation with amplitude greater than this range may be distorting or hitting the supply rails, and therefore needs to be avoided. An oscillation less than this may be sub-optimum for the circuits being driven by the VCO. It is also possible that in some conditions the oscillation does not start at all. Figure 72 shows a scatter plot of the VCO BiST output.
The threshold values for the optimum oscillation magnitude are set at 800mV and 1000mV. Due to the inverting nature of the peak detector, the values higher than 1000mV are oscillations that are less than desired, while values less than 800mV are oscillations that are higher than desired. The band of values around 1500mV, indicate situations where the VCO was unable to oscillate at all. This can easily serve as a go/no go test to ensure that the VCO is actually oscillating. The fault coverage for the VCO was found to be 98.5%. The higher fault coverage in comparison to the LNA BIST, is due to the fact that only one tone is processed in comparison to two or three in the case of the LNA. This leads to fewer errors, due to OPAMP offsets.

Fig. 72. Scatter plot of VCO BiST output for various Montecarlo runs
CHAPTER 5: EXPERIMENTAL RESULTS

In prior chapters, we have demonstrated both the theory and application of the self-test approach to RF front-end circuits. The impact of the BiST scheme on RF circuit performance and its other associated overheads have been quantified. Finally, the self-test of LNAs, mixers and VCOs for various performance metrics has been demonstrated in simulation. The final step is to verify the functionality of the various proposed circuits and techniques in real silicon. This has been accomplished with the help of two chips fabricated in the IBM 0.25 micron 6 metal layer RF CMOS process.

5.1. Measurement Setup

Since no RF packaging was used on the chips, all the circuits were probed directly on die, using the Cascade Microtech RF-1 probe station shown in Figure 73.

![Cascade RF-1 Probe Station](image)

The other test equipment used during the characterization process were

- Agilent E8362A 2-port Vector network analyzer
- HP 4405B spectrum analyzer
- Agilent 8648D RF signal generator
- Programmable DC supplies and low frequency function generators
Figure 74 shows a block diagram of the measurement setup.

![Fig. 74. Block Diagram of Measurement Setup](image1)

The power to the chip was supplied using a custom made RF power probe, with on-probe by-pass capacitance (470pF), through 12 pads with alternate power and ground as shown in Figure 75.

![Fig. 75. Power Pads](image2)

The RF signals were supplied through standard Ground-Signal-Ground (GSG) pads, while the DC voltages were supplied using single DC pads. The current at the input of the current monitor was injected through a 7 ohm on-chip resistor connected at the input of the circuit and RF (GSG) pads.

### 5.2. Experimental Results for Current Monitor

The sense amplifier was fabricated in IBM, 6 metal layers, 0.25µm RF CMOS process. Figure 76 shows a micrograph of the sense amplifier. The circuit was found to occupy an area of 2760µ². This represents a minimal real estate overhead of less than 0.5% for a standard LNA.
The current gain of the sensor was measured to be 24 dB with a 3dB frequency of 3.9GHz. Figure 77 shows a comparison of the simulated and measured frequency spectrum. The sensor has a slightly lower gain than the simulations shown in Chapter 4, but has a higher 3 dB bandwidth. The measured behavior of the circuit is within the limits predicted by a Monte Carlo simulation of the circuit for process variations and transistor mismatches (see Figure 14, Chapter 4).

With further technology scaling, the authors believe it will be possible to design current sensors that work at even higher frequencies.

Another important aspect is dynamic range of the sensor. As seen in Figure 78, the behavior of the sensor is extremely linear until an input current of 11.5mA. At higher input currents the output distorts and eventually saturates. This puts a practical limit to
the maximum possible sensed input current. However, additional input dynamic range can be obtained simply by reducing the value of the sense resistor R_s. At the lower end, the sensor is extremely sensitive and was measured to be able to sense currents as low as -50dbm (45.1uA). The sensor also has an extremely robust power supply rejection of -55.08 dB. The power consumption of the sensor is 7.5mW at 1.7GHz. This represents 15% of the power consumed by a standard LNA. However, in the final BIST architecture the same current sensor will be used for the entire RF front end. In this light, the power consumption represents a very small fraction and a reasonable trade-off to achieve vastly enhanced testability and reliability in the front-end.

![Fig. 78. Dynamic Range of Current sensor](image)

5.3. Impact of the Sensing Circuitry on LNA Performance

In order to establish that the return current path is indeed the point of least intrusion for the LNA, it is necessary to examine the actual effect of the current monitor on an LNA in silicon.
To do this two test LNAs were fabricated on the same die with and without the sense amplifier. Figure 79 shows a chip-micrograph of an LNA without the sense amplifier, and Figure 80 shows the corresponding $S_{11}$ measured using the setup described in Figure 67. The minimum $S_{11}$ frequency as measured using the VNA is 1.75GHz.
Figure 81 shows the corresponding input match in simulation. As seen from these measurements, the input match of the LNA is very close to the value predicted in simulation.

*Fig.81. S11 of LNA – Simulation*

Figure 82 shows the chip-micrograph of the LNA interfaced with a sense amplifier. As indicated by the micro-graph, the sense amplifier presents a minimal real estate overhead to the LNA under test. This is one of the key advantages of the current work over more traditional trans-conductance amplifiers which usually present much higher real-estate

*Fig.82. Micrograph of Sense Amplifier interfaced with LNA*
overheads. Figure 83 shows the measured input return loss in this case. As seen in figure, the input return loss has degraded in a similar manner to that predicted by the theory and simulations in section 4.2. The match frequency has also shifted to 1.82GHz. However as established earlier, this is an acceptable trade-off because it is possible to co-design the RF circuit with the sense amplifier to re-establish a comparable return loss. Even in the absence of co-design, a return loss of -17dB demonstrated in Figure 83 is acceptable for most terrestrial wireless applications.

![Fig.83. Measured S11 for LNA with sense amplifier](image)

5.4. Sensing LNA performance (Verifying the current based approach)

Figure 84 shows a comparison of the amplitude response of the LNA and the sense amplifier together, as predicted by the simulations carried out using Spectre RF and measured data. The figure shows the voltage across the output load resistance of the amplifier for a 100mV input applied to the LNA. Both curves correlate closely and exhibit a similar frequency behavior, although there are some differences in actual magnitude due to process variations. The frequency where the sense amplifier has maximum output has increased slightly in the measured data in comparison with
simulation. The difference between the simulated and measured value is 6.1% of the actual frequency. This is an acceptable change in performance due process variations. The difference in the magnitude of the voltage can be attributed to variation in gain described in Section 4.1.

Fig.84. Output Spectrum of LNA with sensor – Simulated versus Experimental

The input match of the LNA was varied by varying the supply voltage of the circuit by +/- 20%. The nominal supply voltage for the IBM 0.25 micron process is 2.5V.

Fig.85. Variation in return loss (S11) due to change in supply voltage - Simulation vs. Experimental

Experimental
Figure 85 compares the measured variation in the input return loss of the LNA with that predicted by simulation.

Since the measured output of the sense amplifier is the peak to peak current variation, this cannot be attributed to a variation in the DC current of the LNA due to change in supply voltage. A DC blocking capacitor has also been used between the sense amplifier stages to isolate the amplifying cell from any DC related effects in the LNA. Besides, the power supply of the sensor is separate from that of the LNA. Therefore, the variation in the peak to peak output of the sensor must be due to the change in input match of the LNA under test. The above comparisons indicated that the sense amplifier can indeed quantify the variation in LNA parameters, in this case the change in the input return loss.

![Graph showing sensed current output vs frequency]

**Figure 86. Output of the sense amplifier sensing S11 change for 20% variation in supply voltage – Simulation versus Experimental**

5.5. Performance of complete sensor chain

The results in the previous sections have conclusively established the efficacy of the current-based approach to self-test. The next logical step is to combine the sense
amplifier along with post-processing circuitry such as the peak detector into a complete BiST architecture. In order to do this a second chip was designed and fabricated in the IBM 0.25 micron 6 RF process. Figure 87 shows a micrograph of an entire sensor chain comprising of a source follower, sense amplifier, peak detector and buffers.

![Micrograph of entire sensor chain](image)

**Fig.87. Micrograph of entire sensor chain**

The input to the sensor chain is an RF signal while its output is a DC voltage that is indicative of the peak value of the current through a resistive sensing element corresponding to the RF input. The chain is also provided with a discharge signal, to remove any residual charge on the output capacitors of the peak detector. The RF input to the sensor chain was swept from 0 to 800mV, at a frequency of 1.775GHz and the corresponding DC output was measured. Figure 88 shows a scatter plot of the output values. It can be seen that behavior of the sensor chain is extremely linear over the entire range of inputs. The digital control signals, such as the taps and discharge signal were brought out to DC pads, and controlled using DC probes.
Although the gain of the sensor is lower than that predicted by simulation, it is still sufficient to ensure faithful self-test as will be demonstrated by further results. Figure 89 shows a chip-micrograph of the complete sensor chain interfaced with a 1.9GHz LNA.
5.6 Tapped Coil Mechanism

In order to test the ability of the BiST scheme to quantify variations in any LNA parameter, there should be a mechanism that allows one to dynamically alter the LNA performance on-chip. In the current work, this has been accomplished by using a tapped coil mechanism. In order to adaptively move the input match of the LNA, the gate inductor value is made variable by tapping it at several points. The gate coil ($L_g$) is designed for a nominal value and then tapped off at different intervals in its outer-most turn, with each tap leading to a switch. By including the interconnects and switch capacitance in the design process, this coil can be characterized to give accurate inductance values. Based on which switch is turned on, one and only one tap of the coil will be shorted to the input pad of the LNA, and this tap determines the input match of the LNA. The coil was designed in ASITIC (a rudimentary field solver tool). The pi model obtained from ASITIC was simulated in Cadence along with the RF CMOS switches to account for all the parasitics associated with the structure. Figure 90 shows a layout of the tapped coil gate coil and a corresponding micrograph. (it can also been seen in the micrograph in Figure 89). Table 3 shows the various gate inductance values associated with the various taps and the corresponding input match frequencies of the LNA. The presence of the RF switches does degrade the coil Q and increase the noise figure by about 0.8dB. However, this was deemed to be acceptable since the aim of the experiment was to demonstrate the effectiveness of the self-test techniques which would be unaffected by the degradation.
Fig. 90. Tapped Coil a) Layout b) Chip-Micrograph. The dimensions are: radius = 220 µm, width of metal = 5 µm, spacing = 5 µm. It was created on the topmost (Analog metal) layer.

<table>
<thead>
<tr>
<th>Tap no.</th>
<th>Inductance value</th>
<th>Corresponding $S_{11}$ freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7.4 nH</td>
<td>1.7 GHz</td>
</tr>
<tr>
<td>2</td>
<td>8.1 nH</td>
<td>1.8 GHz</td>
</tr>
<tr>
<td>3 (nominal value)</td>
<td>9 nH</td>
<td>1.9 GHz</td>
</tr>
<tr>
<td>4</td>
<td>10 nH</td>
<td>2.0 GHz</td>
</tr>
<tr>
<td>5</td>
<td>11 nH</td>
<td>2.1 GHz</td>
</tr>
</tbody>
</table>

Table 3. The tapped coil values and corresponding $S_{11}$ frequency

5.7. Self-Test for input match of LNA

The LNA that has been used to validate the approach is a standard 1.9GHz cascode LNA. Figure 91 shows the various measured scattering parameters of the LNA. The ripple in the curves occurs because the measurements were carried out in an unshielded environment, hence were subject to various noise sources such as coupling from ac supply sources (60Hz), fluorescent lights etc.
The input match of the LNA is -20.74 dB which is significantly better than the -15dB specification that it was designed to meet. The output match (S22) is also within acceptable limits at -13dB. The LNA was designed to have a power gain of 8dB while the measured gain (S21) is 5dB. It should be noted that the LNA has very moderate specifications, since it was only designed to be a test bed for the BiST approach. Therefore, no attempt was made to optimize the power gain or output match. Two binary control signals were used to switch the taps of the LNA. Table 4 shows the binary signal and a comparison between the corresponding expected match frequency of the LNA and measured match frequency. Figure 92 shows the S11 curves corresponding to the various taps.
<table>
<thead>
<tr>
<th>Binary control (S1S0)</th>
<th>Corresponding $S_{11}$ freq (simulated)</th>
<th>Corresponding $S_{11}$ freq (measured)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>1.72 GHz</td>
<td>1.7375 GHz</td>
</tr>
<tr>
<td>01</td>
<td>1.91 GHz</td>
<td>1.925 GHz</td>
</tr>
<tr>
<td>10</td>
<td>2 GHz</td>
<td>2.03 GHz</td>
</tr>
<tr>
<td>11</td>
<td>2.11 GHz</td>
<td>2.125 GHz</td>
</tr>
</tbody>
</table>

*Table 4. Binary Signal and corresponding match frequency of LNA*

(a)

(b)
Fig. 92. S11 curves for various values of binary control S1S0 a) 00 b) 01 c) 10 d) 11

Having established the change in the behavior of the LNA for various taps, the next step is to now verify if the BiST scheme can detect this change in behavior. For ease of comparison we choose the three taps at 1.7GHz, 1.9GHz and 2.1GHz to validate this. Since we want to measure the variation in S\(_{11}\), the “three-tonal approach” described in
chapter 4 is used. It is also important to note here that the self-test techniques for gain and output match, as well as several of the tests for the mixer also fundamentally use the same three-tonal approach. So this experiment to validate the three-tonal approach also validates all the other post-processing techniques based on this approach.

Tone 1 is set at 1.6GHz, Tone 2 1.2.2GHz and Tone 3 is set at 1.9GHz. Figure 93 shows a comparison of the measured output of the BiST for the first two tones (ie. the output of the subtractor, which is the difference of the responses for the two tones) with that expected in simulation, as a function of input match frequency of the LNA.

![BiST Output for first two tones](image)

**Fig. 93. BiST Output for first two tones, Simulated vs measured**

As seen in the above figure, the measured output of the BiST varies monotonically as predicted by simulation, although there is a DC offset as well as a difference in gain between simulated and measured curves. Figure 94 shows a comparison of the two curves after eliminating the offset.
As predicted by the experimental results of just the sensor chain presented in section 5.5 there is a difference in the gain of the BiST circuitry due to variations in process. However once the gain is determined accurately by means of a calibration input, it is possible to accurately quantify the change in S11 frequency using the DC voltage at the output of the BiST.

Fig.94. BiST output for first two tones, simulated vs. measured (without DC offset)

Fig.95. Measured BiST output for third tone
Similarly the magnitude of S11 can also be quantified using the output of the third tone as shown in Figure 95. (the output of the BiST versus magnitude of LNA return loss in dB). Thus we have successfully demonstrated the use of the three-tonal approach in quantifying the input match of the cascode LNA. These results have also been verified across multiple dies to ensure their reproducibility. Figure 96 shows the response of the BiST circuitry to Tone 1 = 1.6GHz across 4 dies.

![BiST output response for Tone 1 across multiple dies](image)

**Fig.96. BiST output response for Tone 1 across multiple dies**

Thus the values are in close agreement across dies, within limits of measurement related errors. Similarly, Figure 97 shows the BiST output response for Tone 3 across 4 dies. Again the curves are in close agreement adequately demonstrating the reproducibility of the results.
Fig. 97. BiST response for Tone 3 across multiple dies

The data showing the output of the BiST for the three tonal approach was reproducible across dies. This further validates the results of the three-tonal approach eliminating any possible errors specific to a particular measurement setup or a particular die.
CHAPTER 6: CONCLUSIONS

The drive for cheaper and more integrated RF IC products has heralded an age of unprecedented integration in communication circuitry. Coupled with the advent of nanometer CMOS, this has caused most semiconductor companies to move towards RF circuitry, tightly integrated with analog, mixed signal and digital circuitry on a single die. This new design paradigm has brought with it a host of design and manufacturing challenges.

One of the foremost challenges is the efficient and accurate testing of the RF circuitry now embedded in an increasingly complex environment. Due to the challenges associated with testing in the GHz regime, as well as an extensive list of fault mechanisms, test cost in these products can comprise as high as 50% of the total manufacturing cost. Testing times for these integrated RF IC products are also extremely high, leading to very long times to market.

The current work offers a cost-effective, low overhead and completely on-chip solution to this critical problem. The technique achieves self-test of LNAs, mixers and VCOs, with extremely minimal real estate and power overheads, without the use of any complex on-chip or off-chip DSP processing. The entire scheme is minimally intrusive on the circuit-under-test. In certain circuit topologies, the leap has been made from minimal intrusion to non-intrusion. The output of the BIST is a low frequency DC voltage or a digital word that can easily be integrated into existing test scan chain architectures. The work also establishes the efficacy of the specification based testing approach for RF circuits over the structural approach. By moving the emphasis over to
testing for RF circuit performance parameters rather than trying to detect specific failure mechanisms, we have vastly simplified the overall BiST architecture while simultaneously achieving very high fault coverage.

One can also quantify the benefits of the BiST approach presented, by performing a yield versus cost analysis for a typical RF front-end with the BiST. Let us assume a RF front-end cost of $4 per chip for a 5mm$^2$ die. Now if we assumed a standard defect density of 2 defects/mm$^2$, the probability of a faulty chip due to a defect occurring in the BiST (with an area of approximately 4225µm$^2$) is 0.169%. This is the percentage loss in yield due to the presence of the BiST. If we consider a lot size of one million parts. The increase in cost per chip due to this loss in yield is 0.67 cents for a $4 part. The presence of the BiST however reduces test time by four orders of magnitude from approximately 2s [4] to 50µs. By many estimates test cost can consume as high as 40% of manufacturing cost [15]. Even if we conservatively assume that the test cost is 20% of the cost of the chip, this would translate to a test cost of 80 cents for a $4 part. In RF and mixed-signal testing test cost is directly proportional to test time (since equipment cost is considered to be negligible in the long run). With a dramatic reduction in test time on can very conservatively expect a test cost reduction of at least 50%. Therefore test cost per chip would go down to 40 cents. This more than offsets the 0.67 cents increase in part cost due to the loss of yield, leading to a net cost reduction of 39.33 cents per chip, a 9.8% reduction in cost! Therefore the RF BiST solution presented, even under conservative estimates would lead to a significant reduction in cost of the RF part.

The work presented therefore represents the first ever comprehensive, low-cost BiST scheme for integrated RF front-ends.
6.1. Summary of Work presented

The fundamental approach to self-test that has been adopted in this work is to extract RF circuit performance information from the high frequency return current of the circuit-under-test. We have theoretically established the validity of this approach, by deriving the expression for the sensed current in the case of a standard LNA, and examining its sensitivity to soft variations in various circuit parameters. The generalized architecture for the BiST approach involves sensing the high frequency current drawn by the CUT and amplifying it using a current-monitor circuit. Following which, this information is immediately converted into a low frequency DC or digital format for ease of access.

The current monitor is an extremely critical element of the BiST architecture with significant design complexity. This is due to the fact that, it needs to perform significant amplification in the RF domain, while presenting low area and power overheads. All the circuitry succeeding the current monitor will simply convert this sensed information into a low frequency equivalent and post-process that signal, instead of the original RF information. Therefore, the sense amplifier is the only RF processing element in a BiST for RF systems. This is one of the main reasons for the low overheads associated with the over all system.

The current-monitor has been realized in the IBM 0.25 micron process. It demonstrates a high bandwidth of about 3.9GHz, while providing reasonable gain. The circuit is also in itself insensitive to process variations, which is an important criterion for any BiST circuitry. Finally, the sense amplifier is minimally intrusive on the circuit-
under-test which is a significant challenge in the RF domain. Table 5 summarizes the performance metrics of the current monitor.

<table>
<thead>
<tr>
<th>Gain</th>
<th>24dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>3dB</td>
<td>3.9GHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td></td>
</tr>
<tr>
<td>Maximum sensed current</td>
<td>11.5mA</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>45.1uA @2.5V</td>
</tr>
<tr>
<td>Power Supply Rejection</td>
<td>-55.08dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>7.5mW</td>
</tr>
<tr>
<td>Area</td>
<td>2760µ²</td>
</tr>
</tbody>
</table>

**Table 5. Performance Metrics of Current Monitor**

As seen from table 5, the circuit also presents very low real estate and power overheads when taken in the context of an entire RF front-end.

The current monitor is the first block of self-test circuitry that interfaces with any RF CUT. Therefore it is necessary to interface it with the CUT, while minimally intruding on its performance. The return current path was found to be the point of least intrusion for interfacing the current-monitor. The impact of the BiST circuitry on LNA, mixer and VCO performance has also been accurately quantified. In the case of the LNA, the presence of the sensing element does not impact either the gain or the output match. Although, the input match does get affected, it is possible to co-design the LNA with the resistor and get back most of the input match. The only significant impact is a 0.2dB increase in noise figure and a marginal reduction in dynamic range. The presence of the resistor has no major impact on the performance of the VCO. As long as the value of the
sense resistor (7 ohms), is much lower than 1/gm (where gm is the trans-conductance of the active devices in the VCO) the contribution of the sense resistor to the thermal noise is negligible. The presence of the BiST circuitry has no measurable impact on a single balanced mixer as well. Similar to the LNA, the mixer can be co-designed with the resistor to obtain sufficient RF input match. Since noise figure is not as important in the mixer as in the LNA, the degradation in the noise figure is very tolerable. On the local oscillator side, since the sense resistor is placed in the bias circuitry it has no measurable impact on the mixer performance. In commonly used RF circuits for terrestrial communication that have inductive source degeneration, we have also demonstrated the leap from minimal intrusion to complete non-intrusion. By eliminating the need for even a small sensing resistor, the BiST circuitry does not affect the performance of the CUT in any measurable way.

Having successfully interfaced the current monitor with the circuit under test we have also demonstrated a strong co-relation between typical fault mechanisms in front-end circuitry and the sensed current. The impact of various soft variations in passives, process variations, package parasitics as well as hard process faults on circuit performance can be detected and quantified in the sensed high frequency return current.

Various post-processing techniques and circuitry have been developed to extract relevant performance information from the CUT and convert it into the easily accessible form of a DC voltage or digital word. A novel technique known as the “three-tonal approach” has been developed to accurately quantify match and gain in any RF section. The technique is extremely robust and ultra-fast. Since the technique depends on difference between responses to test inputs and not absolute values, it is independent of
absolute gain of the sensing circuitry. A similar differential technique has also been
demonstrated for quantifying linearity. Using these post-processing techniques and
associated circuitry, the self-test of the entire LNA can be carried out in approximately
15µs, which is several orders of magnitude better than anything reported in literature.
Similar tests have been developed for the mixer and VCO that utilize the same post-
processing circuitry, resulting in very low real-estate overheads. The frequency of the
VCO and the LO signal entering the mixer is quantified by using a simple CML/Static
CMOS counter. The self test of the entire VCO (amplitude and frequency) can be
completed in about 2µs, while the self-test of the mixer for RF input match, LO
amplitude and frequency can be carried out in 7µs. Therefore self-test for the entire front-
end can be carried out in less than 30 µs, which is faster than any RF test scheme either in
published literature or industry. Table 6 shows the real estate and power consumption
associated with various front-end implementations in literature.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Technology</th>
<th>Area(mm²)</th>
<th>Power(mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lim [39]</td>
<td>0.35µm CMOS</td>
<td>2</td>
<td>140</td>
</tr>
<tr>
<td>Pfeiffer [40]</td>
<td>0.25 µm CMOS</td>
<td>5.04</td>
<td>73</td>
</tr>
<tr>
<td>Gatta [41]</td>
<td>0.18 µm CMOS</td>
<td>6.8</td>
<td>38</td>
</tr>
<tr>
<td>Rogin [42]</td>
<td>0.13 µm CMOS</td>
<td>3.5</td>
<td>44</td>
</tr>
</tbody>
</table>

*Table 6. Real Estate and Power consumption of standard RF Front-end implementations*

Therefore, the real estate overhead associated with the entire BiST scheme
(4225µm²) is less than 1% of the area associated with the entire front-end. The entire
BiST architecture for the front-end consumes about 10mW which an average of 10% of
the power consumption of the entire front-end (considering scaling associated with the
various implementations). However, the power consumption exists only in test mode,
which lasts for less than 100µs. So this represents a transient power consumption which
translates into a much lower power overhead. The BiST technique was found to have very high fault coverage (about 92% in all cases). Factors affecting the fault coverage have also been analyzed and possible improvements to the circuitry to enable higher fault coverage have also been suggested.

The current-monitor as well as the entire BiST architecture for the LNA has been designed, fabricated and characterized in the IBM 0.25 micron 6 metal layer RF CMOS process. The impact of the current-monitor as well as its ability to detect and quantify change in LNA performance has been verified experimentally. The “three tonal approach” which is at the heart of most of the post-processing techniques used in the current work has also been verified using a test chip in the IBM 0.25 micron process. All the measured data correlates within acceptable limits with simulation results. Additionally, all the silicon data has been verified across multiple dies to ensure repeatability of the techniques.

6.2. Future Work

The current work has demonstrated the realization of a completely on-chip self-test solution for RF front-end circuitry. Although, the techniques and circuits that form the building blocks of the methodology have been verified in silicon, the self-test of an entire integrated front-end has not yet been verified in silicon. In order to do this, it will be necessary to implement a switching matrix that can switch between various circuits-under-test and the BiST block. Each CUT would have its own sensing element along with a source follower, to isolate it from the switching matrix. One can envisage a switching matrix designed using RF transistor switches. The only impact of the switches would be an attenuation of the sense signal, due to the on resistance of the switch. However, this
can be compensated for by increasing the gain of the sense amplifier. The realization of a complete integrated front-end is in itself a challenging task. To implement such an integrated front-end, along with a BIST scheme would be a significant project in itself, and is a future goal.

Although the current work addresses linearity of amplifiers in terms of gain compression, the self-test for second or third order intercepts has not yet been addressed. Although the current-based methodology presented in this work can be used for this approach the main challenge to testing for second or third order intercept is the need for test inputs of two different frequencies applied simultaneously the circuit under test. This is a fundamental necessity to test for any intercept parameter. It is very difficult to realize a multiple frequency test input on-chip with low overheads or without requiring significant re-design of the circuit under test. Due to these challenges, a self-test for third and second order intercept is a matter of ongoing research.

The most challenging parameter for self-test is any parameter related to noise such as noise figure (in the case of LNAs) or phase noise (in the case of VCOs). There are no known on-chip techniques to quantify noise figure. Even off-chip techniques continue to be very difficult and time consuming. The most commonly used technique to test for noise figure is the Y factor method [38]. The main requirement for this technique is to have a white noise source of known noise temperature. In off-chip techniques, a device such as a noise diode is often used to generate a test input of known noise temperature. However, it is not possible to achieve anything similar to this on-chip, in standard CMOS. Additionally, any circuit that is used to measure noise must be completely noise free or have an extremely predictable noise contribution. These
challenges need to be overcome before a reliable self-test technique for noise can be devised. Although low frequency techniques for measuring jitter and zero crossings exist, it has not yet been possible to adapt these techniques to the GHz domain.

Finally, although the current-based self-test has been completely verified for the most commonly used front-end circuit topologies, there are several other circuit topologies to which the technique can be applied. It would be extremely beneficial to study the application of the technique to fully differential LNA and mixer topologies.
REFERENCES


[31] IBM Design Manual and User Manual for 0.25 micron 6-RF CMOS process


