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Nizar Bahaji

Michael Kuhl

A Simulation Study of Composite Dispatching Rules, CONWIP and Push Lot Release in Semiconductor Fabrication

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Abstract- *This paper evaluates dispatching rules and order release policies in two fabs representing two wafer fabrication modes, namely, ASIC and low-mix high-volume production. Order release policies were fixed-interval (push) release, and constant work-in-process, CONWIP (pull) policy. Following rigorous fab modeling and statistical analysis, new composite dispatching rules were found to be robust for system cycle time and due-date adherence measures, in both production modes.*

I. Introduction

In general, the success of a semiconductor manufacturer is determined by the ability of the company to provide the quantity and quality products demanded by customers in an extremely competitive environment. Although changes in technology such as larger wafer sizes and smaller chips have enhanced productivity, the highly complex nature of semiconductor manufacturing can result in high levels of work-in-process (WIP), long flow (cycle) times, and poor due-date performance if not managed properly. The concept of shop floor control addresses these issues by implementing strategies with the goal of maximizing fab productivity.

This paper addresses two main aspects of shop floor control – dispatching rules and lot release strategies. The objectives of this study are to (a) identify current benchmark and "high claim" dispatching rules and commonly used lot release strategies from the literature; (b) develop some new composite dispatching rules; (c) conduct a rigorous experimental performance evaluation using simulation to quantitatively compare the effect of the combination of dispatching

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Nizar Bahaji is with SK Daifuku Corporation, Salt Lake City, UT 84116, USA
Michael Kuhl is with the Industrial and Systems Engineering Department, Rochester Institute of Technology, Rochester, NY 14623, USA

rules and lot release strategies on key fab performance measures; and (d) identify robust combinations the shop floor control strategies in ASIC (make-to-order) and low-mix high-volume (make-to-stock) fabs.

The rest of the paper is organized as follows. Section II gives some background on shop floor control strategies. Section III summarizes previous studies involving dispatching rules and lot release strategies. The experimental performance evaluation and the results are presented in Secitons IV and V, respectively. Finally, the conclusions of this research are presented in Section VI. A list of acronyms is provided in Table XXIII.

II. Background

A. Scheduling

Scheduling refers to "the allocation of resources over time to perform tasks" [1]. While optimization methods are fit for long-term production planning [2], input regulation and dispatching respectively regulate the hourly/daily release and flow of WIP in the wafer fab. Consequently, simulation analysis methods are commonly used to capture computational and dynamic modeling complexities [3]-[4].

B. Fab Performance Measures

Wafer fabrication is characterized by unreliable tools, reentrant WIP flow, shifting bottlenecks, mixed batching modes, sequence-dependent set-ups, variable flow times, and a mix of flow-line

and job-shop aspects [5],[6]. WIP balances the benefits of buffering with inventory costs, risks of congestion, late deliveries, and product obsolescence [7],[8]. Mean WIP level (L) is related to throughput rate (λ) and cycle time (also called flow time, W), via Little's law [9]: $L = \lambda W$. Given that λ is either the input or bottleneck rate, cycle time is proportional to WIP. Cycle time is key for market responsiveness, and for reducing yield loss due to particle exposure [10]. Finally, in the fab context, contrary to typical job-shop scheduling, due-date based measures such as tardiness, are secondary to Little's law's system-oriented ones. In fact, the "98% cycle time" (the mean plus three standard deviations of cycle time), is used as an estimator of due-date adherence [11].

C. Dynamic Shop Floor Control

1) Input Regulation

Whether of the 'push' or 'pull' type, input regulation (also called *order release control*; see [5],[12] for surveys), targets "shorter, more reliable flow times by releasing work to the shop in a controlled manner" [13]. Material requirements planning (MRP) and manufacturing resources planning (MRP II) illustrate push policies; where, based on static demand and *lead time* estimates, lots are released in fixed intervals, irrespectively of floor congestion [14]. Pull strategies however, stress swift market response without excess inventory [15], i.e. WIP is fixed by compensating job completion with job release. WIP can be set at every stage (kanban systems [16]), over the entire facility (CONWIP [17]), or up to the bottleneck [10],[18].

2) Dispatching

Dispatching rules dynamically rank queues by computing lot *priority indices* [19]. They use several lot and system attributes such as: arrival time, due date, processing time(s), queue length(s), work content, and setup time. While *simple dispatching rules* use one attribute, (e.g. arrival time for FCFS (first come first serve)); *composite dispatching rules* use the attributes' ratios, exponentiation, truncation, or conditional combinations. *Scaling parameters* can also be used to weigh multiple objectives. Rule effectiveness depends on the performance measure, shop-load level, and due-date tightness [20]. A review of key composite rule building blocks is presented next. Processing time (PT) targets mean cycle time and throughput rate; but can perform well for due-date measures, under heavy traffic and tight due-dates [19]-[24]. Either the *immediate* or total *remaining* processing times can be used respectively in SPT (shortest processing time) and SRPT (shortest remaining processing time). PT-based rules however, marginalize longer-processing products. *Completed* processing time is used in the *multiplier of theoretical cycle time* (or *X factor* (XF)) [25], and relates cycle time as a multiple of its processing (non-queue) time. Arrival time (AT) refers to initial lot release time, while (AT_{Step}) is the processing step arrival time. "Time in the system" (TIS), uses the dispatching decision time minus AT. Both AT and TIS reduce cycle time variance [26],[27]. "Work in the next queue" (WINQ) adds the lots' processing times in a given queue. Its use balances WIP away from congestion [10],[26],[27]. Finally, due-date attribute use,

does not necessarily improve due-date adherence, and may hinder key cycle time and system throughput measures [28].

III. Previous Comparative Studies

An in-depth review of flow control simulation studies is found in [6]. Table I compares representative works. Some authors concluded that "a significant amount of research remains to be done in measuring the effectiveness of dispatching rules" [19]; and that "comprehensive testing of the previously developed [flow control] approaches in realistic settings" was needed [5]. Reviewers also found that “contradictory” results were common [13],[29]. Finally, fab flow studies can benefit from job-shop scheduling literature findings. Consequently, this study compares the previous shop floor control strategies in a common setting that consists of a realistic fab environment constructed from real fab data.

IV. Design of Experiments

The experimental environment is summarized in Table II. Ample detail for the 2x2x14 full factorial experiment is found in [6]. Acronyms used are described in Table XXIII.

Table I. Fab modeling and recorded performance measures in selected past studies.

	Modeling & Flow Control Aspects												Recorded Performance Measures					
	# of Workstations if reentrant fab	Dispatching	Input regulation	X parallel stations per workstation	Multiple Products	Due dates	Batch and set-up modeling	Operator modeling	Number-of-products factor	ANOVA	Mean comparison factors	Software package	Mean cycle time	Standard deviation of cycle time	Percentage of tardy jobs	Mean tardiness	Standard deviation of tardiness	Average WIP level
Wein [40] (1988)	24	✓	✓	✓								SIMAN	✓	✓				
Glassey and Resende [41] (1988)	5-41	✓	✓	✓								FabSIM (UCB)						
Lu and Kumar [42] (1991)	3	✓										SLAM II	✓	✓				
Wein and Chevalier [28] (1992)	2	✓	✓		✓	✓						Unspecified			✓	✓		✓
Ehteshami *et al.* [43] (1992)	13	✓		✓								BLOCS (UCB)	✓	✓				
Duenyas [39] (1994)	2-3	✓	✓		✓							Unspecified	✓					
Lu *et al.* [33] (1994)	12-24	✓	✓	✓		✓				✓	✓	Unspecified		✓				
Li *et al.* [44] (1996)	4	✓						✓				Unspecified	✓	✓				
Sandell and Srinivasan [11] (1996)	3-45		✓	✓						✓		Delphi & ManSIM	✓	✓				
Graves and Milne [7] (1997)	–		✓									SIMAN	✓					
Palmeri and Collins [45] (1997)	83	✓		✓	✓		✓					AutoSched 4.0	✓					
Kim *et al.* [46] (1998)	24	✓	✓	✓			✓					FACTOR AIM	✓					✓
Mittler and Schoemig [47] (1999)	73-83	✓		✓	✓		✓	✓				Delphi/FX	✓	✓				
This study	85	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	AutoSched AP 6.25	✓	✓	✓	✓	✓	✓

Table II. Summary of this study's experimental factors.

Factor	Number of levels	Levels	Remarks
Number of products	2	3 products	Low-variety fab (make-to-market)
		All 21 original products	ASIC fab (make-to-order)
Order release	2	CONWIP	Fixed-WIP
		Push	Fixed-interval
Dispatching	14	FCFS	Benchmark
		CR	Benchmark
		EDD	Benchmark
		LWNQ	Benchmark
		ESD	Benchmark
		HXF	Benchmark
		CR+SPT	Anderson and Nyirenda [32]
		AT-RPT	Holthaus [27] & Lu *et al.* [33]
		PT/TIS	Holthaus [27]
		(PT+WINQ)/TIS	Holthaus [27]
		(PT+WINQ)/XF	New/Proposed
		(AT_{Step}-RPT)/XF	New/Proposed
		Wt(PT+WINQ)/XF	New/Proposed
		Wt(AT_{Step}-RPT)/XF	New/Proposed

A. Experimental Factors

1) Dispatching Rules

Rules expedite lots with the least priority index value. To avoid redundancy, *i* and *j* indices (Fig.1), were only used when lot or step-specific attributes were used.

i	:	Job (lot) index
j , q	:	Operation (processing step) indices
n	:	Job type index
α	:	Due-date tightness level
η	:	Machine utilization rate
d	:	Due date
m	:	Number of operations
p	:	Processing time
t	:	Time of the dispatching decision
β	:	Shop floor arrival time
σ	:	Operation arrival time
ω	:	Work content (sum of processing times of jobs in the queue)
W	:	Estimated waiting time in next step

Figure 1. Priority index notation.

Benchmark and past research priority indices are given as follows

$$FCFS_{inj} = \sigma_{inj} \tag{1}$$

$$ESD_{in} = \beta_{in} \tag{2}$$

$$EDD_{in} = d_{in} \tag{3}$$

$$LWNQ_{nj} = \omega_{n(j+1)} \tag{4}$$

$$CR_{inj} = \frac{d_{in} - t}{\sum_{q=j}^{m_n} p_{nq}} \tag{5}$$

$$HXF_{inj} = \frac{1}{\left(\frac{t - \beta_{in}}{\sum_{q=1}^{j} p_{nq}} \right)} \tag{6}$$

$$(AT\text{-}RPT)_{inj} = \beta_{in} - \sum_{q=j}^{m_n} p_{nq}. \tag{7}$$

$$(CR + SPT)_{inj} = p_{nj} \cdot \max\left[\frac{d_{in} - t}{\sum_{q=j}^{m_n} p_{nq}}, 1.0\right] \tag{8}$$

$$(PT+WINQ)/TIS_{inj} = \frac{p_{nj} + \alpha_{n(j+1)}}{t - \beta_{in}} \tag{9}$$

$$(PT/TIS)_{inj} = \frac{p_{nj}}{t - \beta_{in}}. \tag{10}$$

Our proposed rules are given as

$$(PT+WINQ)/XF_{inj} = \frac{p_{nj} + \alpha_{nj+1}}{\left(\frac{t - \beta_{in}}{\sum_{q=1}^{j} p_{nq}}\right)} \tag{11}$$

$$(AT_{Step}\text{-}RPT)/XF_{inj} = \frac{\sigma_{inj} - \sum_{q=j}^{m_n} p_{nq}}{\left(\frac{t - \beta_{in}}{\sum_{q=1}^{j} p_{nq}}\right)} \tag{12}$$

$$Wt(PT+WINQ)/XF_{inj} = \exp\left(-\frac{t - \beta_{in}}{\sum_{q=1}^{j} p_{nq}}\right) \cdot \left(\frac{p_{nj} + \omega_{n(j+1)}}{\left(\frac{t - \beta_{in}}{\sum_{q=1}^{j} p_{nq}}\right)}\right) + \exp\left(\frac{t - \beta_{in}}{\sum_{q=1}^{j} p_{nq}}\right) \cdot \left(\frac{1}{\left(\frac{t - \beta_{in}}{\sum_{q=1}^{j} p_{nq}}\right)}\right) \tag{13}$$

$$Wt(AT_{Step}\text{-}RPT)/XF_{inj} = \left(\sigma_{inj} - \sum_{q=1}^{j} p_{nq}\right) \cdot Wt(PT+WINQ)/XF_{inj}. \tag{14}$$

Equation 14 may be shown in attribute abbreviation terms, where the scaling parameters are highlighted:

$$Wt(PT+WINQ)/XF = \mathbf{exp(-XF)} \cdot \left(\frac{PT + WINQ}{XF} \right) + \mathbf{exp(XF)} \cdot \left(\frac{1}{XF} \right) \quad (15)$$

The new rules introduced XF, as a priority index building block; *and* a dynamic scaling parameter into (9). System-based scaling parameters eliminate trial-and-error simulation to find the weight of the parameters [30]. For instance, Raghu and Rajendran [22] weighed the processing time and the due-date attributes as a function of the utilization of the system:

$$RR_{ij} = \left(\frac{d_i - t - \sum_{q=j}^{m_i} p_{iq}}{\sum_{q=j}^{m_i} p_{iq}} \right) (\exp - \eta) p_{ij} + \exp(\eta) p_{ij} + W_{i(j+1)} \quad (16)$$

In our new rules, key lot and fab status attributes such as PT and WINQ are weighed based on how the lot is faring for its cycle time relative to its processing time (XF). Wt(PT+WINQ)/XF expedites lots with the least sum of (PT+WINQ)/XF and 1/XF. Further, the greater XF, the greater the weight of the *(1/XF)* component. Stated otherwise, PT and WINQ, are given less weight when the lot lags behind its processing time. Finally, Wt(AT_{Step}-RPT)/XF blended (AT_{Step}-RPT)/XF into Wt(PT+WINQ)/XF, to improve the latter's cycle time variance performance.

2) Input Regulation

In CONWIP, separate fixed-WIP levels were set for each product. In each fab, the average

product-specific WIP levels found under push, were reused in CONWIP. The FCFS levels were used across the rest of the rules because we wanted to reduce this experiment's number of factors.

3) Number of Products/ Production Mode

The number-of-products (or fab type) factor addresses whether make-to-order (high mix and low volume (ASIC)) and make-to-market (low mix and high volume) production modes affect dispatching and lot release performance. In order to have the factory be the controlled variable, we selected a single fab, fixed all its operating characteristics, and only varied the number of products, by releasing a fraction of the original ASIC products, and increasing the individual product release rates, as to end up with the same overall throughput rate in both fabs. For the low-variety level, 3 products were chosen as to have similar tool utilization levels as in the original 21-product case.

B. Experimental Test Bed

SEMATECH set 5 [31] held an anonymous fab's data such as product routings, processing times, and equipment/operator availability. It was downloaded via ftp from the Arizona State University *Modeling and Analysis for Semiconductor Manufacturing* laboratory site. It is summarized in Table III.

C. Simulation Protocol

AutoSched AP version 6.25 of *AutoSimulations, Inc.*, Bountiful, Utah, was operated on two 128 megabyte RAM *Pentium* desktop computers running *Microsoft Windows NT 4.0*. Some rules tested

were implemented with customized C++ code. Model validation used the sample run data in [31]. The replication-deletion method was used to reproduce point estimates and confidence intervals for the response measures (Tables IV and V). Tool reliability is the main factor behind variability, and different random stream seed increments were used in each treatment level. Also note that including batching, set-ups, operators and reentrant flow sets this study apart from job shop studies.

Table III. Key characteristics of SEMATECH Set 5 [31] as modeled in this study.

Modeling aspect	**Set 5** [31]
Product type	ASIC
Number of products	21
Number of routes	14
Lot wafer size	25, 50
Average number of process steps per layer	30
Number of work centers (tool groups)	85
Number of identical machines per work center	1 - 9
Operators modeled?	Yes
Rework modeled?	No
Yield loss (scrap) modeled?	No
Automated material handling or travel time	No
Wafer starts per month (approximately)	10,000
Raw process time range (hours)	172-368
Number of processing steps range	117-259
Total number of processing steps	3824
PM included?	Yes
Batching policy	MBS (greedy)
Group set-up modeled?	No
Job type set-up modeled?	Yes
Processing time distributions	Constant
Load and unload time distributions	Constant
Setup time distributions	Constant
MTTF distributions	Exponential
MTTR distributions	Exponential

D. Due-date Tightness

Due-date tightness was a controlled factor in this study. The total work content method was used to assign each lot a due date based on a multiple of two of its total processing time, which was added at the time of lot release. Only EDD, CR, and CR+SPT used due-date information.

Table IV. Description of relevant performance measures.

Performance measure	Abbreviation	Description
Number of completed lots	Lots out	Number of completed lots over the non-transient simulation run time period
Average WIP level	WIPAVG	Average number of lots present in the fab at any time during the non-transient run time
Mean cycle time	MCT	Average time a lot spends in the fab from release to completion
Standard deviation of cycle time	SDCT	Standard deviation of cycle time
98% cycle time	98% CT	MCT + 3 SDCT (Industry jargon with no relation to the central limit theorem)
Percentage of tardy lots	%Tardy	Percentage of the lots which were completed past their respective due-dates
Mean tardiness	MT	Average time duration a lot is past due, if late
Standard deviation of tardiness	SDT	Standard deviation of tardiness
% over FCFS	–	Rule's improvement in percentage terms over FCFS under the same release mechanism
% over push	–	Rule's CONWIP's improvement in percentage terms over push
95% confidence interval	(± CI)	Confidence interval

Table V. Simulation run assumptions.

Modeling aspects	This study
Total throughout rate (wafers/week)	2218.6
Run length (years)	5
Transient period (years)	1
Number of replications	10
Confidence interval level	95%
Common random numbers	No

E. Batching and Dispatching Assumptions

Figure 2 summarizes how the added presence of batching affected the dispatching function including the sequence of decisions that face the lot and the tool before processing.

Sequence of major decisions facing lots before processing	Sequence of major decisions made by tools before processing
1. Lot arrives in tool group queue	1. Tool becomes available after 'busy' or 'down' state
2. Lot batch-ID is checked	2. Tool reevaluates priority index for all lots in tool group queue
3. Lot is added to own virtual batch group.	3. Tool selects lot with highest urgency, based on smallest value returned by priority index
4. New batch group is created if lot is first of its kind	4. If tool is a batching process, then
5. Lot's dispatching priority index is recomputed each time the tool becomes idle.	a. Look for same-batch-group lots in the tool group queue
6. Lot waits to be selected for processing in tool group queue	b. Add compatible lot(s) to the batch
	c. Wait for lot arrival(s) if no compatible lot is in the queue
	d. Stop if minimum batch size is reached
	5. Tool starts processing lot or batch

Figure 2. Major assumptions about batching and dispatching in this simulation study.

F. Statistical Analysis Methodology

Using *SAS* version 8.0, our analysis referred to 1, 2 and 3-way ANOVA's, and hypothesis tests for relevant factors at stake. These were followed by the Ryan multiple comparison procedures (MCP) to rank the factor levels.

V. Results and Discussion

A. Experimental Results

Table VI confirms Little's law in the push case, as smaller average WIP led to shorter MCT. Our proposed rules showed 2% MCT improvements over FCFS. As for SDCT, 50% and 25% improvements over FCFS were respectively achieved by AT-RPT; and (AT_{Step}-RPT)/XF; in the 3 and 21-product cases. Fewer rules competed with FCFS in the pull cases (Table VI), where throughput fluctuations, were due to generalizing the FCFS WIP levels. Compared with push, pull performance deteriorated for most rules other than FCFS (Table VII). Finally, the new rules substantially improved due-date adherence in both fabs (Table VIII).

B. Analysis of Variance Results

The three-way analysis of variance factors (number of products, order release, and dispatching) and their interactions; significantly affected MCT and SDCT. This was followed by relevant 2-way ANOVAs (DR x OR) for each and both fabs combined; and 1-way ANOVAS (DR) for each combination of order release and fab type. The ANOVA table is only shown for the 3-way case (Table IX). As the null hypothesis for equality of means was rejected at the 5% significance level for all the relevant ANOVAs, Ryan MCP tables will be the focus of the next section.

Table VI. Experimental results from the push and CONWIP cases.

	No. of Products	Dispatching Rule	Lots Out	WIP AVG	MCT		SDCT		98% CT	
			lots	lots (± CI)	hours (±CI)	% over FCFS	hours (±CI)	% over FCFS	hours	% over FCFS
Push	3	FCFS	13261	168.2 (± 0.81)	444.6 (± 2.13)	-	41.2 (± 0.51)	-	568.1	-
		EDD	13266	175.9 (± 1.05)	465.0 (± 2.77)	-4.6%	60.8 (± 0.54)	-46.6%	647.1	-13.9%
		CR	13267	175.4 (± 0.81)	463.6 (± 2.14)	-4.2%	46.7 (± 1.06)	-13.3%	602.3	-6.0%
		LWNQ	13257	168.8 (± 0.52)	446.3 (± 1.37)	-0.2%	51.7 (± 0.77)	-25.5%	598.0	-5.3%
		ESD	13263	179.5 (± 0.69)	474.5 (± 1.83)	-6.7%	22.4 (± 0.70)	45.5%	541.9	4.6%
		HXF	13262	165.0 (± 0.51)	436.1 (± 1.36)	1.9%	46.8 (± 0.30)	-13.8%	576.6	-1.5%
		CR+SPT	13268	171.7 (± 1.02)	454.0 (± 2.68)	-2.1%	64.6 (± 0.77)	-56.9%	647.8	-14.0%
		AT-RPT	13260	178.4 (± 0.94)	471.8 (± 2.48)	-6.1%	20.2 (± 0.83)	50.9%	532.4	6.3%
		PT/TIS	13261	170.8 (± 0.90)	451.5 (± 2.36)	-1.6%	65.7 (± 1.15)	-59.6%	648.6	-14.2%
		(PT+WINQ)/TIS	13264	169.8 (± 0.73)	448.8 (± 1.93)	0.9%	49.8 (± 0.53)	-21.0%	676.4	-19.1%
		(PT+WINQ)/XF	13260	165.0 (± 0.77)	436.2 (± 2.04)	1.9%	60.2 (± 1.16)	-46.4%	617.0	-8.6%
		(AT_{Step}-RPT)/XF	13260	165.5 (± 0.55)	437.6 (± 1.46)	1.6%	46.9 (± 0.48)	-13.8%	578.3	-1.8%
		Wt(PT+WINQ)/XF	13264	164.8 (± 0.42)	435.7 (± 1.11)	2.0%	53.7 (± 0.25)	-23.4%	596.8	-5.1%
		Wt(AT_{Step}-RPT)/XF	13258	164.5 (± 0.58)	434.8 (± 1.54)	2.2%	51.2 (± 0.53)	-24.4%	588.4	-3.6%
	21	FCFS	13262	186.4 (± 0.92)	492.9 (± 2.43)	-	91.8 (± 2.66)	-	774.4	-
		EDD	13254	194.2 (± 0.79)	513.4 (± 2.07)	-4.2%	97.5 (± 1.33)	-6.2%	806.0	-4.1%
		CR	13260	196.3 (± 2.74)	519.2 (± 7.27)	-5.3%	88.6 (± 4.01)	3.6%	784.9	-1.4%
		LWNQ	13257	191.9 (± 1.38)	507.5 (± 3.63)	-3.0%	117.2 (± 5.87)	-27.6%	859.0	-10.9%
		ESD	13262	195.6 (± 1.93)	517.2 (± 5.08)	-4.9%	74.7 (± 5.01)	18.6%	741.3	4.3%
		HXF	13261	186.7 (± 1.85)	493.7 (± 4.91)	-0.2%	73.5 (± 4.87)	19.9%	714.3	7.8%
		CR+SPT	13257	193.4 (± 1.20)	511.5 (± 3.18)	-3.8%	95.9 (± 1.64)	-4.4%	799.0	-3.2%
		AT-RPT	13260	194.2 (± 1.71)	513.5 (± 4.53)	-4.2%	72.1 (± 4.94)	21.5%	729.9	5.8%
		PT/TIS	13258	191.3 (± 1.04)	505.8 (± 2.72)	-2.6%	92.7 (± 2.63)	-0.9%	783.8	-1.2%
		(PT+WINQ)/TIS	13261	190.0 (± 1.38)	502.3 (± 3.64)	-1.9%	87.2 (± 3.62)	5.1%	763.9	1.4%
		(PT+WINQ)/XF	13264	185.9 (± 1.81)	491.6 (± 4.77)	0.3%	85.4 (± 4.69)	7.0%	747.9	3.4%
		(AT_{Step}-RPT)/XF	13259	184.8 (± 1.52)	488.5 (± 4.02)	0.9%	69.1 (± 2.57)	24.7%	695.8	10.2%
		Wt(PT+WINQ)/XF	13262	182.9 (± 1.15)	483.7 (± 3.04)	1.9%	76.0 (± 2.19)	17.2%	711.7	8.1%
		Wt(AT_{Step}-RPT)/XF	13262	182.8 (± 0.93)	483.2 (± 2.45)	2.0%	73.7 (± 1.96)	19.7%	704.4	9.0%
Pull (CONWIP)	3	FCFS	13036	168	451.9 (± 0.98)	-	46.8 (± 0.80)	-	592.2	-
		EDD	12867	168	446.7 (± 1.44)	1.2%	102.9 (± 2.40)	-120.0%	755.3	-27.5%
		CR	10392	168	566.5 (± 4.12)	-25.4%	214.6 (± 4.77)	-358.8%	1210.2	-104.4%
		LWNQ	13011	168	452.8 (± 1.05)	-0.2%	61.1 (± 1.07)	-30.6%	636.0	-7.4%
		ESD	13041	168	451.7 (± 0.75)	0.1%	46.7 (± 0.90)	0.0%	591.9	0.1%
		HXF	9817	168	582.1 (± 7.36)	-28.8%	309.7 (± 6.46)	-562.2%	1511.1	-155.2%
		CR+SPT	12994	168	450.4 (± 1.51)	0.3%	90.6 (± 2.08)	-93.8%	722.3	-22.0%
		AT-RPT	10447	168	531.5 (± 40.04)	-17.6%	163.9 (± 36.30)	-250.5%	1023.2	-72.8%
		PT/TIS	12944	168	450.2 (± 2.08)	0.4%	114.8 (± 3.97)	-145.5%	794.7	-34.2%
		(PT+WINQ)/TIS	12968	168	450.3 (± 1.77)	0.4%	105.5 (± 3.04)	-125.6%	766.8	-29.5%
		(PT+WINQ)/XF	12366	168	467.3 (± 2.34)	-3.4%	152.0 (± 6.06)	-225.0%	923.2	-55.9%
		(AT_{Step}-RPT)/XF	9826	168	583.0 (± 3.13)	-29.0%	298.4 (± 5.31)	-538.1%	1478.1	-149.6%
		Wt(PT+WINQ)/XF	12995	168	453.5 (± 1.15)	-0.4%	44.7 (± 0.94)	4.4%	587.7	0.8%
		Wt(AT_{Step}-RPT)/XF	9925	168	577.8 (± 3.43)	-27.8%	287.8 (± 3.57)	-515.6%	1441.3	-143.4%
	21	FCFS	13296	188	495.8 (± 1.16)	-	90.2 (± 0.83)	-	766.4	-
		EDD	13140	188	501.6 (± 0.81)	-1.2%	218.6 (± 4.40)	-142.3%	1157.3	-51.0%
		CR	10933	188	602.2 (± 6.31)	-17.7%	229.9 (± 5.18)	-154.9%	1291.9	-68.6%
		LWNQ	13239	188	498.0 (± 0.71)	-0.4%	104.8 (± 1.08)	-16.2%	812.4	-6.0%
		ESD	13304	188	495.6 (± 0.41)	0.1%	90.8 (± 0.55)	-0.7%	768.0	-0.2%
		HXF	11548	188	570.4 (± 4.32)	-15.0%	236.8 (± 4.49)	-162.5%	1280.8	-67.1%
		CR+SPT	12859	188	512.7 (± 1.21)	-3.4%	138.6 (± 2.27)	-53.7%	928.5	-21.2%
		AT-RPT	10871	188	605.6 (± 2.93)	-22.1%	220.3 (± 6.52)	-144.3%	1266.6	-65.3%
		PT/TIS	12865	188	512.0 (± 1.00)	-3.3%	187.5 (± 2.56)	-107.9%	1074.7	-40.2%
		(PT+WINQ)/TIS	12880	188	511.8 (± 1.12)	-3.2%	174.6 (± 3.11)	-93.5%	1035.6	-35.1%
		(PT+WINQ)/XF	12148	188	542.8 (± 2.70)	-9.5%	215.6 (± 4.37)	-139.1%	1189.6	-55.2%
		(AT_{Step}-RPT)/XF	11487	188	573.1 (± 6.98)	-15.6%	229.0 (± 6.57)	-153.9%	1260.1	-64.4%
		Wt(PT+WINQ)/XF	13184	188	500.2 (± 0.75)	-0.9%	89.2 (± 0.44)	1.1%	767.8	-0.2%
		Wt(AT_{Step}-RPT)/XF	11759	188	560.7 (± 5.84)	-13.1%	221.5 (± 6.57)	-145.6%	1225.1	-59.8%

Table VII CONWIP's relative performance for MCT, SDCT, and 98% CT.

No. of Products	Dispatching Rule	MCT	SDCT	98% CT
		% Improvement over push		
3	FCFS	-1.6%	-13.6%	-4.2%
	EDD	3.9%	-69.2%	-16.7%
	CR	-22.2%	-359.9%	-100.9%
	LWNQ	-1.4%	-18.2%	-6.4%
	ESD	4.8%	-108.2%	-9.2%
	HXF	-33.5%	-561.4%	-162.1%
	CR+SPT	0.8%	-40.3%	-11.5%
	AT-RPT	-12.7%	-711.3%	-92.2%
	PT/TIS	0.3%	-74.8%	-22.5%
	(PT+WINQ)/TIS	-0.4%	-111.7%	-13.4%
	(PT+WINQ)/XF	-7.1%	-152.2%	-49.6%
	(AT_{Step}-RPT)/XF	-33.2%	-536.5%	-155.6%
	Wt(PT+WINQ)/XF	-4.1%	16.7%	1.5%
	Wt(AT_{Step}-RPT)/XF	-32.9%	-462.1%	-144.9%
21	FCFS	-0.6%	1.8%	1.0%
	EDD	2.3%	-124.1%	-43.6%
	CR	-16.0%	-159.6%	-64.6%
	LWNQ	1.9%	10.6%	5.4%
	ESD	4.2%	-21.6%	-3.6%
	HXF	-15.5%	-222.0%	-79.3%
	CR+SPT	-0.2%	-44.6%	-16.2%
	AT-RPT	-17.9%	-205.5%	-73.5%
	PT/TIS	-1.2%	-102.4%	-37.1%
	(PT+WINQ)/TIS	-1.9%	-100.2%	-35.6%
	(PT+WINQ)/XF	-10.4%	-152.3%	-59.1%
	(AT_{Step}-RPT)/XF	-17.3%	-231.4%	-81.1%
	Wt(PT+WINQ)/XF	-3.4%	-17.4%	-7.9%
	Wt(AT_{Step}-RPT)/XF	-16.0%	-200.3%	-73.9%

Table VIII Experimental results for secondary performance measures for the push case.

	No. of Products	Dispatching Rule	% Tardy		MT		SDT	
			% (±CI)	% over FCFS	hours (±CI)	% over FCFS	hours (±CI)	% over FCFS
Push	3	FCFS	0.02 % (±	-	9.6 (±4.01)	-	5.9 (±5.22)	-
		EDD	0.01 % (±	50.0%	6.4 (±3.26)	33.7%	4.0 (±3.77)	31.6%
		CR	0.16 % (±	-700.0%	6.5 (±2.87)	33.0%	7.7 (±3.35)	-30.4%
		LWNQ	0.90 % (±	-4400.0%	28.3 (±2.77)	-193.0%	28.0 (±3.04)	-374.9%
		ESD	1.52 % (±	-7500.0%	11.4 (±2.00)	-18.3%	10.8 (±2.11)	-82.5%
		HXF	0%	100.0%	0	100.0%	0	100.0%
		CR+SPT	0.06 % (±	-200.0%	6.9 (± 2.95)	28.2%	5.0 (±2.70)	15.3%
		AT-RPT	1.67 % (±	-8250.0%	11.6 (± 1.09)	-20.3%	11.5 (± 1.11)	-95.9%
		PT/TIS	0.13 % (±	-550.0%	16.8 (± 8.12)	-74.4%	9.6 (± 6.37)	-63.7%
		(PT+WINQ)/TIS	0.04 % (±	-100.0%	12.5 (± 4.94)	-29.2%	6.4 (± 5.93)	-8.2%
		(PT+WINQ)/XF	0%	100.0%	0	100.0%	0	100.0%
		(AT_{Step}-RPT)/XF	0%	100.0%	0	100.0%	0	100.0%
		Wt(PT+WINQ)/XF	0%	100.0%	0	100.0%	0	100.0%
		Wt(AT_{Step}-RPT)/XF	0%	100.0%	0	100.0%	0	100.0%
	21	FCFS	10.29 % (±	-	23.9 (±2.68)	-	20.6 (±1.89)	-
		EDD	12.62 % (±	-22.6%	31.9 (±1.58)	-33.2%	25.1 (±1.66)	-21.8%
		CR	14.94 % (±	-45.2%	17.3 (±7.02)	27.7%	17.0 (±5.77)	17.7%
		LWNQ	19.02 % (±	-84.8%	83.1 (±8.82)	-247.3%	74.3 (±8.18)	-260.1%
		ESD	13.34 % (±	-29.6%	28.9 (±7.89)	-20.9%	23.0 (±5.24)	-11.7%
		HXF	3.01 % (±	70.8%	13.2 (±4.88)	45.0%	11.3 (±2.92)	45.2%
		CR+SPT	13.03 % (±	-26.6%	12.2 (± 2.98)	49.1%	13.5 (±3.01)	34.4%
		AT-RPT	11.75 % (±	-14.2%	22.3 (± 3.89)	6.8%	19.3 (±2.31)	6.3%
		PT/TIS	14.41 % (±	-40.0%	42.3 (± 2.61)	-76.7%	30.8 (±2.21)	-49.4%
		(PT+WINQ)/TIS	11.21 % (±	-8.9%	41.0 (±4.30)	-71.2%	30.4 (±3.27)	-47.4%
		(PT+WINQ)/XF	5.53 % (±	46.3%	20.1 (±9.09)	16.0%	15.0 (±4.74)	27.5%
		(AT_{Step}-RPT)/XF	0.70 % (±	93.2%	9.9 (±3.52)	58.6%	8.5 (±2.73)	58.6%
		Wt(PT+WINQ)/XF	0.77 % (±	92.5%	9.3 (± 3.25)	61.1%	7.4 (±3.13)	64.2%
		Wt(AT_{Step}-RPT)/XF	0.32 % (±	96.9%	5.6 (±2.00)	76.5%	5.5 (±2.27)	73.4%

Table IX. Overall 3-way ANOVAs for the 2x2x14 experiment.

Response Measure	Source of Variation	DF	Sum of Squares	Mean Square	F	Pr > F
MCT	NO. OF PRODUCTS (NP)	1	297081.48	297081.48	3924.11	<.0001
	ORDER RELEASE (OR)	1	205873.54	205873.54	2719.36	<.0001
	DISPATCHING (DR)	13	298872.76	22990.21	303.67	<.0001
	NP x OR	1	4380.89	4380.89	57.87	<.0001
	NP x DR	13	31847.1	2449.78	32.36	<.0001
	OR x DR	13	343669.43	26436.11	349.19	<.0001
	NP x OR x DR	13	33317.27	2562.87	33.85	<.0001
	ERROR	504	38156.2	75.71		
	TOTAL	559	1253198.67			
SDCT	NO. OF PRODUCTS (NP)	1	151719.72	151719.72	2252	<.0001
	ORDER RELEASE (OR)	1	1216025.14	1216025.14	18049.7	<.0001
	DISPATCHING (DR)	13	680142.08	52318.62	776.57	<.0001
	NP x OR	1	1992.14	1992.14	29.57	<.0001
	NP x DR	13	134586.91	10352.84	153.67	<.0001
	OR x DR	13	791205.02	60861.93	903.38	<.0001
	NP x OR x DR	13	95821.57	7370.89	109.41	<.0001
	ERROR	504	33955.01	67.37		
	TOTAL	559	3105447.6			

C. Ryan Mean Comparison Procedure Results

For MCT, (Push x Wt(AT_{Step}-RPT)/XF) and (Push x Wt(PT+WINQ)/XF) pairs ranked best for both fabs combined (Table X). However, neither was statistically distinct from 18 other pairs, including FCFS under both push and pull. ESD, EDD, CR+SPT, PT/TIS and LWNQ were statistically unaffected by OR; while (AT_{Step}-RPT)/XF, HXF, and Wt(AT_{Step}-RPT)/XF worsened in going from push to pull. CR was a poor MCT performer in both release policies. As for SDCT, even though push had an edge (e.g., Push x AT-RPT), large overlapping groups remained, and no rule statistically improved in going from push to pull. Lastly, (AT_{Step}-RPT)/XF, Wt(AT_{Step}-RPT)/XF, HXF, and AT-RPT, deteriorated under pull.

Table X Ryan MCP ranking for the (OR x DR) factor: Both factories combined.

MCT		SDCT	
(OR x DR)	(hours)	(OR x DR)	(hours)
Push x Wt(AT_{Step}-RPT)/XF	459.0	Push x AT-RPT	46.2
Push x Wt(PT+WINQ)/XF	459.7	Push x ESD	48.6
Push x (AT_{Step}-RPT)/XF	463.1	Push x (AT_{Step}-RPT)/XF	58.0
Push x (PT+WINQ)/XF	463.9	Push x HXF	60.2
Push x HXF	464.9	Push x Wt(AT_{Step}-RPT)/XF	62.5
Push x FCFS	468.8	Push x Wt(PT+WINQ)/XF	64.9
CONWIP x ESD	473.6	Push x FCFS	66.5
CONWIP x FCFS	473.9	CONWIP x Wt(PT+WINQ)/XF	67.0
CONWIP x EDD	474.2	Push x CR	67.6
CONWIP x LWNQ	475.4	CONWIP x FCFS	68.5
Push x (PT+WINQ)/TIS	475.6	Push x (PT+WINQ)/TIS	68.5
CONWIP x Wt(PT+WINQ)/XF	476.9	CONWIP x ESD	68.8
Push x LWNQ	476.9	Push x (PT+WINQ)/XF	72.9
Push x PT/TIS	478.7	Push x EDD	79.2
CONWIP x (PT+WINQ)/TIS	481.1	Push x PT/TIS	79.2
CONWIP x PT/TIS	481.1	Push x CR+SPT	80.2
CONWIP x CR+SPT	481.6	CONWIP x LWNQ	82.9
Push x CR+SPT	482.7	Push x LWNQ	84.4
Push x EDD	489.2	CONWIP x CR+SPT	114.6
Push x CR	491.4	CONWIP x (PT+WINQ)/TIS	140.0
Push x AT-RPT	492.6	CONWIP x PT/TIS	151.2
Push x ESD	495.9	CONWIP x EDD	160.7
CONWIP x (PT+WINQ)/XF	505.0	CONWIP x (PT+WINQ)/XF	183.8
CONWIP x AT-RPT	568.6	CONWIP x AT-RPT	192.1
CONWIP x Wt(AT_{Step}-RPT)/XF	569.2	CONWIP x CR	222.2
CONWIP x HXF	576.2	CONWIP x Wt(AT_{Step}-RPT)/XF	254.7
CONWIP x (AT_{Step}-RPT)/XF	578.1	CONWIP x (AT_{Step}-RPT)/XF	263.7
CONWIP x CR	584.4	CONWIP x HXF	273.2

In the 21-product fab, Wt(PT+WINQ)/XF and Wt(AT_{Step}-RPT)/XF under push, were best for MCT, while being distinct from (Push x FCFS) (Table XI). The former was robust under pull. FCFS, PT/TIS, and especially CR+SPT were insensitive to OR. Except for EDD, ESD, and LWNQ, dispatching rules fared better under push. As for SDCT; ESD, HXF, AT-RPT, (AT_{Step}-RPT)/XF, Wt(PT+WINQ)/XF, and Wt(AT_{Step}-RPT)/XF, all under push; were best. CONWIP only benefited LWNQ. Best performers such as AT-RPT, (AT_{Step}-RPT)/XF, HXF, and Wt(AT_{Step}-RPT)/XF deteriorated under pull.

In the 3-product fab, there is more group overlap for MCT (Table XII). The top (Push x Wt(AT_{Step}-RPT)/XF) and (Push xWt(PT+WINQ)/XF), were in the same group as 14 other pairs.

Table XI. Ryan MCP ranking for the (OR x DR) factor: 21-product fab.

MCT		SDCT	
(OR x DR)	(hours)	(OR x DR)	(hours)
Push x Wt(AT_{Step}-RPT)/XF	483.2	Push x (AT_{Step}-RPT)/XF	69.1
Push x Wt(PT+WINQ)/XF	483.7	Push x AT-RPT	72.1
Push x (AT_{Step}-RPT)/XF	488.5	Push x HXF	73.5
Push x (PT+WINQ)/XF	491.6	Push x Wt(AT_{Step}-RPT)/XF	73.7
Push x FCFS	492.9	Push x ESD	74.7
Push x HXF	493.7	Push x Wt(PT+ WINQ)/XF	76.0
CONWIP x ESD	495.6	Push x (PT+WINQ)/XF	85.5
CONWIP x FCFS	495.9	Push x (PT+WINQ)/TIS	87.2
CONWIP x LWNQ	498.0	Push x CR	88.6
CONWIP x Wt(PT+WINQ)/XF	500.2	CONWIP x Wt(PT+WINQ)/XF	89.2
CONWIP x EDD	501.6	CONWIP x FCFS	90.2
Push x (PT+WINQ)/TIS	502.3	CONWIP x ESD	90.8
Push x PT/TIS	505.8	Push x FCFS	91.8
Push x LWNQ	507.5	Push x PT/TIS	92.7
Push x CR+SPT	511.5	Push x CR+SPT	95.9
CONWIP x (PT+WINQ)/TIS	511.8	Push x EDD	97.5
CONWIP x PT/TIS	512.0	CONWIP x LWNQ	104.8
CONWIP x CR+SPT	512.7	Push x LWNQ	117.2
Push x EDD	513.4	CONWIP x CR+SPT	138.6
Push x AT-RPT	513.5	CONWIP x (PT+WINQ)/TIS	174.6
Push x ESD	517.2	CONWIP x PT/TIS	187.5
Push x CR	519.2	CONWIP x (PT+WINQ)/XF	215.6
CONWIP x (PT+WINQ)/XF	542.8	CONWIP x EDD	218.6
CONWIP x Wt(AT_{Step}-RPT)/XF	560.7	CONWIP x AT-RPT	220.3
CONWIP x HXF	570.4	CONWIP x Wt(AT_{Step}-RPT)/XF	221.5
CONWIP x (AT_{Step}-RPT)/XF	573.1	CONWIP x (AT_{Step}-RPT)/XF	229.0
CONWIP x CR	602.2	CONWIP x CR	229.9
CONWIP x AT-RPT	605.6	CONWIP x HXF	236.8

Table XII. Ryan MCP ranking for the (OR x DR) factor: 3-product fab.

MCT		SDCT	
(OR x DR)	(hours)	(OR x DR)	(hours)
Push x Wt(AT_{Step}-RPT)/XF	434.8	Push x AT-RPT	20.2
Push x Wt(PT+WINQ)/XF	435.7	Push x ESD	22.5
Push x HXF	436.1	Push x FCFS	41.2
Push x (PT+WINQ)/XF	436.2	CONWIP x Wt(PT+WINQ)/XF	44.7
Push x (AT_{Step}-RPT)/XF	437.7	Push x CR	46.7
Push x FCFS	444.6	CONWIP x ESD	46.8
Push x LWNQ	446.3	CONWIP x FCFS	46.8
CONWIP x EDD	446.7	Push x HXF	46.8
Push x (PT+WINQ)/TIS	448.8	Push x (AT_{Step}-RPT)/XF	46.9
CONWIP x PT/TIS	450.3	Push x (PT+WINQ)/TIS	49.8
CONWIP x (PT+WINQ)/TIS	450.3	Push x Wt(AT_{Step}-RPT)/XF	51.2
CONWIP x CR+SPT	450.4	Push x LWNQ	51.7
Push x PT/TIS	451.5	Push x Wt(PT+WINQ)/XF	53.7
CONWIP x ESD	451.7	Push x (PT+WINQ)/XF	60.3
CONWIP x FCFS	451.9	Push x EDD	60.8
CONWIP x LWNQ	452.8	CONWIP x LWNQ	61.1
CONWIP x Wt(PT+WINQ)/XF	453.5	Push x CR+SPT	64.6
Push x CR+SPT	454.0	Push x PT/TIS	65.7
Push x CR	463.6	CONWIP x CR+SPT	90.6
Push x EDD	465.0	CONWIP x EDD	102.9
CONWIP x (PT+WINQ)/XF	467.3	CONWIP x (PT+WINQ)/TIS	105.5
Push x AT-RPT	471.8	CONWIP x PT/TIS	114.8
Push x ESD	474.5	CONWIP x (PT+WINQ)/XF	152.0
CONWIP x AT-RPT	531.5	CONWIP x AT-RPT	163.9
CONWIP x CR	566.5	CONWIP x CR	214.6
CONWIP x Wt(AT_{Step}-RPT)/XF	577.8	CONWIP x Wt(AT_{Step}-RPT)/XF	287.8
CONWIP x HXF	582.1	CONWIP x (AT_{Step}-RPT)/XF	298.4
CONWIP x (AT_{Step}-RPT)/XF	583.0	CONWIP x HXF	309.7

Pull and push pairs of CR+SPT, LWNQ, FCFS, PT/TIS, (PT+WINQ)/TIS were not statistically different. Only EDD and ESD statistically improved from push to pull. Contrary to the ASIC fab, we can notice a better pull performance, but without statistically improving any rule over push. Finally, the best SDCT group was made of (Push x ESD) and (Push x AT-RPT). FCFS, LWNQ, and Wt(PT+WINQ)/XF were statistically insensitive to OR; and HXF, AT-RPT, (AT_{Step}-RPT)/XF, and CR were dramatically eroded by pull.

In the 21-product fab under pull, top MCT rules were such for SDCT as well: FCFS, ESD, and Wt(PT+WINQ)/XF (Table XIII). LWNQ was in the best performing MCT group and was in the second best group for SDCT. HXF, CR, and (AT_{Step}-RPT)/XFlagged in both MCT and SDCT.

Table XIII Ryan MCP ranking for the DR factor: 21-product fab under CONWIP.

MCT			SDCT		
(Dispatching rule)	(hours)		(Dispatching rule)	(hours)	
ESD	495.6		Wt(PT+WINQ)/XF	89.2	
FCFS	495.9		FCFS	90.2	
LWNQ	498.0		ESD	90.8	
Wt(PT+WINQ)/XF	500.2		LWNQ	104.8	
EDD	501.6		CR+SPT	138.6	
(PT+WINQ)/TIS	511.8		(PT+WINQ)/TIS	174.6	
PT/TIS	512.0		PT/TIS	187.5	
CR+SPT	512.7		(PT+WINQ)/XF	215.6	
(PT+WINQ)/XF	542.8		EDD	218.6	
Wt(AT_{Step}-RPT)/XF	560.7		AT-RPT	220.3	
HXF	570.4		Wt(AT_{Step}-RPT)/XF	221.5	
(AT_{Step}-RPT)/XF	573.1		(AT_{Step}-RPT)/XF	229.0	
CR	602.2		CR	229.9	
AT-RPT	605.6		HXF	236.8	

In the 3-product fab under pull, the best rules for both SDCT and MCT were FCFS, ESD, Wt(PT+WINQ)/XF, and LWNQ (Table XIV). As in the 21-product fab, HXF, (AT_{Step}-RPT)/XF, Wt(AT_{Step}-RPT)/XF, and CR were poor for both MCT and SDCT.

In the 21-product fab under push, (AT_{Step}-RPT)/XF) and Wt(PT+WINQ)/XF were the best for both MCT and SDCT while being distinct from FCFS (Table XV). The same performance was seen for MT, SDT, and %Tardy (Table XVI), and far outpaced due-date-based rules such as EDD. In the 3-product fab under push, despite more group separation, 21-product fab trends are seen for MCT, with the top rules of Wt(PT+WINQ)/XF and (AT_{Step}-RPT)/XF), being joined by HXT, (PT+WINQ)/XT, and Wt(AT_{Step}-RPT)/XF. In contrast, SDCT was dominated by AT-RPT. Table XVIII again confirmed the superiority of our new rules for the due-date measures for the 3-product case.

Table XIV. Ryan MCP ranking for the DR factor: 3-product fab under CONWIP.

MCT		SDCT	
(Dispatching rule)	(hours)	(Dispatching rule)	(hours)
EDD	446.7	Wt(PT+WINQ)/XF	44.7
PT/TIS	450.3	ESD	46.8
(PT+WINQ)/TIS	450.3	FCFS	46.8
CR+SPT	450.4	LWNQ	61.1
ESD	451.7	CR+SPT	90.6
FCFS	451.9	EDD	102.9
LWNQ	452.8	(PT+WINQ)/TIS	105.5
Wt(PT+WINQ)/XF	453.5	PT/TIS	114.8
(PT+WINQ)/XF	467.3	(PT+WINQ)/XF	152.0
AT-RPT	531.5	AT-RPT	163.9
CR	566.5	CR	214.6
Wt(AT_{Step}-RPT)/XF	577.8	Wt(AT_{Step}-RPT)/XF	287.8
HXF	582.1	(AT_{Step}-RPT)/XF	298.4
(AT_{Step}-RPT)/XF	583.0	HXF	309.7

Table XV. Ryan MCP ranking for the DR factor: 21-product fab under push.

MCT		SDCT	
(Dispatching rule)	(hours)	(Dispatching rule)	(hours)
Wt(AT_{Step}-RPT)/XF	483.2	(AT_{Step}-RPT)/XF	69.1
Wt(PT+WINQ)/XF	483.7	AT-RPT	72.1
(AT_{Step}-RPT)/XF	488.5	HXF	73.5
(PT+WINQ)/XF	491.6	Wt(AT_{Step}-RPT)/XF	73.7
FCFS	492.9	ESD	74.7
HXF	493.7	Wt(PT+WINQ)/XF	76.0
(PT+WINQ)/TIS	502.3	(PT+WINQ)/XF	85.5
PT/TIS	505.8	(PT+WINQ)/TIS	87.2
LWNQ	507.5	CR	88.6
CR+SPT	511.5	FCFS	91.8
EDD	513.4	PT/TIS	92.7
AT-RPT	513.5	CR+SPT	95.9
ESD	517.2	EDD	97.5
CR	519.2	LWNQ	117.2

D. The 98% Cycle Time Performance Measure

We recorded the 98% cycle time measure, with the actual 98th percentile mean cycle time (Table XIX). The latter's value was found by merging cycle time values from 10 replications, sorting them in ascending order, and finding the 98th percentile value. The 98% cycle time value overestimated the 98th percentile mean cycle time by about 15%.

VI. CONCLUSIONS

A. Summary

Table XX lists the best rules for MCT and SDCT, for combinations of production type and order release. Wt(PT+WINQ)/XF was the most versatile of the 14 rules tested. The simpler (AT_{Step}-RPT)/XF also achieved excellent dual results for MCT and SDCT, even though it was less robust under pull. Both rules were also in the best groups for MT, SDT, and (%Tardy) (Tables XXI and XXII).

Table XVI. Ryan MCP ranking for the DR factor (tardiness measures): 21-product fab under push.

MT		SDT		%Tardy	
(Dispatching rule)	(hours)	(Dispatching rule)	(hours)	(Dispatching rule)	(%)
Wt(AT_{Step}-RPT)/XF	5.6	Wt(AT_{Step}-RPT)/XF	5.5	Wt(AT_{Step}-RPT)/XF	0.32
Wt(PT+WINQ)/XF	9.3	Wt(PT+WINQ)/XF	7.4	AT_{Step}-RPT)/XF	0.70
(AT_{Step}-RPT)/XF	9.9	(AT_{Step}-RPT)/XF	8.5	Wt(PT+WINQ)/XF	0.77
CR+SPT	12.2	HXF	11.3	HXF	3.01
HXF	13.2	CR+SPT	13.5	(PT+WINQ)/XF	5.53
CR	17.1	(PT+WINQ)/XF	15.0	FCFS	10.29
(PT+WINQ)/XF	20.1	CR	17.0	(PT+WINQ)/TIS	11.22
AT-RPT	22.3	AT-RPT	19.3	AT-RPT	11.75
FCFS	23.9	FCFS	20.6	EDD	12.62
ESD	28.9	ESD	23.1	CR+SPT	13.03
EDD	31.9	EDD	25.1	ESD	13.36
(PT+WINQ)/TIS	41.0	(PT+WINQ)/TIS	30.4	PT/TIS	14.41
PT/TIS	42.3	PT/TS	30.8	CR	15.61
LWNQ	83.1	LWNQ	74.3	LWNQ	19.02

Table XVII. Ryan MCP ranking for the DR factor: 3-product fab under push.

MCT		SDCT	
(Dispatching rule)	(hours)	(Dispatching rule)	(hours)
Wt(AT_{Step}-RPT)/XF	434.8	AT-RPT	20.2
Wt(PT+WINQ)/XF	435.7	ESD	22.5
HXF	436.1	FCFS	41.2
(PT+WINQ)/XF	436.2	CR	46.7
(AT_{Step}-RPT)/XF	437.7	HXF	46.8
FCFS	444.6	(AT_{Step}-RPT)/XF	46.9
LWNQ	446.3	(PT+WINQ)/TIS	49.8
(PT+WINQ)/TIS	448.8	Wt(AT_{Step}-RPT)/XF	51.2
PT/TIS	451.5	LWNQ	51.7
CR+SPT	454.0	Wt(PT+WINQ)/XF	53.7
CR	463.6	(PT+WINQ)/XF	60.3
EDD	465.0	EDD	60.8
AT-RPT	471.8	CR+SPT	64.6
ESD	474.5	PT/TS	65.7

Table XVIII. Ryan MCP ranking for the DR factor (tardiness measures): 3-product fab under push.

MT		SDT		%Tardy	
(Dispatching rule)	(hours)	(Dispatching rule)	(hours)	(Dispatching rule)	(%)
Wt(PT+WINQ)/XF	0.0	Wt(PT+WINQ)/XF	0.0	Wt(PT+WINQ)/XF	0.00
AT_{Step}-RPT)/XF	0.0	AT_{Step}-RPT)/XF	0.0	AT_{Step}-RPT)/XF	0.00
(PT+WINQ)/XF	0.0	(PT+WINQ)/XF	0.0	(PT+WINQ)/XF	0.00
Wt(AT_{Step}-RPT)/XF	0.0	Wt(AT_{Step}-RPT)/XF	0.0	Wt(AT_{Step}-RPT)/XF	0.00
HXF	0.0	HXF	0.0	HXF	0.00
EDD	3.2	EDD	2.0	EDD	0.01
CR	6.5	CR+SPT	5.0	FCFS	0.02
CR+SPT	6.9	(PT+WINQ)/TIS	5.1	(PT+WINQ)/TIS	0.04
FCFS	9.7	FCFS	5.9	CR+SPT	0.06
(PT+WINQ)/TIS	10.0	CR	7.7	PT/TIS	0.13
ESD	11.4	PT/TIS	9.6	CR	0.16
AT-RPT	11.6	ESD	10.8	LWNQ	0.90
PT/TIS	16.8	AT-RPT	11.5	ESD	1.52
LWNQ	28.3	LWNQ	28.0	AT-RPT	1.67

Table XIX 98% cycle time versus 98th percentile of cycle time.

Experimental assumptions and results	
Release policy	Push
Number of products	21
Dispatching rule	FCFS
Run Length (years)	5
Warm-up (years)	1
Number of independent replications	10
Mean cycle time (hours)	492.91 ($\pm$ 2.43)
Standard deviation of cycle time (hours)	91.83 ($\pm$ 2.66)
98% cycle time (hours)	768.4
98th percentile of cycle time (hours)	662.21

B. Past Research Retrospective

AT-RPT [33],[27] and ESD confirmed their SDCT edge. Wt(PT+WINQ)/XF however broke their monopoly. LWNQ and similar WIP-balancing rules [10],[34], may only be recommended under pull policies. PT/TIS and (PT+WINQ)/TIS [27] were proposed to dually address MCT and SDCT. Their performance however, was mid-range. No due-date based rule (CR, CR+SPT, EDD) outpaced FCFS for MCT or SDCT. This contrasts the reported extensive usage of CR in fabs [35]-[37], even though, its performance might improve under loose due dates, and/or lighter loading levels. CONWIP was found to lessen the effect of dispatching on MCT [33]. We

found that the benefits of including certain lot or fab-status attributes are mostly applicable in the push case. In fact, the good performance of the EDD and ESD under CONWIP for MCT, run counter to the way we understood the basics of composite rule design.

C. Contributions of This Work

Besides rigorous fab modeling and statistical analysis, composite rule design trends were adapted to the fab context. Original use of the multiplier of theoretical cycle time (XF) as a priority index attribute *and* dynamic system-based scaling parameter; resulted in new versatile rules for the multiple objectives of MCT, SDCT, MT, SDT, and %Tardy. Achieving a dual objective for just MCT and SDCT is not an easy task, as some researchers custom-designed separate rules for each [33]. Push outperformed CONWIP in both the original ASIC fab (for MCT and SDCT), and the 3-product fab (for SDCT). As for MCT in the 3-product fab, pull improved for a tie with push. Up to this study, the effect of dispatching rules on CONWIP was not fully understood. In general, most rules failed to outpace FCFS in CONWIP, thus supporting the FCFS vision in [15]. FCFS was also particularly insensitive to OR. Finally. the few available CONWIP studies for multiple products used a single factory-wide WIP-level, and careful sequencing of the released product types [38]. Building on the ideas in [39], we explored a product-specific WIP implementation in a large, unreliable, and batching-prone reentrant fab.

D. Recommendations for Future Research

Rework, yield, and material handling can be added to fab modeling; while batching policy, lot size, and due date tightness are worthy experimental factors. Further tests in fabs and job shops, will likely confirm the potential of the new rules. Future research may also explore the effect of routing and priority attributes on separate product performance. In implementing CONWIP, one can either look at using fab-wide WIP levels, or the optimization of separate product WIP levels. In composite rule design, XF was encouraging as a dynamic scaling parameter, and should be further explored. Further, PT and WINQ's potential variations include total remaining processing time (RPT), and total work content in downstream queues in the route.

Table XX. Best rules for cycle time measures as sorted by the Ryan MCP.

Factory type x Release Policy	MCT	SDCT
21-product x CONWIP	**Wt(PT+WINQ)/XF**, FCFS, ESD, LWNQ, EDD	**Wt(PT+WINQ)/XF**, FCFS, ESD
3-product x CONWIP	**Wt(PT+WINQ)/XF**, FCFS, ESD, LWNQ, EDD, (PT+WINQ)/TIS, (PT+WINQ)/XF, PT/TIS, CR+SPT, At-RPT	**Wt(PT+WINQ)/XF**, FCFS, ESD, LWNQ
21-product x Push	**Wt(PT+WINQ)/XF**, **(AT_{Step}-RPT)/XF**, Wt(ATStep-RPT)/XF	**Wt(PT+WINQ)/XF**, **(AT_{Step}-RPT)/XF**, Wt(ATStep-RPT)/XF, ESD, AT-RPT, HXF
3-product x Push	**Wt(PT+WINQ)/XF**, **(AT_{Step}-RPT)/XF**, Wt(ATStep-RPT)/XF, (PT+WINQ)/XF, HXF	AT-RPT

Table XXI. Best rules for due-date measures as sorted by the Ryan MCP (21-product fab under push).

Factory type	MT	SDT	%Tardy
21-product	**Wt(PT+WINQ)/XF, (ATStep-RPT)/XF,** Wt(AT_{Step}-RPT)/XF, HXF, CR+SPT	**Wt(PT+WINQ)/XF, (ATStep-RPT)/XF,** Wt(AT_{Step}-RPT)/XF, HXF	**Wt(PT+WINQ)/XF, (ATStep-RPT)/XF,** Wt(AT_{Step}-RPT)/XF, HXF, (PT+WINQ)/XF

Table XXII. Dispatching rules with 100% on-time performance (3-product fab under push).

Factory type	MT	SDT	%Tardy
3-product	**Wt(PT+WINQ)/XF, (ATStep-RPT)/XF,** Wt(AT_{Step}-RPT)/XF, HXF, (PT+WINQ)/XF	**Wt(PT+WINQ)/XF, (ATStep-RPT)/XF,** Wt(AT_{Step}-RPT)/XF, HXF, (PT+WINQ)/XF	**Wt(PT+WINQ)/XF, (ATStep-RPT)/XF,** Wt(AT_{Step}-RPT)/XF, HXF, (PT+WINQ)/XF

Table XXIII. List of acronyms

Abbreviation	Description
AT	Arrival Time
ASIC	Application Specific Integrated Circuit
CI	Confidence Interval
CONWIP	CONstant Work IN Process
CR	Critical Ratio
DR	Dispatching Rule
EDD	Earliest Due Date
ESD	Earliest Start Date
FCFS	First Come First Serve
HXF	Highest X Factor
LWNQ	Least Work in Next Queue
MBS	Minimum Batch Size
MCP	Mean Comparison Procedure
MCT	Mean Cycle Time
MRP	Material Requirements Planning
MRP II	Manufacturing Resources Planning
MT	Mean Tardiness
NP	Number of Products
OR	Order Release
PT	Processing Time
RPT	Remaining Processing Time
RR	Raghu & Rajendran's [56] (Dispatching Rule)
SDCT	Standard Deviation of Cycle Time
SDT	Standard Deviation of Tardiness
SPT	Shortest Processing Time
SRPT	Shortest Remaining Processing Time
TIS	Time in the System
WINQ	Work in Next Queue
WIP	Work in Process
XF	X Factor (or "multiplier of theoretical processing time")

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BIOGRAPHIES

Nizar Bahaji was born in Morocco. He received the B.S. degree in electrical engineering from Milwaukee School of Engineering, the M.A. degree in international relations from the International University of Japan, and the M.S. degree in industrial engineering from Louisiana State University.

He is a Simulation Engineer with SK Daifuku Corporation, Salt Lake City, UT. His research interests include automated materials handling systems.

Michael Kuhl received the B.S. degree in industrial engineering from Bradley University, and the M.S. and Ph.D. degrees from North Carolina State University, respectively in industrial engineering/operations research and industrial engineering.

He is an Assistant Professor at Rochester Institute of Technology. His research interests are: simulation, systems engineering, operations research, and production control.