Investigation of ALD Dielectrics in Silicon Capacitors

Enri Marini

***Abstract*—The goal of this analysis is to scale aluminum oxide films deposited by ALD for use in transistor fabrication with silicon and silicon-germanium substrates and the two metals offer varying work functions for gate control on the transistor level. MOS capacitors were fabricated on six-inch silicon substrates consisting of aluminum-oxide (Al_2O_3) as the dielectric and aluminum as the gate metal. The Al_2O_3 was deposited using atomic layer deposition (ALD) with thicknesses of 15nm and 20nm, while the aluminum gate metal was DC sputter deposited containing thickness of approximately 1200$\mathring{A}$. Capacitance values were measured in order to back-calculate the relative permittivity of Al_2O_3. The observed experimental relative permittivity of Al_2O_3 of ϵ_r = 8.83$\pm$0.55 matched reported values in literature of ϵ_r = 9.0$\pm$0.1. Future works for this project include testing different gate metals and dielectric materials for capacitance-voltage response.**

I. Introduction

Silicon-based CMOS technology currently dominates the semiconductor industry given its great scaling capability and incorporation of silicon dioxide as the dielectric interface. Planar scaling of traditional CMOS technology is becoming more difficult as higher operating speeds and lower power consumption are sought after. Compound substrates and stoichiometric channel MOSFET devices have been of great interest as they can achieve similar operating frequencies and current densities without many of the processing issues as traditional planar CMOS devices.

II. Theory

A. Sputtering and Sheet Resistance

Sputtering is a method of PVD that utilizes momentum transfer to eject atoms from a target material onto the substrate. Sputtering occurs whenever a particle strikes a surface with enough energy to dislodge an atom from the surface. The sputter yield (S) is the ratio of the number of emitted particles per incident particle. Sputtering can occur for any incident species, including atoms, ions, electrons, photons, and neutrals, as well as macro-scale things like molecules and molecular ions. Sputtering uses ion bombardment, which come as either Ar^+ or Kr^+ molecular ions, such as N_2^+ and O_2^+. Physical sputtering is categorized by the energy range of the ions used to sputter. There are four ranges and they are described as follows: 1) For very low energy ranges where incident ions have a few eV to roughly $\sim$40eV, there is little sputtering. The minimum ion energy for sputtering is the binding energy of the weakest-bound surface atom. 2) In the knock-on energy regime, which ranges from 40eV$\sim$1000eV, has more than enough energy to dislodge hundreds of atoms, however this regime is erratic and depends on where the incident particle hits. 3) Collision-cascade sputtering operates at ion energies of 1keV$\sim$50keV, where the incident particle has sufficient energy to break all of the bonds between atoms in a spherical region around the incident site. This regime has generally higher yields than the knock-on energy regime. 4) Finally, the high energy implant operates at 50keV and above, where the ion is able to travel into the bulk of the material before depositing its energy. This creates damage deep into the material as penetration distances range in the micron scale. Very little to no sputtering occurs within this regime because the energy is deposited so far away from the surface [1].

$$\rho_s = \frac{\pi}{\ln 2} \cdot \frac{V}{I} = \frac{\rho}{t} \tag{1}$$

In equation 1, voltage refers to a DC potential and current refers to a DC current. Sheet resistance is denoted as ρ_s and expressed in units of [$\Omega/\square$], [Ω/square], or [Ω/sq.]. This relation of sheet resistance is useful for calculating the experimental value of resistivity (ρ), which is expressed in units of [Ω·cm]. Film thickness is denoted by (t) and expressed in variable units. Film thickness and sheet resistance measurements are obtained, which allows for the derivation of an experimental value of resistivity of the material. There is a direct relationship between thickness and the given cross-sectional area of current flow in the film. The bulk resistance of a rectangular shaped section of film is shown by equation 2 [1].

$$R = \frac{\rho L}{tW} \tag{2}$$

where R is the resistance, L is the length of the film, and W is the width of the film. Equation 3 shows the relation resistivity of a thin film to its respective hole mobility (μ_p), electron mobility (μ_n), and carrier concentration. Resistivity is a verifiable material property to which experimental data can be used to compare to, regardless if the film in question is thin or bulk material [7]. Literature reports aluminum resistivity $\sim 2.70\times10^{-8}\Omega$·m at room temperature and molybdenum has a reported resistivity of $\sim 5.57\times10^{-8}\Omega$·m at room temperature [2][3]. As equation 3 shows, resistivity is an intrinsic property dictated by the temperature that results from the mobility and carrier concentration.

$$\rho = \frac{1}{q(\mu_n n + \mu_p p)} \tag{3}$$

The four-point probe is a tool that measures sheet resistance of thin films. Its four probes, assumed to be equally spaced,

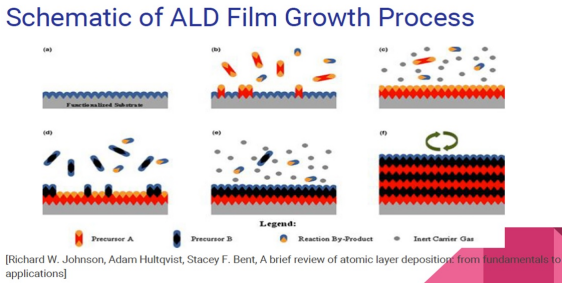


Fig. 1: Process flow for deposition of ALD films [4].

run a current onto the sample and read the current that is sampled back from the wafer being measured. Another key assumption of the four-point probe is that the probe spacing (s), when compared to the diameter (d) and width (w) of the wafer being measured, is such that s << d and s << w. In the case where w ≈ s, a correction factor (k) is added to the resistivity relation, so that the new resistivity relation becomes $\rho = \frac{2\pi s \cdot \frac{V}{I}}{k}$ [7].

B. Atomic Layer Deposition Overview

ALD is a technique used for depositing thin films and offers very high conformal coating. Prior to its current name, the technique of ALD was first known as atomic layer epitaxy (ALE) [4][7]. Tuomo Suntola was able to demonstrate the first application of ALE in 1974, and in 1977, a patent was launched by Tuomo Suntola and Jorma Antson for inventing a method for using ALE to produce compound thin films [4][7].

The current techniques for thin film deposition include chemical vapor deposition (CVD) and physical vapor deposition (PVD), where ALD is a CVD method of deposition. The two main reasons for why ALD is superior to all other techniques is due to the conformal quality of the films deposited and the precision control over the film thickness, which is in the single digit Angstrom level. ALD is carried out at temperatures less than 300°C. Aspect ratio (AR), which is the ratio of an objects height to its width, is crucial in current scaling and very large scale integration (VLSI) trends. An example of AR playing a crucial role is in stacked DRAM capacitors [8]. In order to access a bit-line, a voltage difference in the hundreds of millivolts (≈150mV) must be applied to charge the capacitor which accesses that memory array [8]. Supply voltages are less than 1V for DRAM and DRAM technology requires capacitance values as low as 10^{-15}F. To achieve such low capacitor values, the solution is to create tall structures. The takeaway from this examples is the definition of the height and width geometries must be of high quality, which highlights several process challenges [8]. These challenges include etching the geometries of such structures, filling these structures without creating a pinch-off or an air-gap, and ensuring physical integrity so that these structures do not collapse [8]. As shown in Figure 1, the ALD process goes as follows: In part a), the substrate is treated in the appropriate conditions by being pumped down to vacuum levels less than 1 Torr. In part b), a precursor is introduced and reacts with the surface of the substrate. Part c) shows excess precursor and reaction byproducts being purged via an inert carrier gas (such as N_2). Part d) shows a second precursor being introduced via controlled pulses. Part e) shows that after the film is grown to a desired thickness with the second precursor, any excess precursor and reaction byproducts are remove with an inert carrier gas. Part f) shows that then steps a) - e) are repeated until the desired film stack is achieved.

C. Applications of ALD Films

	K	Gap (eV)	CB offset (eV)
Si		1.1	
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8 (not ALD)
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8
La_2O_3	30	6	2.3
Y_2O_3	15	6	2.3
a-$LaAlO_3$	30	5.6	1.8

TABLE I: Static dielectric constants, experimental band gap, and conduction band (CB) offset measured on a silicon substrate [6].

One of the largest issues facing all quantum well (QW) MOSFET devices is that they use a Schottky gate and experience high gate leakage. A Schottky gate is a gate that has a metal-semiconductor (MS) junction. Current does not flow directly through the gate and instead, the Schottky effect allows for a lowering of the energy barrier at the MS junction via an electric field. This leakage current is uncontrolled current that flows through parts of the device that should not contain current, such as the gate oxide [8]. This is where aluminum oxide comes into play. Having a high breakdown voltage in the range of 5-30MV/cm makes aluminum oxide an excellent dielectric material for short channel devices, which suffer from degradation effects as a result of fringing electric fields. The high bandgap of 9eV allows aluminum oxide to have less oxide traps, unlike HfO_2 which has a lower bandgap of 5.8eV. Aluminum oxide has high thermal stability due to its melting point of approximately 1,710°C. Having such a high melting point helps make it a viable material during drain/source implant steps. It can act as a masking film and allows for subsequent processing to electrically activate the implanted ions and repair lattice damage by means of a rapid thermal process (RTP) anneal, as RTP quickly ramps up to temperatures of 1000°C and above.

Table 1 shows a list of various dielectric materials and their respective relative permittivity and bandgaps. The MOS capacitor stands for metal–oxide–semiconductor capacitor,

which is made up of a semiconductor substrate, a dielectric film, and a metal electrode called the gate. MOS capacitors have varying modes of operation that depend on the doping concentrations in the substrate. The capacitance of the MOS structure depends on the voltage on the gate with respect to the body. The regimes are described by what is happening to the semiconductor surface. Flatband is the condition where the energy band of the substrate is flat at the semiconductor–dielectric interface. This condition is achieved by applying a negative voltage for a p–type substrate and a positive voltage for an n–type substrate. In accumulation, carriers of the same type as the body accumulate at the surface. In depletion, the surface is devoid of any carriers leaving only a space charge or depletion layer. Inversion is when carriers of the opposite type from the body aggregate at the surface to alter the conductivity type. When an applied positive gate voltage is larger than the flatband voltage, it induces positive charge on the gate and negative charge in the semiconductor. The only negative charges available are electrons and they accumulate at the surface. When the electron concentration at the surface is above the bulk value, this leads to a condition referred to as surface accumulation. Under flatband condition, there is no charge on the gate electrodes of the capacitor, therefore there is no electric field across the oxide. The oxide capacitance can be modeled several ways and in this project, it was taken to be modeled after a parallel plate system. The oxide capacitance is expressed in units of [F/cm^2] and is strictly a function of the relative permittivity of the material as well as its thickness. This relation is given in equation 4. Once oscilloscope measurements are performed to obtain capacitance values, equation 5 can be used to back out an experimental observation of the relative permittivity. Within this equation, since experimental values are used, there exist uncertainty in the measurements and therefore standard deviations and errors must be included in reported values.

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \tag{4}$$

$$\epsilon_r = \frac{Cd}{A\epsilon_0} \tag{5}$$

III. Experimental Procedure

The process flow for manufacturing the MOS capacitors is as follows:

1) Obtain bare silicon substrates six inches in diameter degenerately doped n^+ with a2 phosphorous with doping concentration of 10^{19}cm^{-3}
2) Deposit Al_2O_3 using ALD using trimethylaluminum (TMA) and water as the precursors and N_2 as the purging gas. Two thicknesses were targeted, 15nm and 20nm. The recipe for the 15nm target thickness uses 150 purge cycles with a 15 minute settling time and the 20nm target thickness recipe uses 200 purge cycles with a 15 minute settling time. The inner and outer ring temperatures must be set to 200°C for both the 15nm and 20nm thickness recipes.
3) Static DC sputter deposit gate metal. Each sample only had one metal layer; this is not to be confused with using multiple metal layers in a single sample. The recipe for molybdenum was to use a 5 minute static sputter deposition on the CVC 601 with a power of 600W, a voltage of 348V, current of 1.72A, a base pressure of 2.2×10^{-6} Torr, and a sputter pressure of 5mTorr. A target burn–in was done prior to the deposition on the molybdenum target using 1000W for the power at a time of 2 minutes. For the aluminum, a static DC sputter deposition was done using a power of 300W, voltage of 385V, current of 0.81A, deposition time of 5 minutes, base pressure of 1.5×10^{-6} Torr, and sputter pressure of 6mTorr. A target burn–in was done prior to depositing with a power of 2000W at for 2 minutes.
4) Samples were then coated using FujiFilm HPR504 positive photoresist on the SVG Wafer Track.
5) Lithography was done using the GCA stepper (g–line wavelength) to pattern the metal. The reticle used was the 'CV MASK' and the exposure recipe used was 'CVTEST06'. A ten–by–ten array (rows by column) was set. However, the size of the array does not matter – a larger array was chosen for the sake of having more sites to measure during capacitance testing.
6) The patterned metal was then etched. For aluminum, a wet bath using the Fuji 16:1:1:2 mixture was used, which consists of nitric acid, acetic acid, phosphoric acid, and water respectively. Etch rates will depend on thickness of metal. Once etching of aluminum is complete, a spin–rinse–dry (SRD) was done. For etching molybdenum, sulfur hexafluoride (SF_6) was used on the Drytek Quad. Etch time will depend on thickness of metal and an etch rate should be calculated on non–product samples before assuming an etch rate.
7) Once the patterned metal is etched, the remaining photoresist is stripped using the GaSonics Aura 1000 asher tool using oxygen plasma.
8) Capacitance and voltage responses are then characterized by measuring individual die of varying areas on each finished product using an oscilloscope tool that was set to sweep voltages from -1V to 1V and collect capacitance values. Only the peak capacitance value out of this range was of interest to perform average capacitance calculations and include marginal errors. This process was repeated throughout multiple sites on the wafer on die areas of 0.001cm^2 and 0.002cm^2.

Thickness measurements of the deposited aluminum and molybdenum films were performed using the Tencor P2 Profilometer. The Tencor P2 Profilometer is a long scan profilometer that is capable of measuring step heights, stress, and surface roughness by moving a stylus over a defined step in the film to be measured. This step is artificially created by placing a strip of tape that covers the side that will have the film deposited on [7]. The glass samples used in this experiment were rectangular, so the strip of tape was placed halfway across the length of the sample. The tape was notched on the ends to allow for easy removal after the deposition for measurements and the peeling of the tape was done manually to ensure that a clean peel was performed to have a clear

and defined step in the film. The tape was removed prior to placing the sample in the tool for measuring. A profilometer measurement is considered a destructive test in that scratching can occur during the process of the stylus drawing over the film being measured [7]. Calibration was needed for the machine to differentiate between a zero reference point since the stylus begins scanning laterally on top of the film. The substrate was set as the zero point. Different parts of the film were analyzed to test for potential gradients within the sample. The thin film thickness was then calculated by taking the difference of the measured film thickness and the thickness of the bare substrate. A visual representation was outputted by the tool showing the stylus running across the film until the point it transitioned into bare glass substrate [7].

Sheet resistance measurements were done using two tools; the first being a manual 4-point probe with manual voltage and current adjustments and the second being the CDE Res Map. The manual 4-point probe system was used simply to verify measurements. With the CDE Res Map tool, a 25-point probe test was used, wherein the tool drops its probes onto select positions defined by the process recipe selected. The tool maneuvers its probes radially throughout the sample, which is why it is important that the correct process recipe is selected as to avoid measuring an area that either does not have film or is completely off of the substrate. Sheet resistance measurements should be redone if metrics like the standard deviation and/or good to bad measured points ratio are skewed [7]. Ellipsometry was used to perform thickness measurements on the aluminum oxide film. The WVASE Ellipsometer was the tool used to perform these measurements. When performing thickness measurements, it is important to select the proper simulation file to base measurements, as there are several recipes for different materials in the tools' recipe catalog. The recipe used was "al2o3-thin-film.mat".

IV. Discussion of Results

As the power used to sputter aluminum decreased, the average aluminum film thickness decreased, thereby making the sputter power and film thickness directly associated. No trend was observed in the sheet resistance non-uniformity as a function of the deposition power and no trend was observed in the film thickness non-uniformity as a function of the deposition power. A higher voltage would give the ions in the plasma more energy, and a higher current means that more ions are being moved towards the target. Sputter theory says that as the atomic mass of the target material increases, sputter yield should decrease. This means that the heavier the element, there should be less material being sputtered for the same power. Mass is not the only factor for sputter yield. Geometry of the target should be taken into account. This is because there is a optimum angle of incidence for the incoming ion. "Race tracks" can form on targets, changing the sputter yield of the target [7]. The film resistivity values remained the same across all films and this is to be expected as resistivity is a material property and should not change no matter the technique used to deposit the film. Resistivity does, however, change with temperature and there is research showing experimental curves of resistivity of elements with respect to temperature.

Due to the samples used being degenerately doped, the capacitance and voltage response curve did not follow the same smooth transition as non–degenerately doped samples do. If the applied gate voltage is lowered below the threshold voltage, the semiconductor surface inverts its conduction type from n–type to p–type (and vice versa), but this particular situation, the conduction type would have to be inverted from n^+. The threshold voltage in these samples would be when the surface layer has more holes attracted to the surface than the number of electrons that existed at the surface during flatband. Starting at flatband, as the gate voltage is lowered, negative mobile carriers are pushed away from the silicon–dielectric interface, leaving behind a positive space charge region which is called the depletion layer. Although the assumption that the dielectric layer is devoid of all mobile carriers is used for approximate calculations, what actually happens is that the density of electrons decreases exponentially from the surface going into the bulk. In the relative permittivity calculations, error in the die area was excluded and assumed to be constant and true to the respective values read on the mask, which were 0.001cm^2 and 0.002cm^2. This definitely played a role in the standard deviation of the relative permittivity calculations as a wet etch technique was used. Non–uniformity in the etch was due to variations in the acids and manner in which the wafers were loaded into the wet bath.

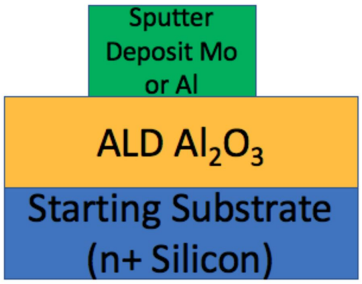


Fig. 2: Material stack for finished MOS capacitor. The silicon substrate is six-inches in diameter and is degeneratively doped (n+) with phosphorus, with doping of 10^{19}cm^{-3}. The dielectric material is aluminum oxide and varies in thickness of either 15nm and 20nm. The gate metal is aluminum that was DC sputtered.

V. Conclusion

Conformality of ALD deposited films is a critical factor in why ALD is superior to existing techniques of thin film deposition by CVD and PVD. As device structures become smaller and more geometrically complex, with techniques such as AR being adopted to meet these demands, thickness control also becomes a key factor that ALD excels in by offering control at the Angstrom level. ALD does not champion in all categories, as it takes long periods of time to complete each cycle of film growth and moves at a monolayer pace and consist of growth rates of 100nm/hr. Proper chemistry also plays a crucial factor in ALD processing, as certain materials of high importance in contemporary industry, such as Si_3N_4, Si, and Ge, cannot be deposited in a cost-effective

	Hand-calculated Capacitance	Ideal ϵ_r (no units)	Experimental Capacitance	Experimental ϵ_r (no units)
15nm oxide with Area = 0.001cm^2	531 pF	9.00	489 pF ± 58 pF	8.64 ± 1.03
20nm oxide with Area = 0.001cm^2	395 pF	9.00	367 pF ± 34 pF	8.45 ± 0.78
15nm oxide with Area = 0.002cm^2	1063 pF	9.00	1001 pF ± 105 pF	8.84 ± 0.93
20nm oxide with Area = 0.002cm^2	797 pF	9.00	767 pF ± 48 pF	8.83 ± 0.55

TABLE II: Capacitance calculations using the parallel plate capacitance model listed in equation 4. The ideal hand calculated capacitance values were obtained by assuming no deviation in any of the parameters (thickness of dielectric, die area, relative permittivity), while the experimental calculations of capacitance were obtained using an oscilloscope. The observed relative permittivity was then backed out using equation 5.

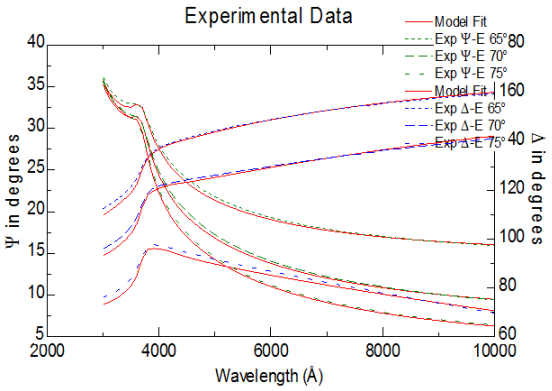
	15nm CD Deposition	20nm CD Deposition
Experimental Thickness	15.642nm ± 0.105nm	20.391nm ± 0.115nm
Experimental Refractive Index	1.744 ± 0.010	1.613 ± 0.010

TABLE III: Thickness and refractive index measurements using ellipsometry of the targeted 15nm and 20nm thick aluminum oxide. A Cauchy model was used to obtain precise measurements by assuming a fit to the expected refractive index of aluminum oxide as reported in literature, which is n=1.8 for wavelengths of 1000$\mathring{A}$ to 20,000$\mathring{A}$ [8].

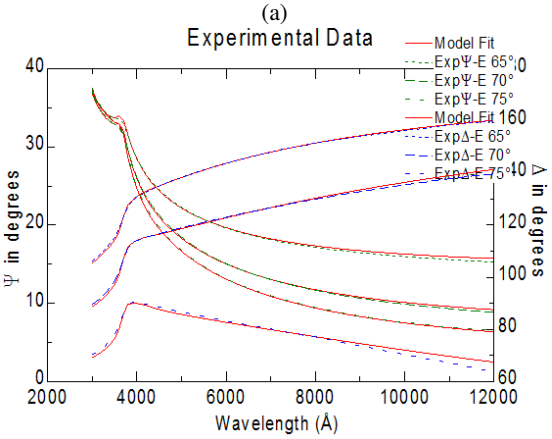
method [8]. In the relative permittivity calculations, error in the die area was excluded and assumed to be constant and true to their respective values read on the mask, which were 0.001cm^2 and 0.002cm^2. This definitely played a role in the standard deviation of the relative permittivity calculations as a wet etch technique was used and non–uniformity in the etch due to varying concentrations of the acids and manner in which the wafers were loaded into the wet bath. Furthermore, thickness non–uniformity of the metal and dielectric thickness variation impact capacitance results. Nevertheless, the sample that most closely resembled reported ϵ_r values of aluminum oxide with the lowest standard error was the aluminum gate MOS capacitor, which has a dielectric thickness of 20nm that is measured on the die area of 0.002cm^2. Future work would include reviewing different gate metals and dielectric materials to characterize capacitance–voltage responses as well as scaling these processes for use in MOSFET manufacturing.

	Molybdenum	Aluminum	Units
Measurement	**Value**	**Value**	
Avg. Thickness	3785	1635	[Å]
Thickness Non-Uniformity	18.438	10.326	[%]
Sheet resistance (ρs)	563.16	347.52	[mΩ/square]
Sheet resistance Non-Uniformity (NU)	8.011	9.546	[%]
Resistivity (ρ)	2.223E-07	5.771E-07	[Ω·m]
Good sites : Bad Sites	49:52	51:52	None

TABLE IV: Average thickness, thickness non-uniformity, sheet resistance, sheet resistance non-uniformity, and resistivity measurements of aluminum and molybdenum, which were used as the gate metals used in the MOS capacitor.



(a)



(b)

Fig. 3: Ellipsometry measurements using the WVASE ellipsometer to measure the aluminum oxide after being deposited using ALD on a bare silicon substrate. Figure (a) on the left shows the matching between the simulated fit of the Cauchy model (solid red line) to the experimental fit (dashed blue line) based on fitting a fixed refractive index of n=1.8. Figure (b) on the right shows the matching between the simulated fit of the Cauchy model (solid red line) to the experimental fit (dashed blue line) based on fitting a fixed refractive index of n=1.8. Both the simulated and experimental observations closely match, as seen by the overlaying of the red and blue lines.

VI. Acknowledgements

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Enri Marini (B.S. RIT 17') is a 5th year undergraduate student at the Rochester Institute of Technology in the Microelectronics Engineering program. During his undergraduate degree, Enri has had the opportunity to work at several places. This past summer 2017, Enri worked as a Lithography Engineer with L3 Communications in Mason, OH, where he was involved with improving process yields for their focal plane array (FPA) technology. Two years ago (2015), Enri worked with IBM as a Procurement Engineer in their Memory Technology division, overseeing the quality and acquisitions of DRAM, Flash, and SSD technology used in IBM enterprise storage systems. Three years ago (2014), Enri conducted research sponsored by a National Science Foundation (NSF) grant on Esaki tunnel diodes, where he created a design of experiments (DOE) to improve peak-to-valley current ratios of InGaAs diode samples of varying critical dimensions.

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