2003

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Recommended Citation
Ozbas, Murat; Patru, Dorin; and Mukund, P.R., "Power supply noise coupling in a standard voltage reference circuit" (2003). Accessed from http://scholarworks.rit.edu/other/497

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Power Supply Noise Coupling in a Standard Voltage Reference Circuit

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Abstract—Power supply noise (PSN) coupling represents a challenge in the design of current and future analog and mixed-signal circuits. This paper studies the impact of PSN coupling on a key analog circuit building block: a voltage reference. A model representing the amount of noise coupling in the frequency domain is developed and verified through simulations. A design solution for increasing high frequency PSN rejection is identified and evaluated. Finally, the effect of technology scaling on PSN is studied in two successive CMOS processes.

I. INTRODUCTION
The precision achievable with respect to temperature, process, and supply of a voltage reference is very critical to the performance of many analog and RF circuits. Voltage references that deviate from their expected DC values can produce undesirable effects such as bit errors in analog-to-digital converters, non-linearity in RF mixers and low-noise amplifiers (LNA) [4].

Circuit design techniques have been developed to provide nearly zero or small DC variations with respect to each of the three error generating factors: temperature, process, and supply. For example, a bandgap reference is employed to produce a reference with a theoretically zero temperature coefficient (TC) [1]. Where a bandgap reference cannot be used, circuits that are proportional to absolute temperature (PTAT) are used instead. PTAT references provide a reference where the variation with respect to temperature is well characterized. In order to reduce the effects of process variations, transistors with large areas are used to provide better matching. For added precision, post-processing steps, such as laser trimming, may be incorporated into the fabrication of the final chip. As will be shown, at low frequencies references are relatively independent of power supply variations. However, high frequency noise can more easily couple into the circuits seriously degrading signal integrity [2].

In modern system-on-a-chip (SoC) designs, radio-frequency (RF), analog, and digital circuits reside in a common package. In order to reduce the coupling of digital switching noise (dI/dT noise) onto the analog power supply, separate power supply planes are used for analog and digital circuits. By decoupling the two, switching noise coupling is further reduced. The RF and analog portions of the chip however, may still share a common supply. High frequency noise components from RF circuits can couple onto the analog power supply. Voltage references, which share the same supply, can be greatly effected by these high frequency noise sources.

With continued scaling of supply voltages and increased integration, PSN becomes a major design concern for reference circuits [1], [3]. Based on a standard voltage reference circuit, this paper provides an in depth analysis of PSN coupling.

The voltage reference is described in Section II. In Section III, a theoretical expression modeling supply noise rejection is derived. Section IV compares how supply noise scales across different CMOS process technologies.

II. CIRCUIT DESCRIPTION
The circuit shown in Fig. 1 can be used as either a PTAT voltage or current reference [4]. A current reference would be created if R2 is removed. For the purpose of analyzing PSN coupling however, this circuit will be treated as a voltage reference.

The current produced by M1, in branch 1, is mirrored to both branch 2 and branch 3. Branch 2 is the middle branch and 3 is the right most branch. Transistors M4, M5, and M8 are identical in size, producing equal currents in all three branches. Resistor R1 produces VGS1, which sets the current in branch 1 and branch 2. Equation 1 shows that theoretically VGS1 is completely independent of VDD, but still a function of process parameters. Process variations will be neglected in this analysis. Finally, VREF is created by mirroring the same current to branch 3, and dropping it across a resistor, R2.

\[
I_2 R_1 = V_{GS1} = V_{TN} + \frac{2I_1}{\mu_n C_{ox} \left(\frac{W}{L}\right)}
\]
Fig. 1. Threshold voltage referenced self-biasing reference circuit.

Since the current in branch 3 is equivalent to the current in branch 2, (1) and (2) can be combined to produce the result obtained in (3). As a first order approximation this result suggests that variations in $V_{DD}$ will not effect the reference voltage.

$$V_{REF} = I_3 R_2$$

(2)

$$V_{REF} = V_{GS1} \left( \frac{R_2}{R_1} \right)$$

(3)

Further analysis however, will show that low and high frequency noise components can couple from external sources through $V_{DD}$ and onto $V_{REF}$. An approximate model of the expected PSN coupling is derived in the following section.

III. NOISE COUPLING MODEL

A. Derivation of Model

The purpose of developing a model for this reference is to extract the transistor parameters that have the greatest effect on noise coupling. Knowledge of the most critical transistor parameters would allow a circuit designer to make the necessary tradeoffs for optimal PSN rejection.

In order to develop a model of the noise coupled from the power supply to $V_{REF}$, small-signal equivalent circuits are used and a few approximations are made.

The first approximation relates to the noise coupled onto nodes $V_1$ and $V_2$, from Fig. 1. In order to determine the amount of noise coupled from the supply to both $V_1$ and $V_2$, branch 2 is analyzed with branch 1 and 3 removed. The low frequency small-signal equivalent circuit of branch 2 is shown in Fig. 2.

$M_3$ and $M_6$ are both diode-connected transistors; therefore, their small-signal equivalent reduces to a resistor with a value of $1/g_{m}$. Since this approximation is made for low frequencies, it is assumed that the gate of $M_2$ is at ac ground. Equations (4) and (5) represent the gain of the PSN ($V_N$) to nodes $V_1$ and $V_2$, respectively. When real values for the small-signal parameters are substituted in, both expressions

$$V_1 = \frac{g_{me}[x(g_m + 1/r_{o2}) - R_1(g_{m2} + 1/r_{o2})]}{x(g_m + 1/r_{o2}) - R(g_{m2} + 1/r_{o2})(g_{m} + g_{me}) - x(g_{m2})^2}$$

(4)

$$\frac{V_2}{V_N} = \left[ \frac{V_1}{V_N} \right] \left[ \frac{x(g_m)}{x(g_m + 1/r_{o2}) - R(g_{m2} + 1/r_{o2})} \right]$$

(5)

reduce to approximately 1. In other words, noise on the power supply ($V_N$) couples directly to nodes $V_1$ and $V_2$ in its entirety. This result was obtained for low frequencies, but simulations indicate that this approximation is also valid for high frequencies. This allows branch 3 to be analyzed independently from the rest of the circuit. By isolating branch 3 and using the low frequency approximation at $V_1$ and $V_2$, a simpler small-signal model can be used.

Fig. 3 shows the approximate small-signal equivalent circuit of branch 3. Through simulations in SPICE and calculations in Matlab, it was determined that the most significant contributions come from the drain to bulk and source to bulk junction capacitances. The effect of the gate to source and gate to drain capacitances on the overall transfer function is negligible. Equation (6) shows the final expression modeling the noise gain from the power supply to $V_{REF}$.

$$V_{REF} = \frac{\frac{1}{g_{m}}}{\frac{1}{g_{m}} + \frac{1}{C_1}}$$

(6)

$$\frac{V_N}{V_2} = \frac{sC_2}{sC_2 + \frac{1}{R_c} + C_2(\frac{1}{R_c} + \frac{1}{g_{me}}) + \frac{2}{R_c} + \frac{1}{R_c} + \frac{1}{g_{me}}}$$

where $C_1 = a(C_{04} + C_{05})$ and $C_2 = C_{07}$. 

Fig. 2: Small signal equivalent circuit of Branch 2.

Fig. 3: Small signal equivalent circuit of Branch 3.
Fig. 4 compares the actual noise gain from a circuit simulation and the predicted gain from the model. In order to more accurately predict the noise attenuation, a scaling factor (s) between 2 and 3 is inserted in front of the parasitic capacitance in the model. Fig. 4 shows the difference in the model with and without the scaling factor.

When observed at lower frequencies, (6) reduces to (7). Equation (7) is obtained by assuming $\omega = 0$ in (6).

$$\frac{V_{\text{REF}}}{V_N} = \frac{R}{g_m r_o^2 + 2r_o - R}$$  \hspace{1cm} (7)

B. Analysis of Model

The purpose of deriving the models in (6) and (7) was to provide a mathematical expression to aid in the identification of those transistor parameters which have the biggest impact on PSN rejection. From (7), it can be concluded that increasing channel length will improve noise rejection at low frequencies. Increasing channel length and maintaining a constant aspect ratio however, results in an increase in the associated transistor parasitic capacitances. In particular, the drain to bulk and source to bulk capacitances will increase; hence, there will be a shift in the poles and zeros of the full noise model from (6). There is an obvious tradeoff between channel length and noise suppression. Fig. 5 shows the noise gain from 10Hz to 5GHz for increasing channel lengths. Aspect ratios were maintained constant for all transistors as channel lengths were increased.

As predicted from (7), low frequency noise rejection improves as channel length increases; however, increasing the channel length degrades the noise rejection in the range 10kHz to 100MHz. This can be attributed to the shifting of the zero to the left due to an increase in the associated parasitic capacitance. Beyond 100MHz there is no significant improvement in the noise rejection as channel length is varied. Noise below 100MHz can be suppressed by off-chip decoupling capacitors [2]. Noise beyond 100MHz however, has a higher probability of being encountered on-chip. A solution to improve high frequency noise rejection is presented in the following section.

C. Improving Noise Rejection Performance

Observing (6), it is apparent that changing the capacitance at $V_{\text{REF}}$ can shift the pole location. Moving the pole to the left will result in an improvement in high frequency noise rejection. This can be achieved by inserting a capacitance to ground at $V_{\text{REF}}$. At this point, one might argue that a capacitor can be placed on $V_{\text{DD}}$ rather than at $V_{\text{REF}}$ and would serve the same purpose. The reason for not exploring this option for reducing PSN is because a large capacitor would be needed to reduce the noise directly at $V_{\text{DD}}$. By placing a capacitor at $V_{\text{REF}}$ instead, a small capacitor can achieve the same PSN rejection as placing a large capacitor at $V_{\text{DD}}$.

Capacitances in the range 0.5pF to 2.5pF provide a significant improvement in high frequency noise rejection. On-chip metal-insulated-metal capacitors can easily be used to produce capacitances of this order. Fig. 6 shows the improvement in noise rejection as the capacitance at $V_{\text{REF}}$ is increased. Adding a 1pF capacitor at $V_{\text{REF}}$ provides approximately -18dB of attenuation at 2GHz, whereas before there was almost no noise rejection. Fig. 5 shows that a channel length of 0.48$\mu$m provides a good tradeoff between noise rejection at low frequencies and noise rejection in the

![Fig. 5. Gain of power supply noise for various channel lengths. (Bubbles show the scaling factor from the minimum channel length of 0.24$\mu$m)](https://example.com/image1.png)
range 10kHz to 100MHz. Thus, a constant channel length of 0.48μm was used to obtain the resulting graph in Fig. 6.

IV. TECHNOLOGY SCALING

As the semiconductor roadmap indicates, supply voltages will continue to reduce while transistors dimensions are scaled [3]. PSN will become an increased problem for circuit and package designers as noise margins shrink and more circuits are combined in a single chip. In order for a circuit to be reused in a future technology node, it must maintain an acceptable amount of noise rejection. Degradation of the noise rejection would result in expensive redesigns or require additional power supply decoupling capacitors.

Since channel length modulation coefficients increase with newer process technologies, one would assume that at low frequencies noise rejection would improve. Also, since parasitic capacitances are smaller, it would be expected that the location of the poles and zeros would move to the right; hence, providing a larger frequency range where noise is rejected. Table 1 compares the actual noise gain at various frequencies for the 0.18μm and 0.25μm processes. Aspect ratios and bias currents were maintained constant across technologies.

It is evident that for this particular voltage reference, when no capacitance is included, PSN rejection is similar for both technologies. Not evident from table 1 however, is that the circuit using the 0.18μm process requires a smaller capacitance at V_REF to improve high frequency noise rejection. To achieve the same high frequency noise rejection figure, a larger capacitance is needed in the 0.25μm process. For example, to obtain a gain of -22dB at 2GHz, the circuit in the 0.25μm process requires approximately 2pF of capacitance, whereas the 0.18μm process requires only 1pF.

V. CONCLUSION

With increasing levels of integration, controlling PSN will become a major design effort for both package and circuit designers. The current design method involves placing decoupling capacitors on the package and on-chip to reduce noise levels. However, the number of decoupling capacitors is overestimated for the purpose of ensuring signal integrity. Study of the mechanism that affect the PSN in standard circuits is imperative for efficient decoupling solutions, saving valuable silicon space.

In this paper, the PSN sensitivity of a voltage reference was analyzed. It was determined that there exists a tradeoff between low and high frequency noise rejection and channel length. Also, by adding an on-chip capacitor, high frequency noise rejection can be improved. Comparison of two successive technology nodes indicates that PSN coupling trends and rejection solutions remain consistent for both technologies. On-chip decoupling in the 0.18μm process shows that noise rejection can be achieved with even less area in future processes.

TABLE I

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Gain in 0.25μm Process (dB)</th>
<th>Gain in 0.18μm Process (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1kHz</td>
<td>-59.22</td>
<td>-59.22</td>
</tr>
<tr>
<td>100kHz</td>
<td>-49.55</td>
<td>-49.56</td>
</tr>
<tr>
<td>1MHz</td>
<td>-30.08</td>
<td>-30.21</td>
</tr>
<tr>
<td>10MHz</td>
<td>-10.4</td>
<td>-16.28</td>
</tr>
<tr>
<td>100MHz</td>
<td>0.52</td>
<td>-17.68</td>
</tr>
<tr>
<td>1GHz</td>
<td>-0.29</td>
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</tr>
<tr>
<td>2GHz</td>
<td>-0.27</td>
<td>-21.14</td>
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<tr>
<td>5GHz</td>
<td>-0.15</td>
<td>-21.07</td>
</tr>
</tbody>
</table>

REFERENCES


